Enhancement of the ATLAS Trigger System with a Hardware Tracker Finder FTK

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for the FTK collaboration

Outline

- **Motivation**

- **FTK approach**

- **System overview and component functionality**

- **Performance**

  - **Single particle efficiency and timing**

  - **Identifying physics objects at 3×10^{34}**

- **Summary**

Trigger with Tracks

- **Enhancement of the capability to examine the event characteristic at the LVL1 rate with all tracks**

- **Identification of heavy fermion objects originated from possible new physics scenarios (e.g., Higgs decay) in the enormous QCD jet background**

  - b-jets: displaced vertices or tracks with large impact parameter
  - τ-jets: 1 or 3 tracks in a narrow cone with a surrounding isolation region

- **Effective lepton selection with tracking isolation**

The challenge & the Solution

- **The increasing LHC luminosity leads higher rate and larger event size.**
    - The trigger problem at high P_T can't be solved by just increasing thresholds
    - Suppression of the higher background rates will require more sophisticated algorithms in earlier trigger levels
    - Pileup increases the need for tracking and its execution time

- **With introducing FTK, the global tracking would be completed at the beginning of the Level-2 trigger (LVL2). Thus the LVL2 processing power can be used more on needed sophisticated algorithms.**
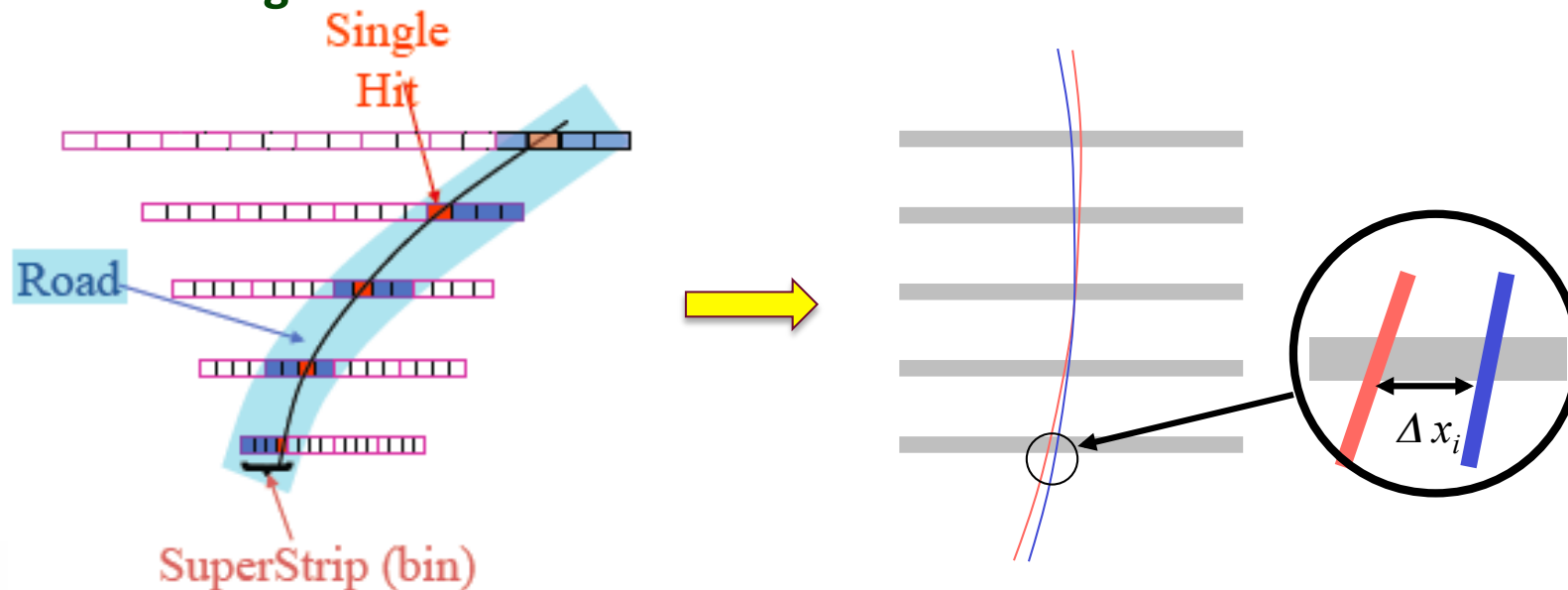
ATLAS TDAQ+FTK
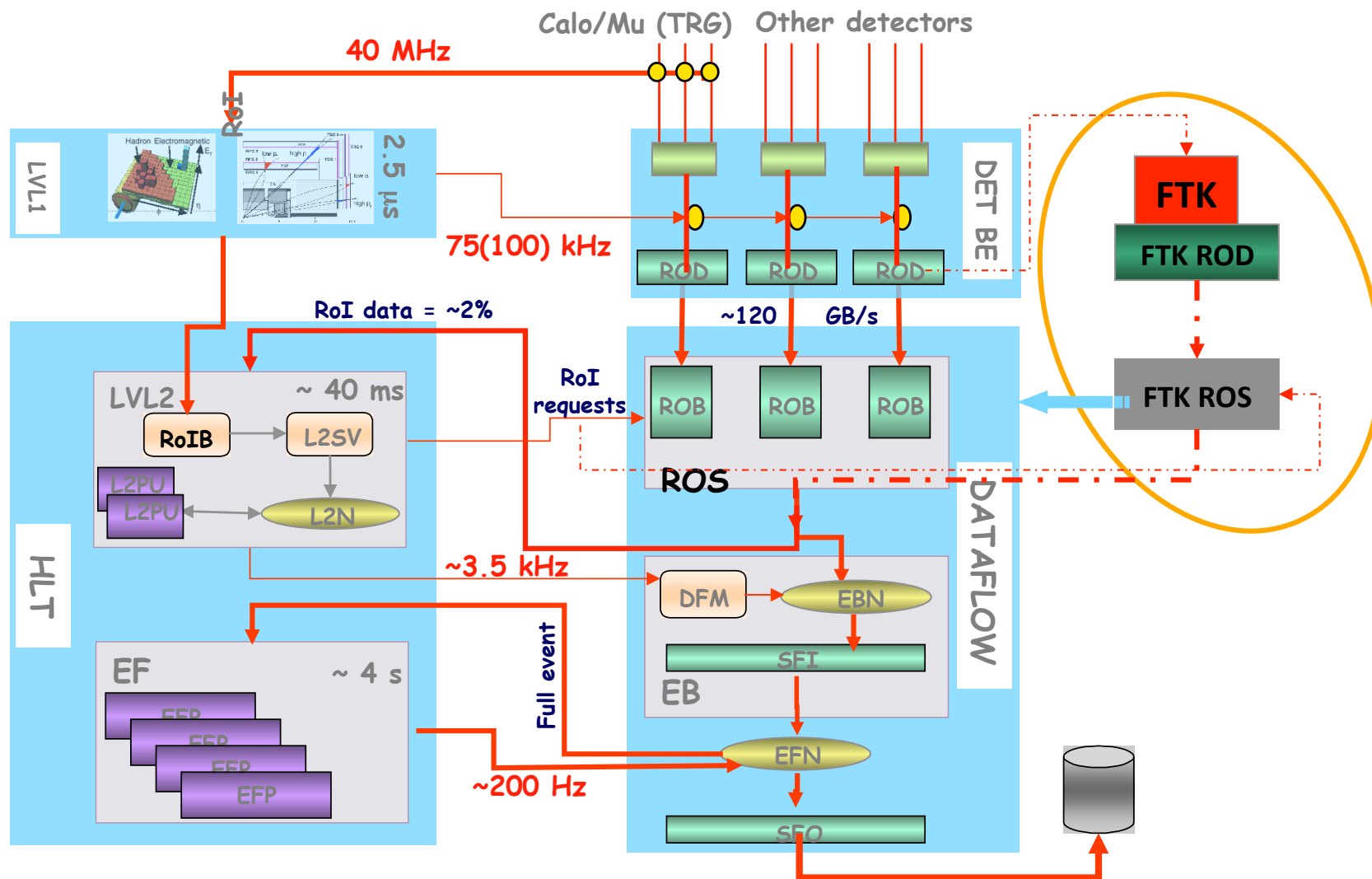
Fast TracKer (FTK) Approach

Use hardware to perform the global tracking in two steps pattern recognition and track fit
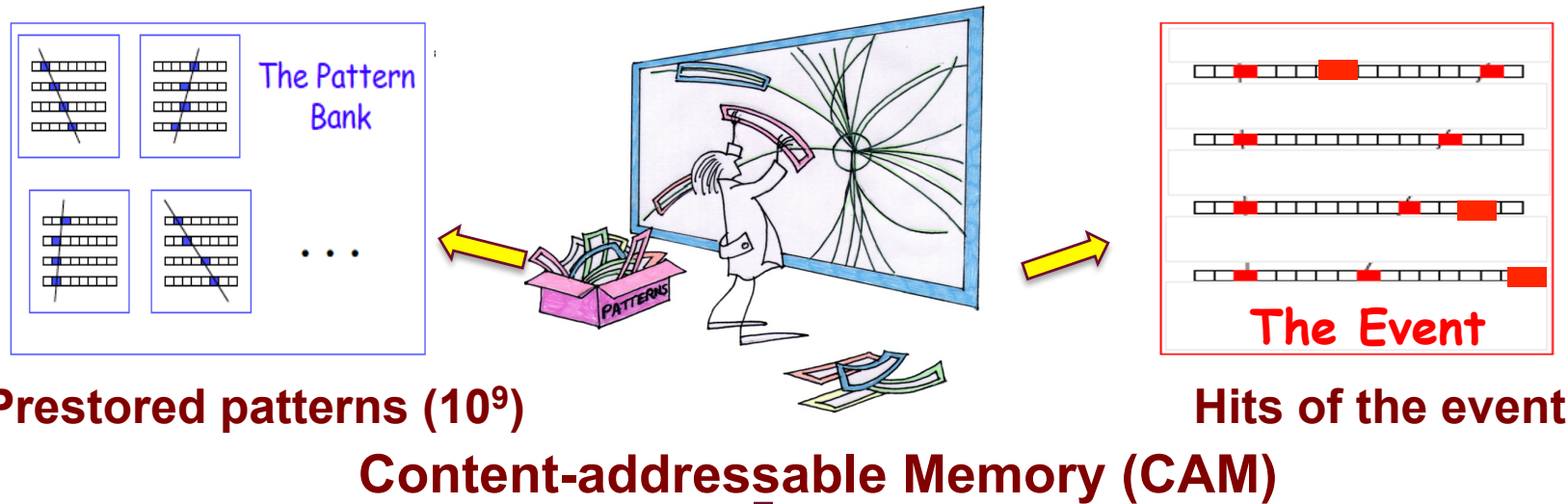
Single
Hit

Road

SuperStrip (bin)

Δx_i

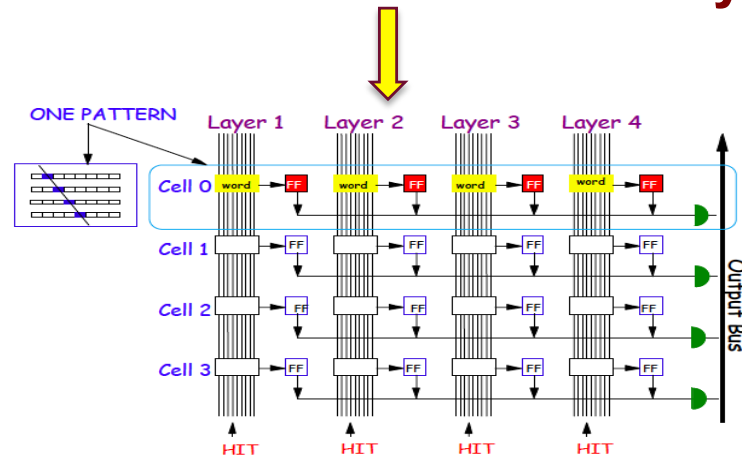**Pattern recognition in coarse resolution (superstrip➔road)**

Track fit in full resolution (hits in a road)

$F(x_1, x_2, x_3, ...) \sim a_0 + a_1 \Delta x_1 + a_2 \Delta x_2 + a_3 \Delta x_3 + ... = 0$

Road size to balance the workload between two steps

Pattern Recognition

Prestored patterns (10^9)

Hits of the event

Content-addressable Memory (CAM)

Fast pattern recognition

Content-addressable Memory (CAM)

- **Take user data as input rather than the address**

- **Search the entire memory in a single operation**

- **Used often in network search elements**

- **Available commercially and in HEP custom design (limited)**
  - INFN AM able to identify correlation among input data words received on different clock cycles

	AM INFN (2004)	CAM (latest)
Availability	Non-commercial	Good
Technology	180 nm	55 nm
Speed	40 MHz	500 MHz
Size	(6x16) X 5K	36X 1024K, 576X 64K
Max Channels	384K	576
Flexibility	Low	High
Price	10-15 €	O (100-200 €)

INFN
Istituto Nazionale
di Fisica Nucleare

NETLOGIC
MICROSYSTEMS

1) IEEE Trans.Nucl.Sci.53:2428-2433,2006
2) http://www.netlogicmicro.com/Products/Layer2/Layer2-3.htm
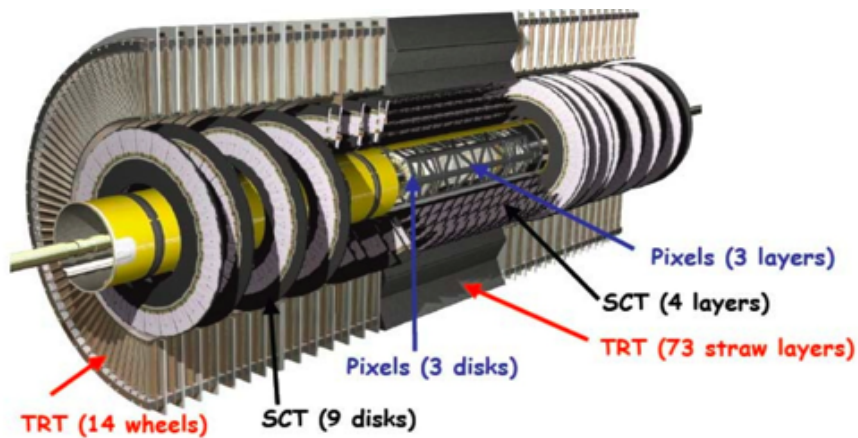
Track Fitting

- **Determine the helix parameters and χ^2**

- **Fit with the local silicon hit coordinates (one module in each layer) in linear**

$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

  - **P_i: the helix parameters and χ^2 components**
  - **X_j: the hit coordinates in the silicon layers**
  - **a_{ij} & b_i: prestored constants determined from full simulation or real data track**

- **Very fast in DSPs (~1 ns per track)**
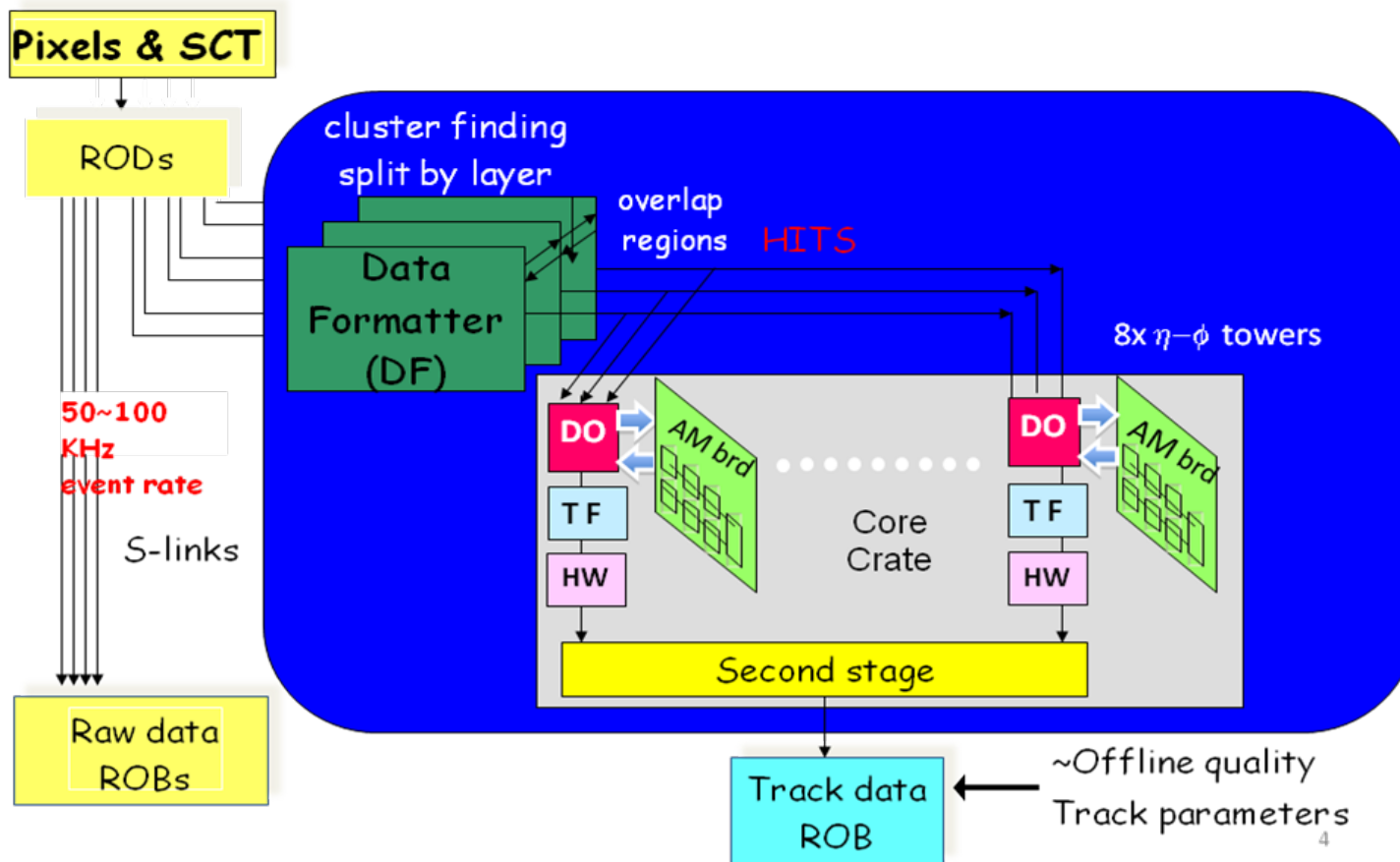
System Overview

- PIX (3 layers) & SCT (4 double layers)
- Architecture of 11 layers in one step (PIX 3 + SCT 4 axial + SCT 4 stereo) unaffordable
- Options:
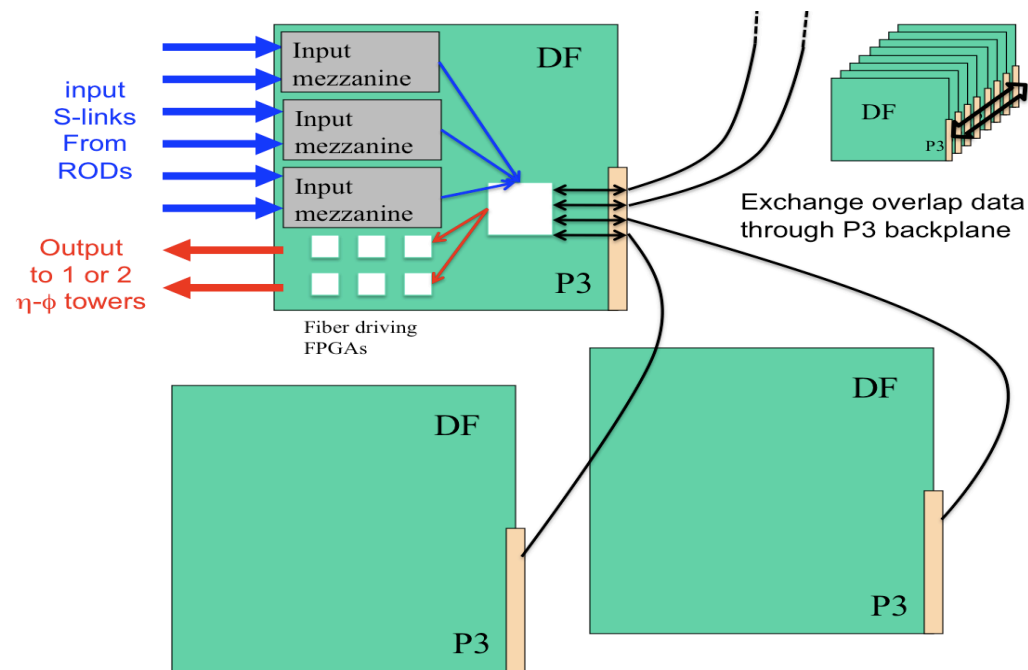 - 7 layers (PIX 3 +SCT 4 axial)
  - SCT[1st] – PIX[2nd] (8➔4)

- 8 ϕ sectors, each with one crate, 8 (12) crates @ 10^{34} (3×10^{34}) total
- 4X2 η−ϕ towers in each sector, each tower with one slot unit
- Overlaps to maintain high efficiency

# System Functional Sketch

Data Formatter (DF)

- **Receive the silicon hits from the pixels and SCT**
- **Perform cluster finding (2D in pixels)**
- **Sends the cluster centroids to the appropriate η-ϕ towers in the core crates**

Process Unit (AM board)

- **Contain 4 mezzanine cards, each connected to a separate DO, TF, HW chain.**

- **The mezzanine card holds 32 custom standard-cell content-addressable memory chips**
  - **3.7K patterns per existing AM chip (for 8 layers); 1.8 W power consumption per chip**
  - **60-135K patterns possible for the next generation chip (65-90nm, custom cell, larger size, 3D technology)**

    1) Associative Memory design for the FastTrack processor (FTK) at ATLAS (ATL-DAQ-PROC-2010-013)

- **Tree Search Processor (TSP) improves the resolution by a factor 2 to reject fake roads before track fitting**
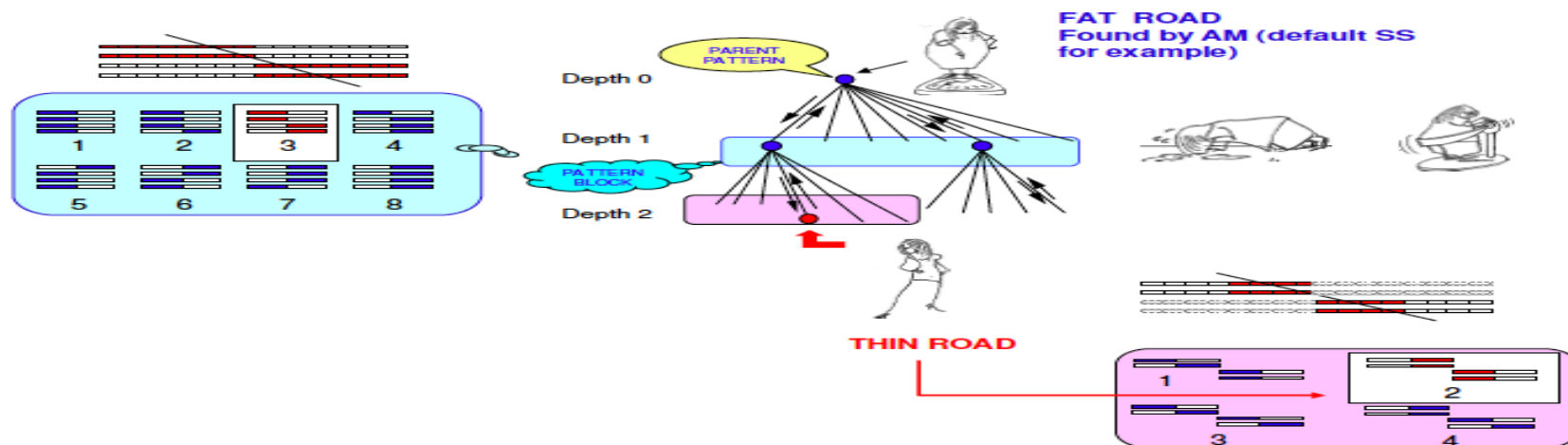
Process Unit (AUX card)

- **Data Organizer (DO)**
  - **Store full resolution hits in a smart database**
  - **Send hits at a coarser resolution to the Associative Memory (AM) for pattern recognition**
  - **Fetch the hits in a road and send to the Track Fitter for a matched pattern**

- **Track Fitter (TF)**
  - **Use DSPs in an FPGA to calculate the helix parameters and the components of the χ^2**
  - **store the constants in the internal FPGA memory**
  - **Expect ns per track with 288 DSPs in the FPGA being considered**

- **Hit Warrior (HW)**
  - **Remove duplicate tracks defined as having more than N hits in common with another track**
  - **Employ an associative memory built on the fly and implemented in an FPGA**

# Processor Unit Prototype
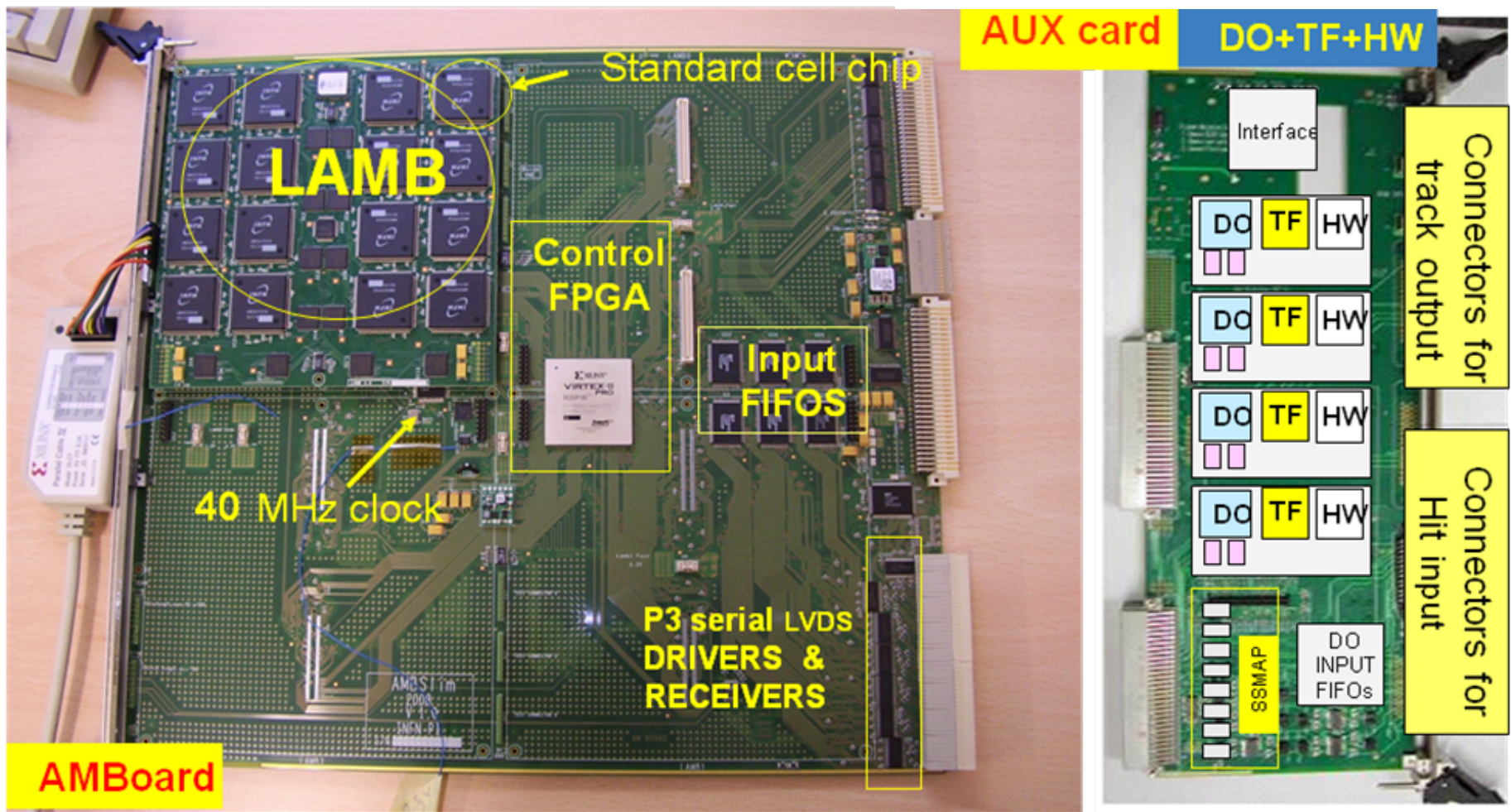
Interface to the Current TDAQ

- **Input**
  - **Dual output SLINK interface in the RODs of PIX and SCT**

- **Output**
  - **ROD: The tracks from the second stage that pass a χ^2 cut are sent to a ROD**
  - **ROS: Special configuration or special running mode is necessary.**
    - **The typical output event size for all tracks with PT > 1 GeV/c at 3×10^{34} is 5.0 kB.**
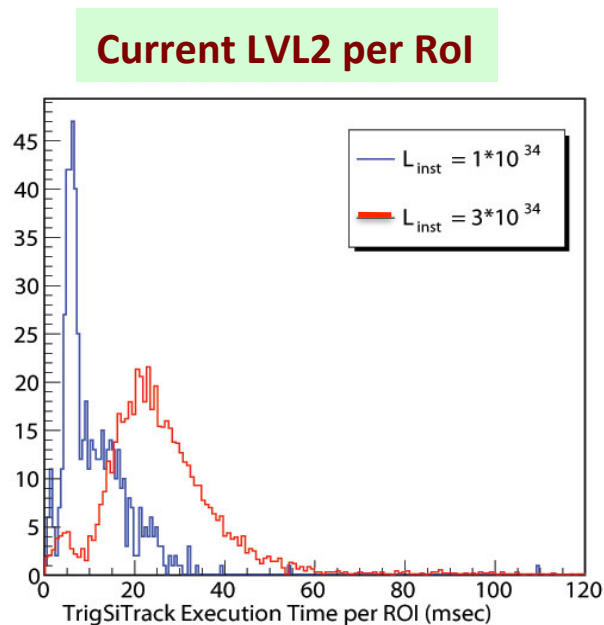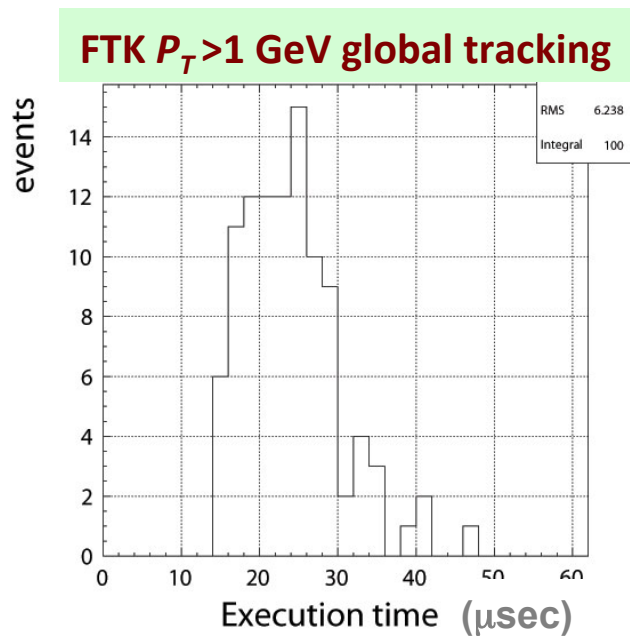   - **Data is desirable at the full LVL1 rate for the LVL2 algorithms.**

Single Track Efficiency
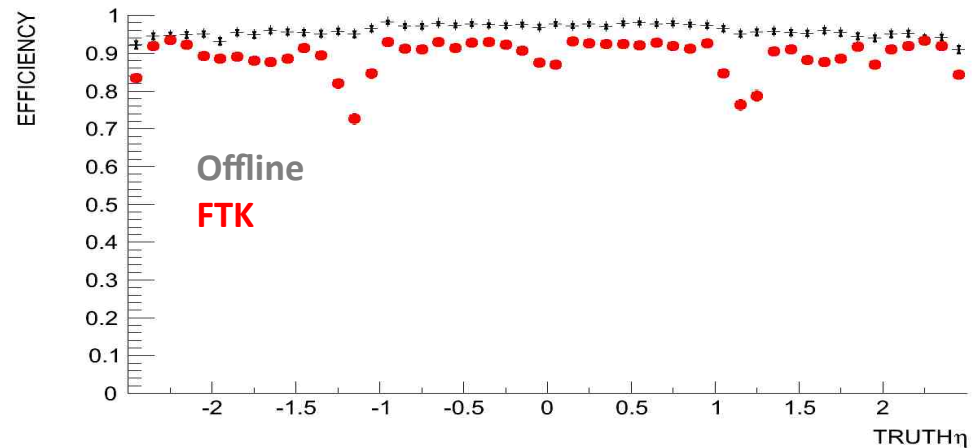
- **The overall efficiency has not yet been optimized**
- **The dip at η = 0 is an artifact of how we produced the pattern bank**
- **The dip near $|\eta|$ = 1.2, the region between the barrel and the forward, will be optimized**

Timing

FTK P_T >1 GeV global tracking

Current LVL2 per RoI

- **WH(bb) MC events are used.**
- **FTK finishes global tracking in 25 μs at 3×10^{34}.**
- **Current LVL2 need 25 ms per jet or lepton RoI at 3×10^{34} and the number of RoIs is large**

Summary

- **Global tracking can make a significant contribution to the ATLAS trigger.**

- **A conceptual design shows that an affordable FTK will take less than 100 μs/event at the LHC design luminosity and beyond, and have excellent physics performance.**

- **The implementation can help ATLAS even at low luminosity.**
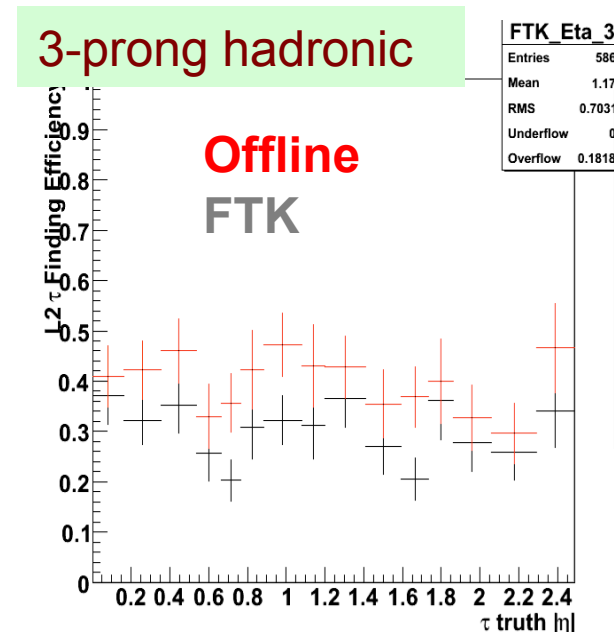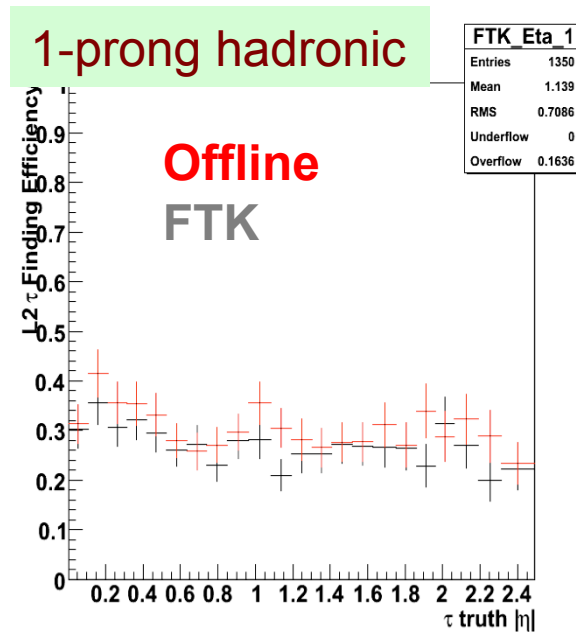
# Single Track Helix Parameter Resolution
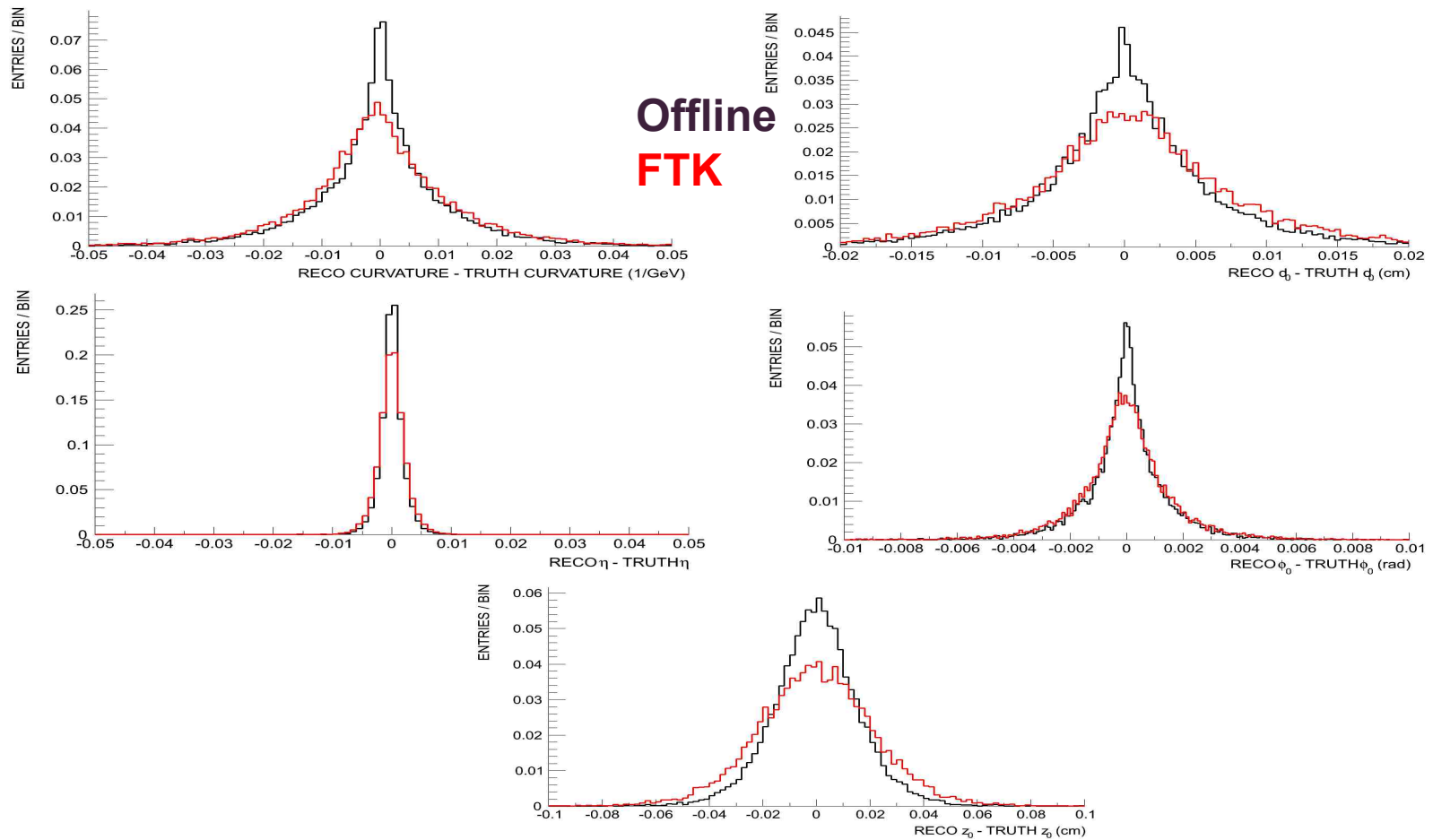
b-tagging at 3×10^{34}
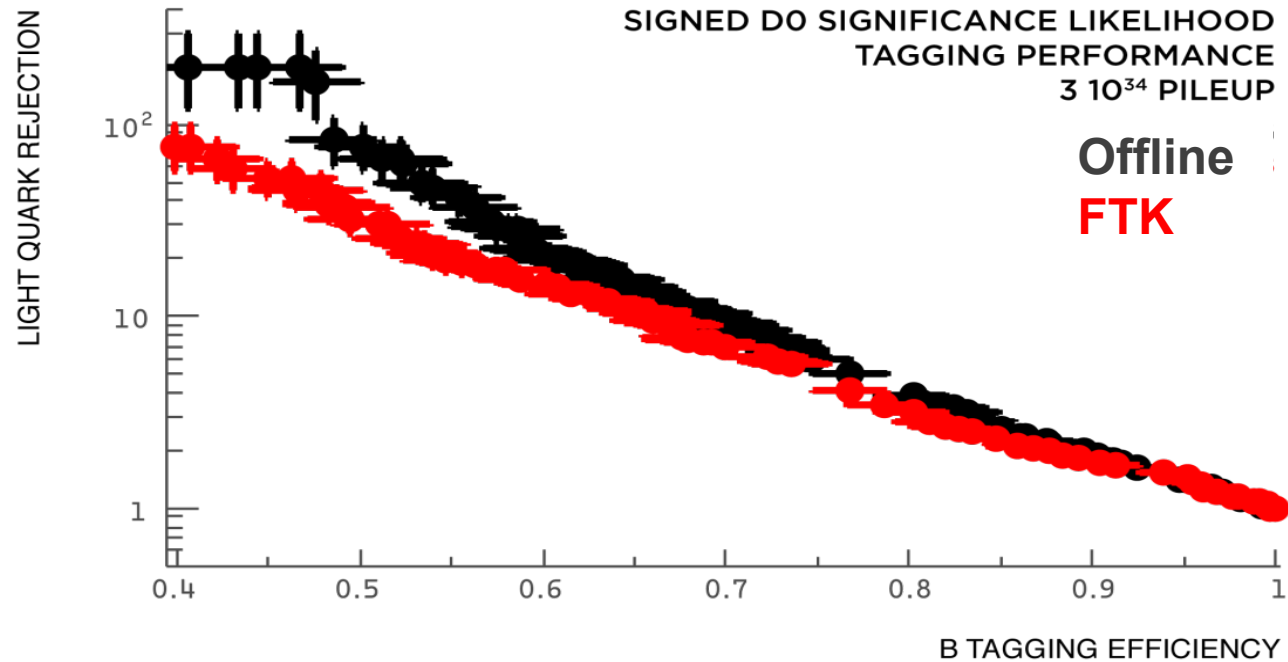
- **Using signed impact-parameter significance likelihood tagger**
- **To test more sophisticated b-taggers to have a larger light-quark rejection**

τ-tagging at 3×10^{34}

- Requiring 1 (2 or 3) tracks in the signal cone for 1 (3) prong τ's and no tracks with P_T >1.5 GeV/c in the isolation cone
- With ~10^{-3} jet fake probability

Lepton (muon) Isolation at 3×10^{34}
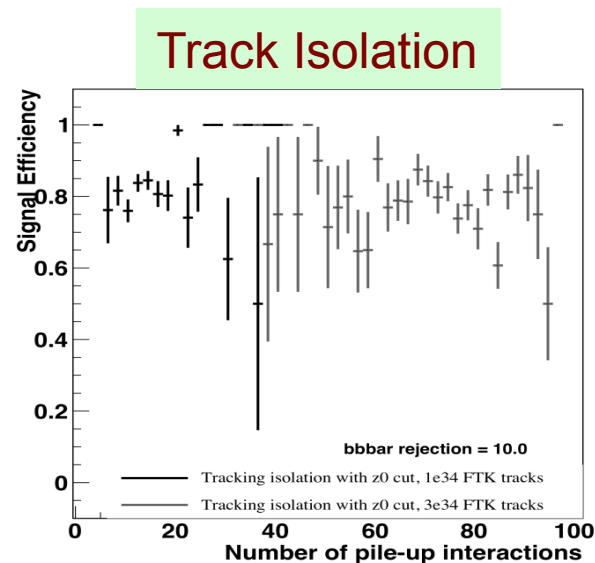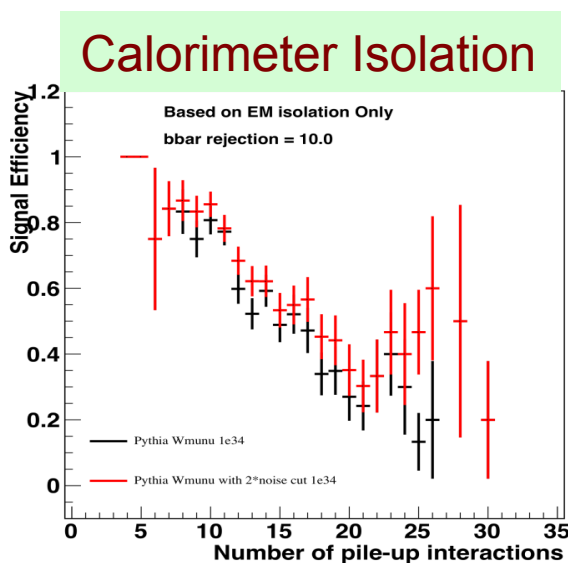
- **Calorimeter isolation usually used to suppress QCD background but will deteriorate due to energy from 75 pileups at 3×10^{34}**
- **Track isolation will still work due to using only tracks pointing within a few mm of the muon at the beamline**