Highly Pixelated Transparent Devices for Future Vertex Detectors

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(on behalf of the MIMOSA, PLUME, HP-2 & AIDA collaborations)

▷ **more information on IPHC Web site: http://www.iphc.cnrs.fr/-CMOS-ILC-.html**

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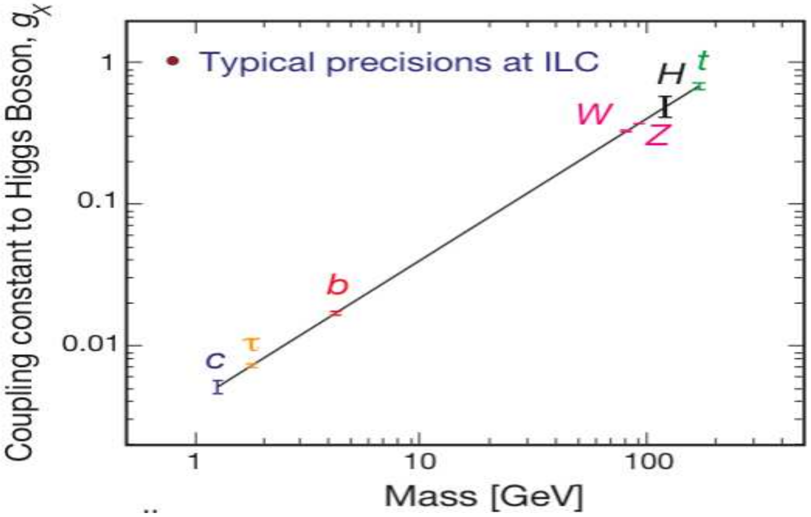
The Trend for Ultra-Light Pixelated Devices

- **Trend of subatomic physics experiments for highly granular and thin pixel devices**
- **Central motivation :**
  - ⋇ high performance reconstruction of (displaced) charm vertices
  - ⋇ high performance multi-jet final state flavour tagging ($t\bar{t}$, $t\bar{t}H$, AH, ...)
- **Flagship of this trend : International Linear Collider (ILC)** $\rightarrowtail$ Letters of Intent delivered in 2009
  $\hookrightarrow$ Detector Baseline Document ($\simeq$ TDR) to be delivered by 2012
  - ⋇ also: Heavy Ion experiments, CLIC, LHC upgrades, ..., hadrontherapy, ...

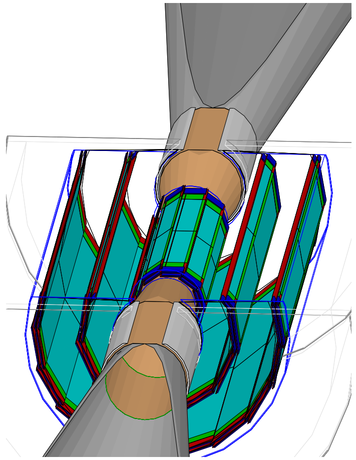
$\hookrightarrow$ Figure of merit : $\sigma_{\mathbf{ip}} = \mathbf{a} \oplus \mathbf{b}/\mathbf{p} \cdot \sin^{\mathbf{3/2}} \theta$

⋇ a governs high momentum ⋇ b governs low momentum ($\sim$ 30 % particles $<$ 1 GeV/c)

Accelerator	a (μm)	b ($\mu m \cdot GeV$)
LEP	25	70
SLD	8	33
LHC	12	70
RHIC-II	12	19
ILC	$<$ 5	$<$ 10

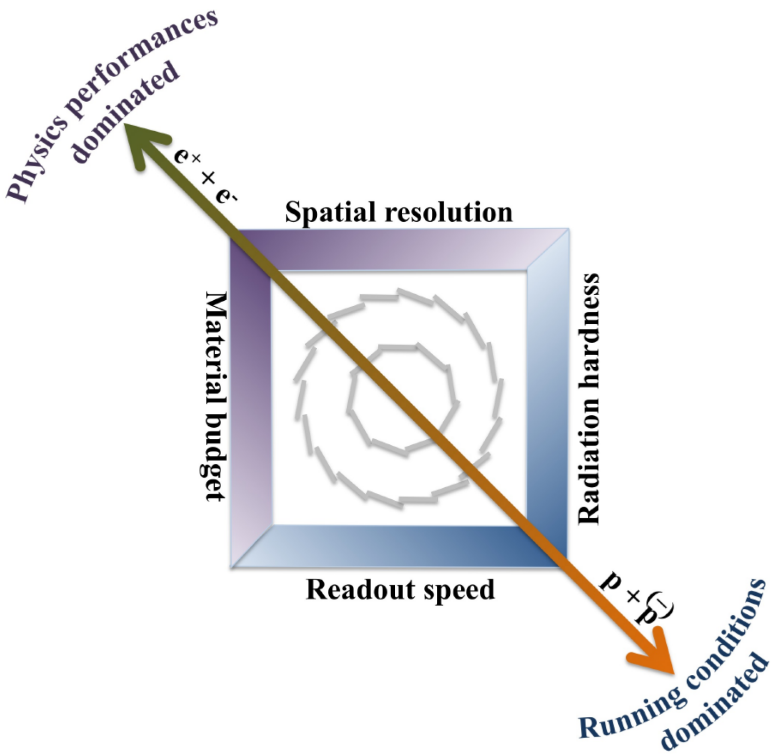


On-Going R&D



- Several R&D activities since $\sim$ 1 decade
  - ⋇ mainly driven by the ILC physics program
  - ⋇ originating from various starting points

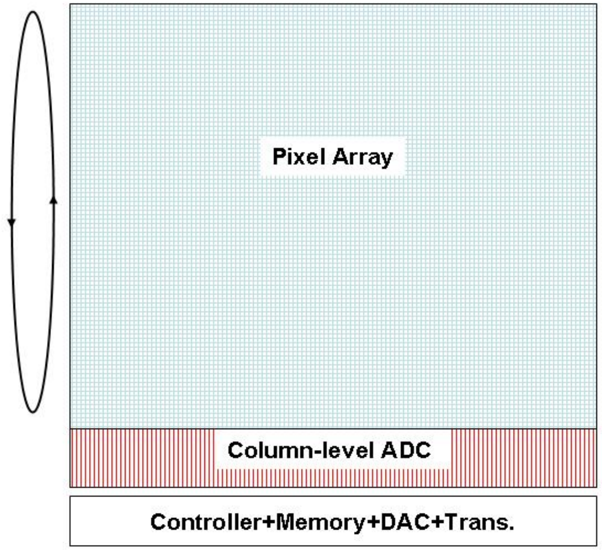
- Main R&D devt lines on highly granular and thin pixel sensors:
  - ⋇ SLD-VTX based on CCDs (a=8, b=33, $t_{r.o.}$ = 200 ms)
    - ⟶ CPCCD, FPCCD, ISIS
  - ⋇ X-Ray imager
    - ⟶ DEPFET
  - ⋇ industrial CMOS pixel imagers
    - ⟶ MIMOSA, APSEL, CAPS, Chronopix, ...



- Prominent difficulties:
  - ⋇ Suppressed material budget (m.s., N_γ)
    - ⇛ constrains pixel technology & services
      - ⇛ vigorous upstream R&D
  - ⋇ Be as close as possible to the I.P. (short lever arm)
    - ⇛ Speed (occupancy !) & radiation tolerance (beam & physics related)

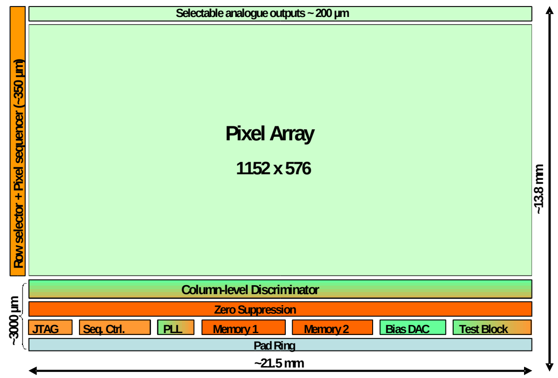
CMOS Pixel Sensors: State of the Art

- **Prominent features of CMOS pixel sensors:**
  - ⋇ high granularity ⇛ excellent (micronic) spatial resolution
  - ⋇ very thin (signal generated in 10-20 μm thin epitaxial layer)
  - ⋇ signal processing μ-circuits integrated on sensor substrate



- **Sensor organisation:**
  - ⋇ signal sensing and analog processing in pixel array
  - ⋇ mixed and Digital circuitry integrated in chip periphery
  - ⋇ read-out in rolling shutter mode

    (pixels grouped in columns read out in //)

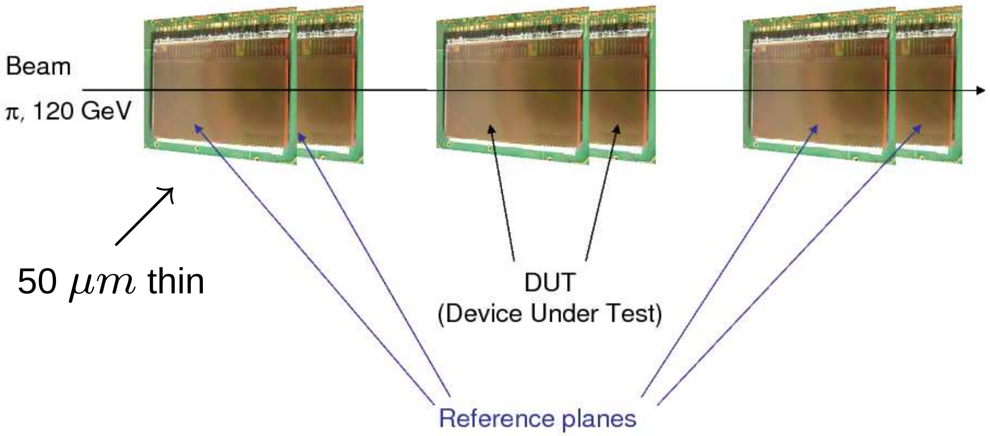


- **Main characteristics of MIMOSA sensor equipping EUDET BT:**
  - ⋇ 0.35 μm process with high-res. epitaxy (coll. with IRFU/Saclay)
  - ⋇ column // architecture with in-pixel amplification

    and end-of-col. discrimination, followed by $\emptyset$
  - ⋇ active area: 1152 columns of 576 pixels (21.2×10.6 mm^2)
  - ⋇ pitch: 18.4 $\mu m \rightarrowtail \sim$ 0.7 million pixels ⇛ $\sigma_{sp} \lesssim 4\ \mu m$
  - ⋇ T$_{r.o.} \lesssim 100\ \mu s$ ($\sim 10^4$ frames/s) ⇛ suited to $>10^6$ part./cm^2/s

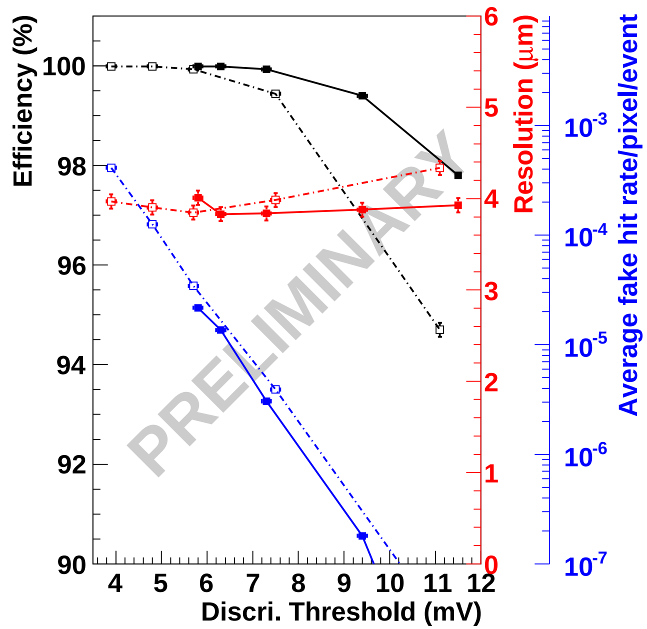
High-Resistivity CMOS Pixel Sensors

- **M.i.p. detection with LOW & HIGH resistivity CMOS sensors combined in a Beam Telescope (BT)**
  - ⁜ 4 EUDET ref. sensors & 2 sensors under test
  - ⁜ June 2010 at CERN-SPS ($\sim$ 120 GeV pions)
  - ⁜ sensor variants : standard epitaxy (14 μm thick)
    & high-resistivity epitaxy (10 & 15 μm thick)

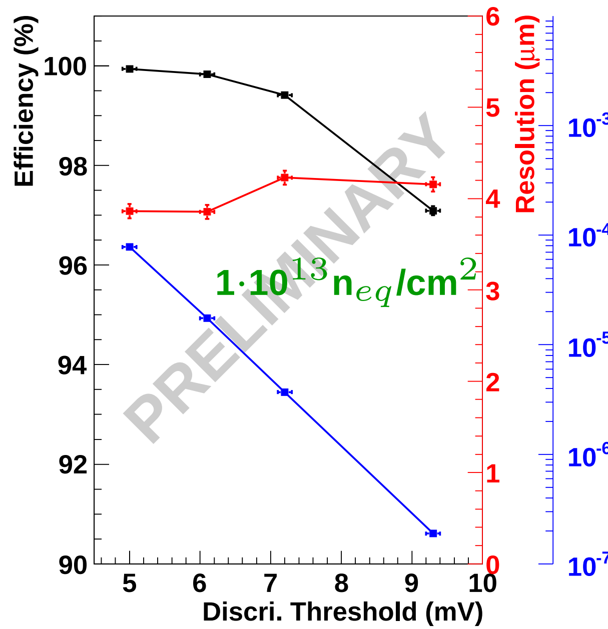


- **Preliminary conclusions:**
  - ⁜ det. eff. $\sim$ 100 % (SNR $\sim$ 40) for very low fake rate:
    - ▷ plateau until fake rate of few 10^{-6}
  - ⁜ single point resolution $\lesssim$ 4 μm
  - ⁜ det.eff. still $\sim$ 100 % after exposure
    to fluence of $1{\cdot}10^{13} n_{eq}/cm^2$

Mi26 HR-15 and HR-10 Efficiency, Fake rate and Resolution



Mi26 HR-15 Efficiency, Fake rate and Resolution
for a chip irradiated with a $1.10^{13}N_{eq}$ dose at T_{op} ~ 0° C



$\Rightarrow$ **Excellent detection performances**
with high-resistivity epitaxial layer
despite moderate resistivity (400 $\Omega \cdot cm$)
and poor depletion voltage ($<$ 1 V)

$\Rightarrow$ **Tolerance to $\gtrsim$ O(10^{14}) n_{eq}/cm^2 seems within reach (study under way)**

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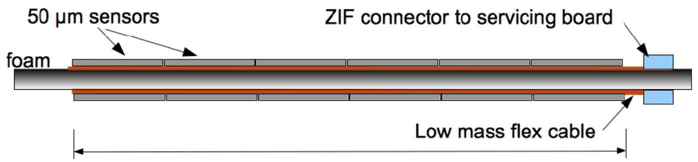
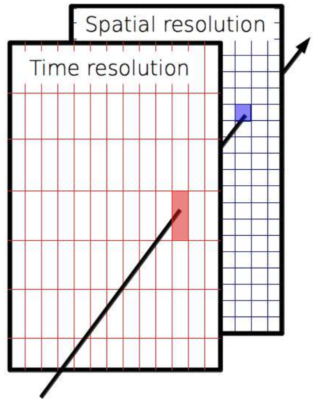
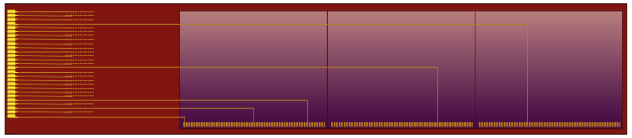
Sensor Integration in Ultra Light Devices

- **Double-sided ladders with time stamping :**
  - ⋇ expected added value of 2-sided ladders:
    alignment, pointing accuracy (shallow angle), etc.
  - ⋇ studied by PLUME coll. (Oxford, Bristol, DESY, IPHC) & AIDA (EU)
    ↪ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - ⋇ square pixels for single point resolution on beam side
  - ⋇ elongated pixels for 4-5 times shorter r.o. time on other side
  - ⋇ correlate hits generated by traversing particles
  - ⋇ expected total material budget $\sim$ 0.2 - 0.3 % X_0

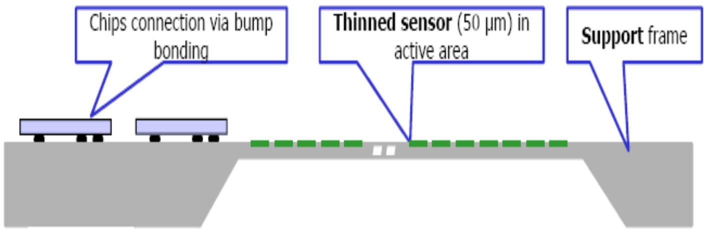




- **Unsupported & flexible (?) ladders (Hadron Physics 2 / FP-7)**
  - ⋇ 30 μm thin CMOS sensors mounted on thin cable
    and embedded in thin polyimide $\rightarrowtail$ suited to beam pipe ?
  - ⋇ expected total material budget $\lesssim$ 0.15 % X_0

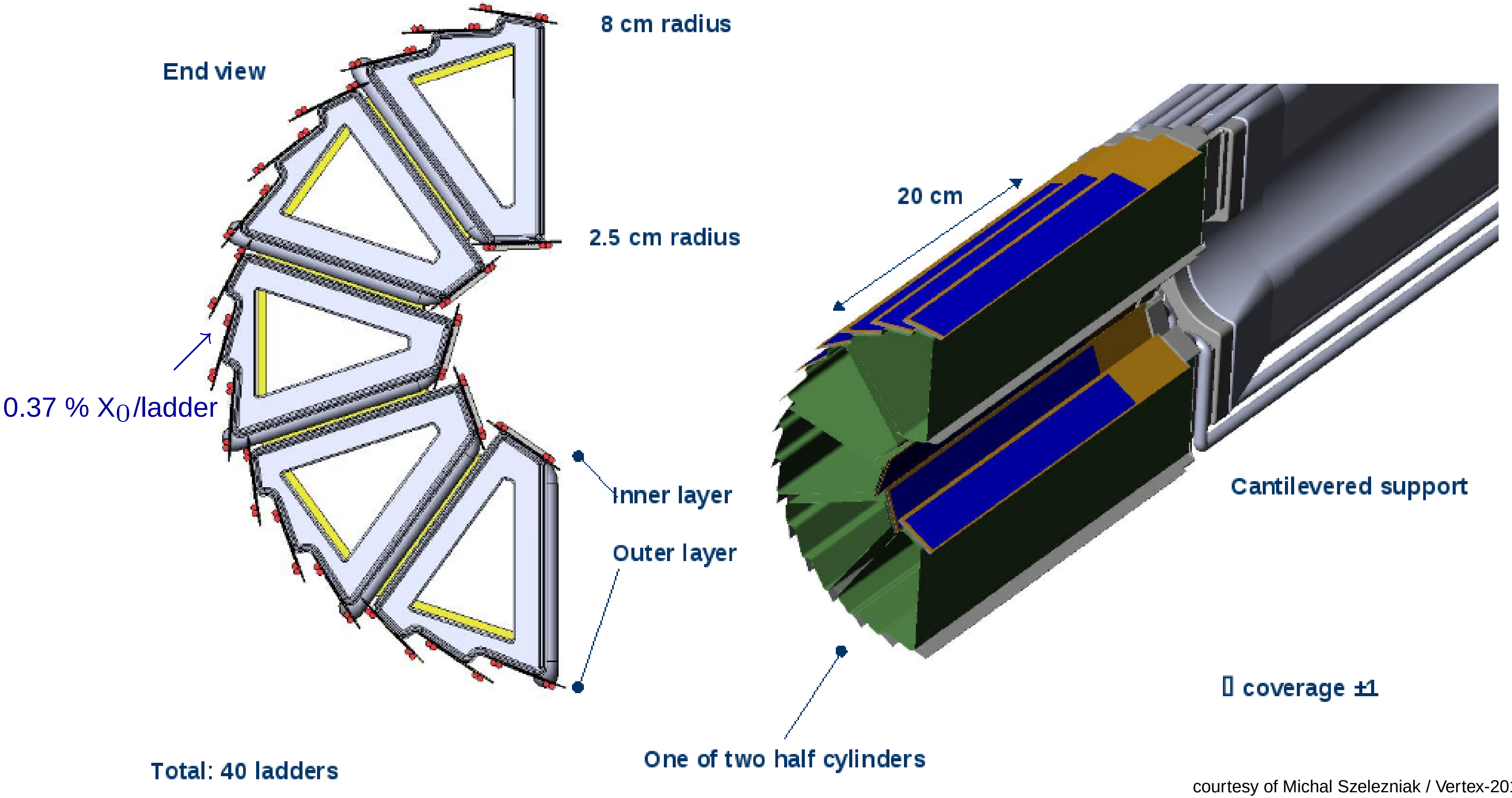


- **All silicon almost monolithic device (DEPFET):**
  - ⋇ sgle piece ladders using bulk Si of sensors as mechanical supports
  - ⋇ expected total material budget $\lesssim$ 0.2 % X_0 (average)



Application of CMOS sensors to the STAR-PIXEL

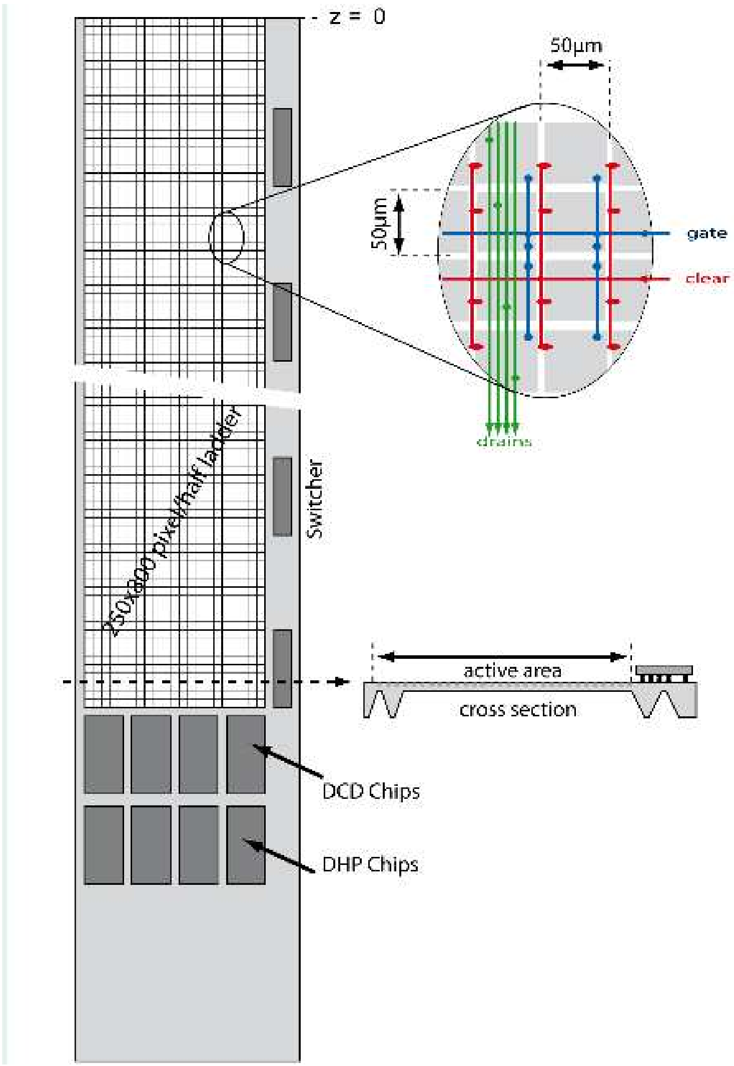
The detector ladders are 50 µm thinned silicon, on a flex kapton/aluminum cable.

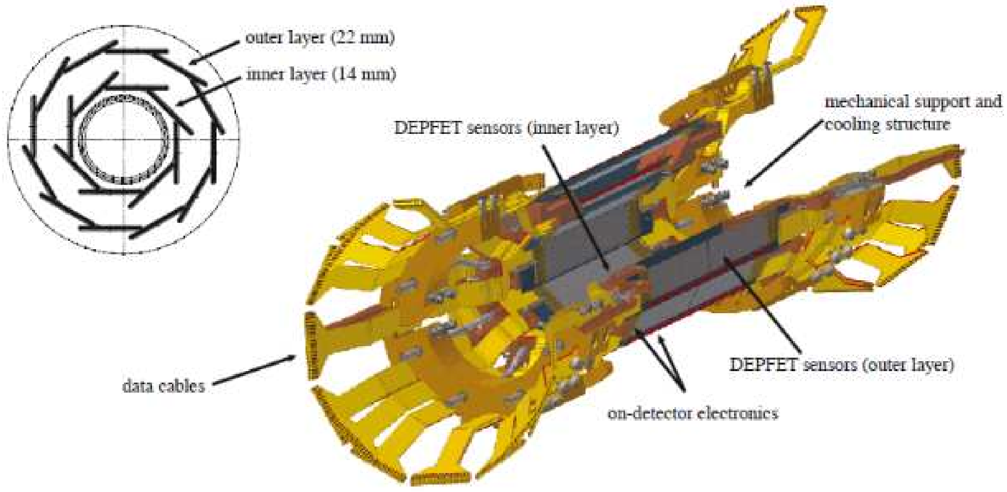


courtesy of Michal Szelezniak / Vertex-2010

▷▷▷ **1st vertex detector equipped with CMOS pixel sensors ⟶ 1st data taking in 2012/13**

Application of DEPFET sensors to the BELLE-2 Vertex Detector





- Two DEPFET layers at 1.4 cm and 2.2 cm radius
- Ladders : 8@L1, 90 mm, 12@L2, 123 mm, ≈25 Mpixel
- frame rate : 100kHZ
- material budget : 0.19% X_0 (incl. frame, chips, bumps)
- power/ladder : DEPFETs ~ 1 W
  Switcher ~ 1 W
  DCD/DHP ~ 8 W on each ladder end

courtesy of Laci Andricek / NSS-MIC 2009

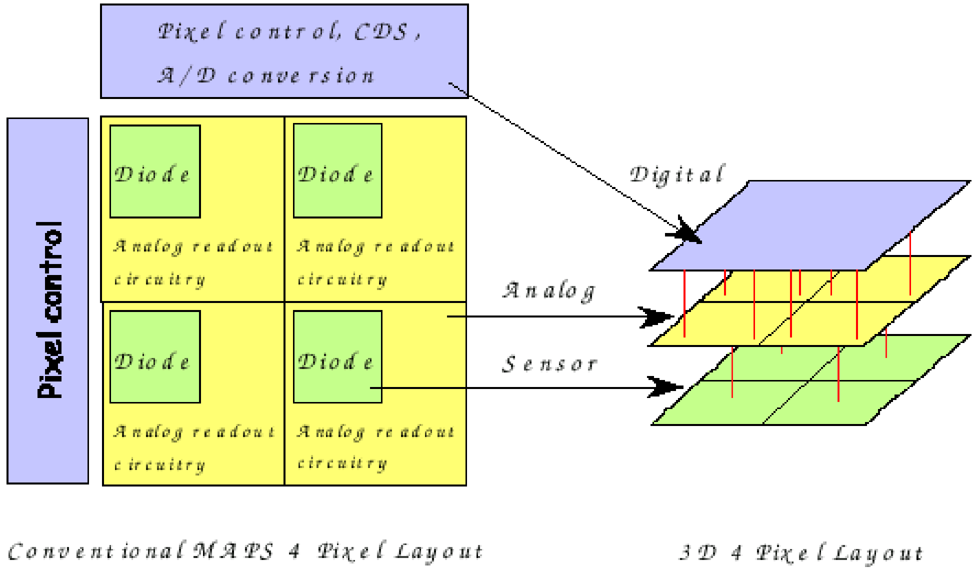
▷▷▷ **1st vertex detector equipped with DEPFET sensors ⟶ 1st data taking expected in 2014**

3DIT to achieve Ultimate CMOS Sensor Performances

- **3D Integration Techno.** allow integrating high density signal processing μcircuits inside small pixels

- **3DIT are expected to be particularly beneficial for CMOS sensors :**
  - ⋇ combine different fabrication processes
  - ⋇ alleviate constraints on transistor type inside pixel

- **Split signal collection & processing functionnalities using optimal technology in each tier :**
  - ⋇ Tier-1 : epitaxy (depleted or not), deep N-well ?
  - ⋇ Tier-2 : analog, low I_{leak}, process (nb of ML)
  - ⋇ Tier-3 (& -4) : digital VDSM process (nb of ML),
    $\rightarrowtail$ fast laser (VOCSEL) driver, etc.



- **The path to nominal exploitation of CMOS pixel potential :**
  - ⋇ fully depleted 10-20 μm thick epitaxy $\Rrightarrow$ $\lesssim$ 5 ns collection time, rad. hardness $>$ Hybrid Pix. Sensors ???
  - ⋇ FEE with $\leq$ 10 ns time resolution $\rightarrowtail$ solution for CLIC & HL-LHC specifications ???

- **Devt of** CAIRN $\equiv$ **C**MOS **A**ctive pixel sensors with vertically **I**ntegrated **R**ead-out and **N**etworking functionnalities
  $\hookrightarrow$ 1st set of 4 chips submitted to foundry in Spring 2009 (within 3DIC)

SUMMARY – CONCLUSIONS

- **ILC drives (since $\sim$ 1 decade) an R&D prog. on novel, highly granular and thin, pixelated devices introducing a new performance standard for vertex detectors:**
  - ⋇ new pixel technologies: CMOS pixel sensors, DEPFETs, CCD variants, ..., 3DIT
  - ⋇ new ladder concepts: double-sided, unsupported, monolithic

    $\hookrightarrow$ to be assessed in FP-7 project AIDA

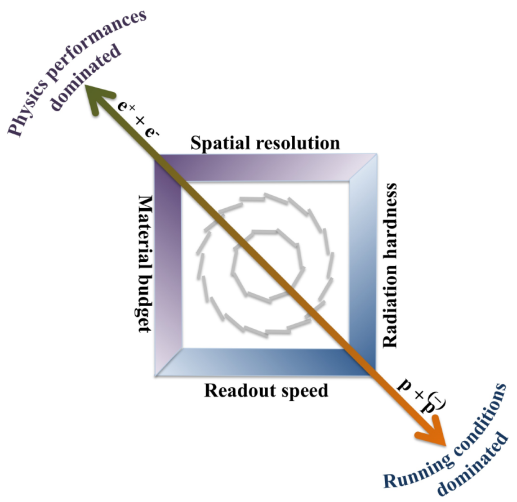
- **2 pixel techno. being prepared for vertex detectors of less demanding expts than those at ILC:**
  - ⋇ CMOS sensors: numerous BT, STAR ('12/13), CBM ('16), perspectives at CLIC, LHC, etc.
  - ⋇ DEPFETs: BELLE-2 ('14)

- **CMOS pixel sensors undergo a fast transition in radiation tolerance & speed:**
  - ⋇ 1st step: high res. epitaxy $\Rrightarrow$ SNR $\sim$ 40, rad. tol. $\rightarrowtail$ $\gtrsim$ O(10^{14})n_{eq}/cm^2
  - ⋇ important goal: combine thin HR sensitive tier with 2nd step:

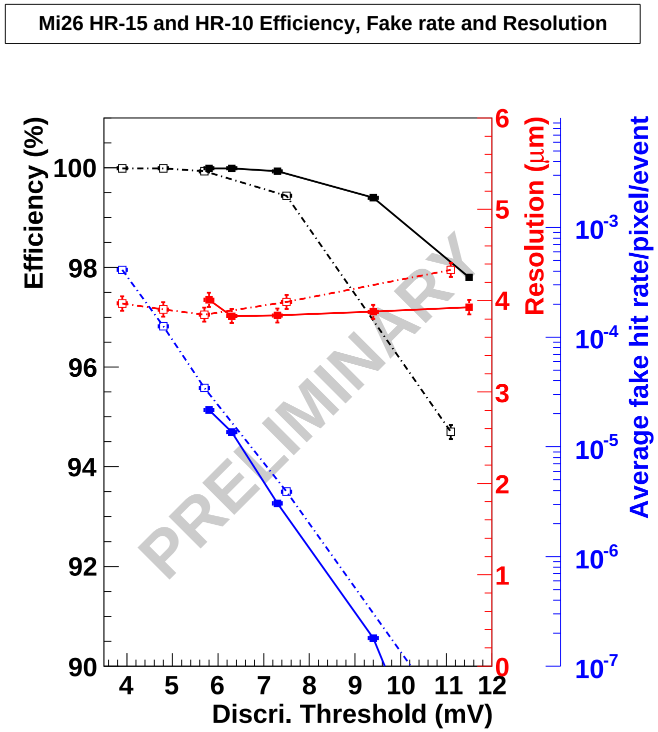
    CAIRN $\equiv$ 3D sensors combining high-res epitaxy with fast FEE $\rightarrowtail$ $\lesssim$ 10 ns

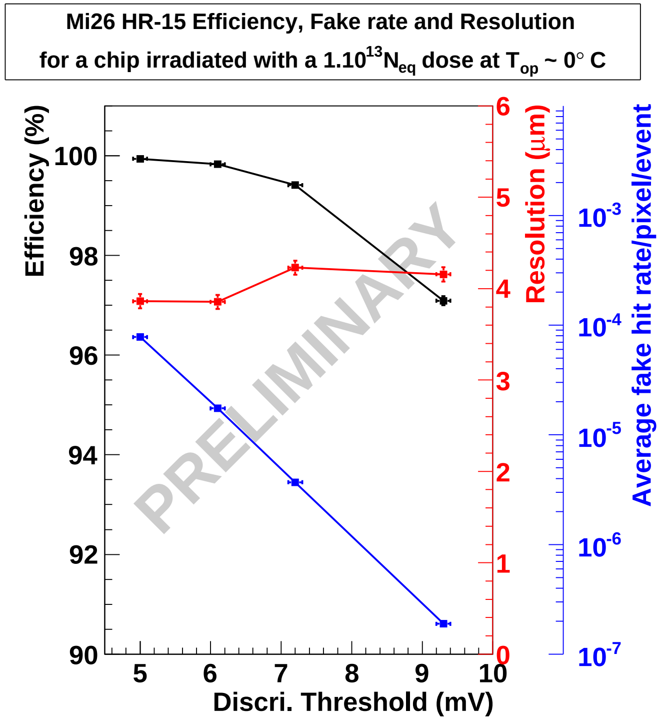
    $\hookrightarrow$ the vertex detector quadrature may be achievable ...

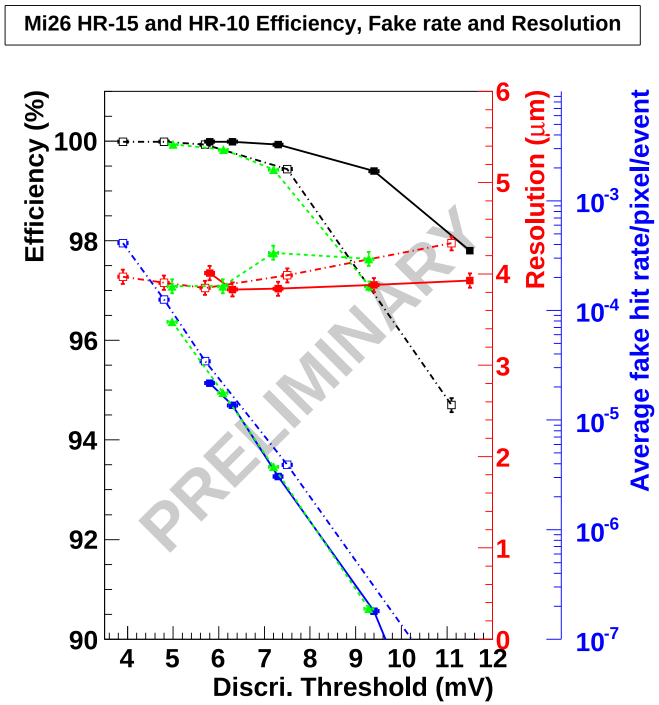
    $\hookrightarrow$ horizon opens up for CLIC & HL-LHC



▷▷▷ Impact of $1{\cdot}10^{13} n_{eq}/cm^2$ on detection performances at $T_{op} \sim 0^{\circ}C$





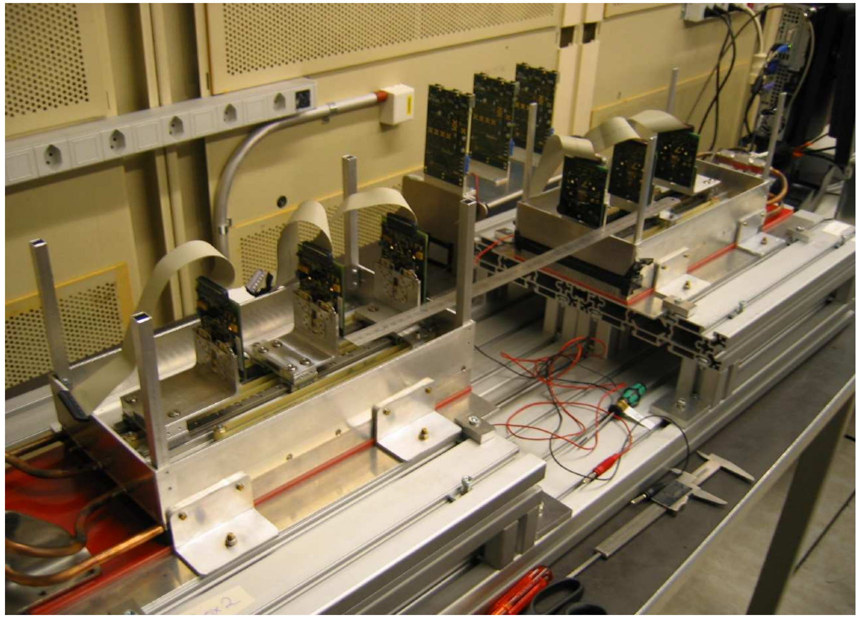


- **Preliminary conclusions:**
  - ⋇ det. eff. $\sim$ 100 % for very low fake rate: HR-15 ▷ plateau until fake rate of few 10^{-6}
  - ⋇ single point resolution $\lesssim 4\ \mu m$
  - ⋇ det.eff. of HR-15 still $\sim$ 100 % after exposure to $1{\cdot}10^{13} n_{eq}/cm^2$

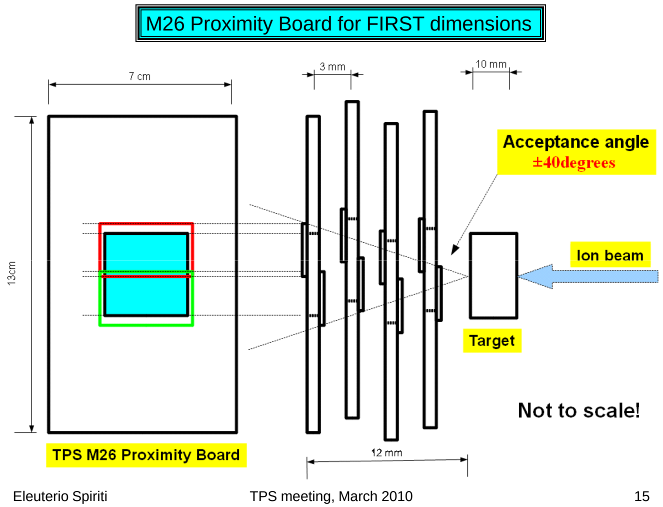
$\Rrightarrow$ **Striking evidence for performance improvment with HR epitaxy (in particular 15 μm thick)**

Back-Up : Direct Applications of EUDET Sensor

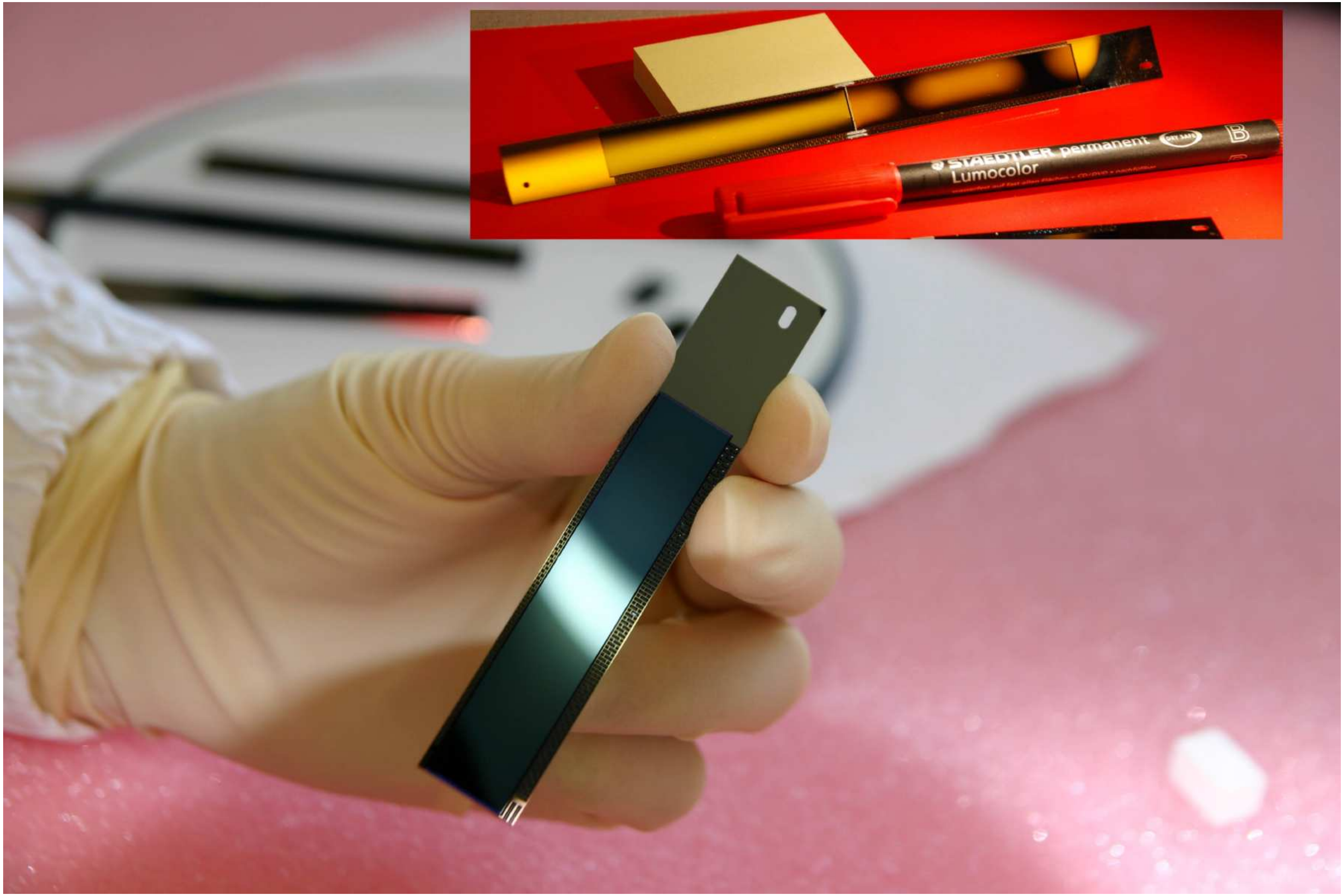
- **Beam telescope of the FP6 project EUDET**
  - 2 arms of 3 planes (plus 1-2 high resolution planes)
  - M-26 thinned to 50 μm
  - $\sigma_{extrapol.} \sim$ 1-2 μm EVEN with e^- (3 GeV, DESY)
  - frame read-out frequency O(10^4) Hz
  - running since '07 (demonstrator: analog outputs) at CERN-SPS & DESY (numerous users)



- **Spin-offs :**
  - **Several BT copies :** foreseen for detector R&D
  - BT for channelling studies
  - **CBM (FAIR) :** MVD demonstrator (2-sided layers) for CBM-MVD (HP-2 project)
  - **FIRST (GSI) :** VD for hadrontherapy x-sec. measts ▷▷▷



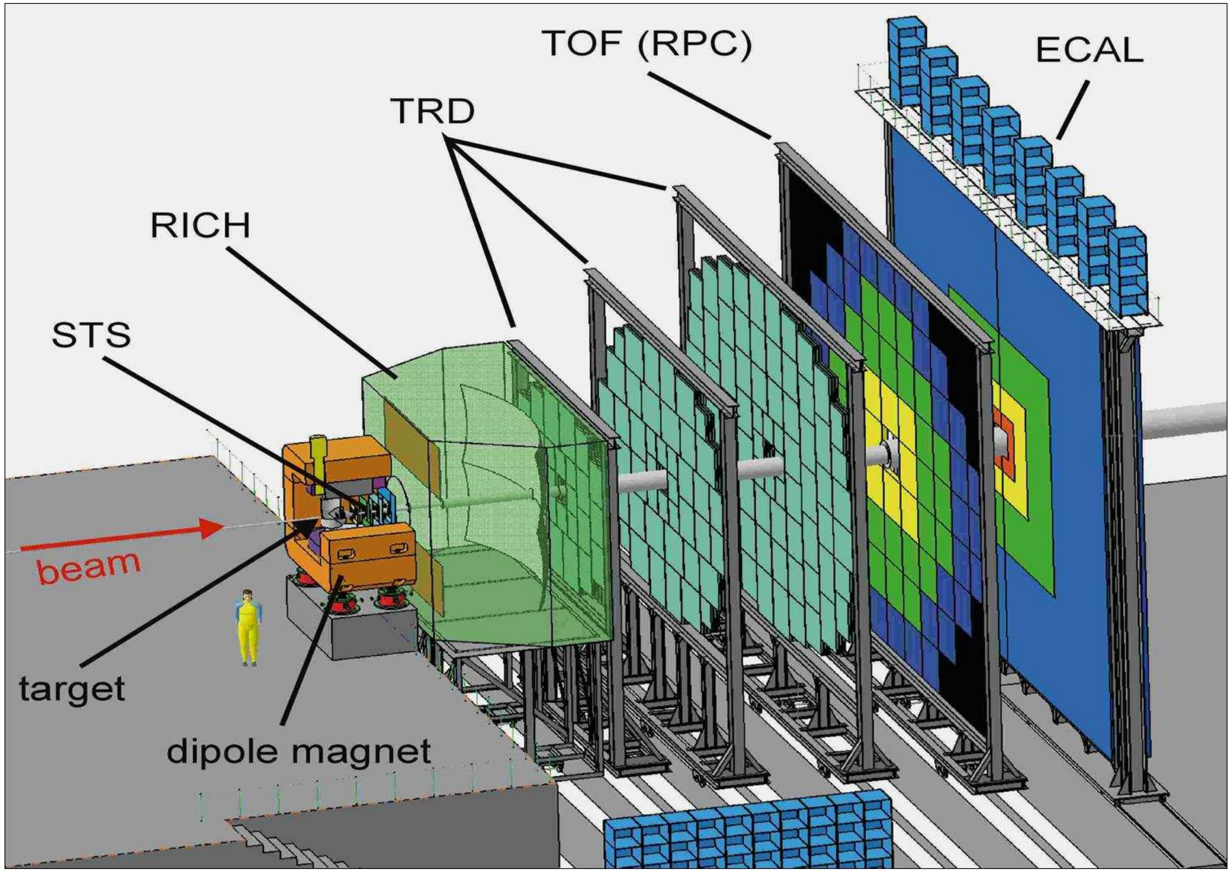
Back-Up : Application of DEPFET Sensors to BELLE-2 Experiment



Back-Up : Application of CMOS Sensors to CBM Experiment

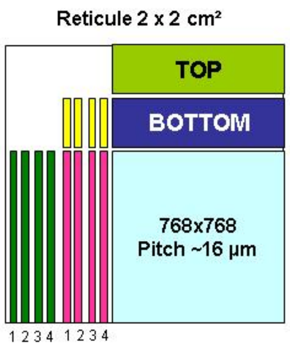
- **Cold Baryonic Matter (CBM) experiment at FAIR:**
  - ⋇ Micro-Vertex Detector (MVD) made of 2 of 3 stations located behind fixed target
  - ⋇ double-sided stations equipped with CMOS pixel sensors)
  - ⋇ operation a negative temperature in vacuum
  - ⋇ each station accounts for $\lesssim$ 0.5 % X_0
  - ⋇ sensor architecture close to ILC version

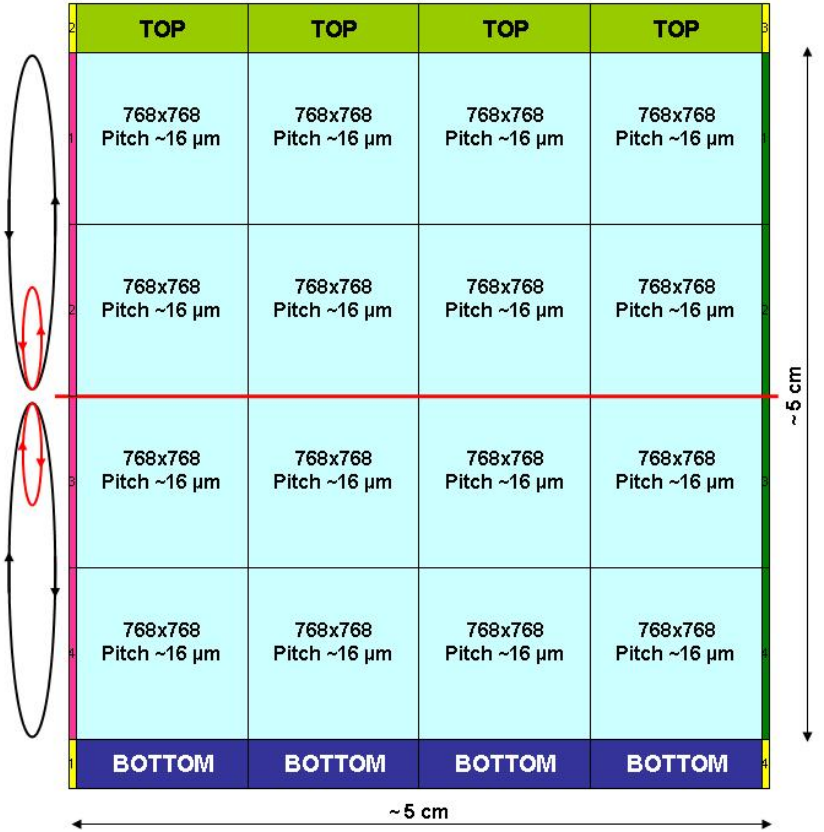
- **Most demanding requirements :**
  - ⋇ ultimately ($\sim$ 2020): 3D sensor
    $\lesssim$ 10 μs, $>$ $10^{14} n_{eq}/cm^2$, $\gtrsim$ 30 MRad
  - ⋇ intermediate steps: 2D sensors
    $\lesssim$ 30-40 μs, $>$ $10^{13} n_{eq}/cm^2$, $\gtrsim$ 3 MRad
  - ⋇ 1st sensor for SIS-100 (data taking $\sim$ 2016)



Back-Up : Investigating Large Area CMOS Sensors

- **Prototype multireticule sensor for large area stations:**
  - ⋇ *3072×3072 pixels (16 μm pitch)*
    - ⇛ *5×5 cm^2 sensitive area*
  - ⋇ *requires combining several reticules*
    - ⇛ *stitching process* ⇛ *establish proof of principle*
  - ⋇ *double-sided read-out of 1536 rows in 250–300 μs*
    - ⇛ *Large Area Telescope for AIDA project*
      (EU-FP7 approved recently)
  - ⋇ *windowing of $\lesssim$ 1×5 cm^2 (collim. beam)*
    - ⇛ *$\lesssim$ 50–60 μs r.o. time*

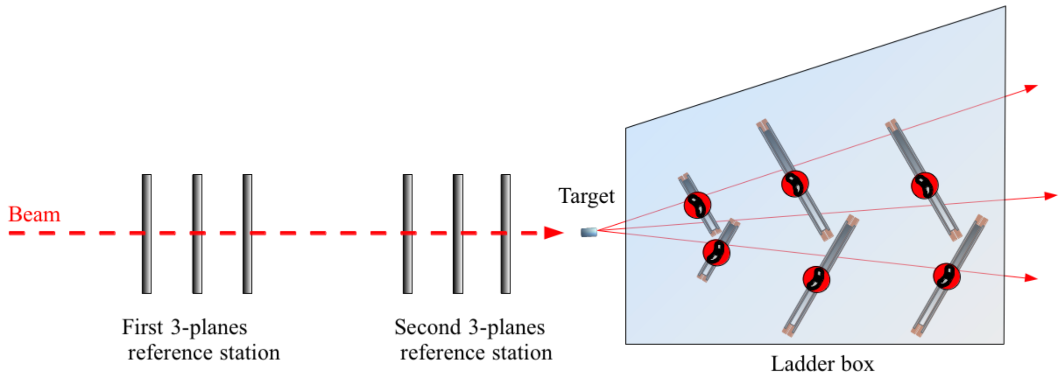


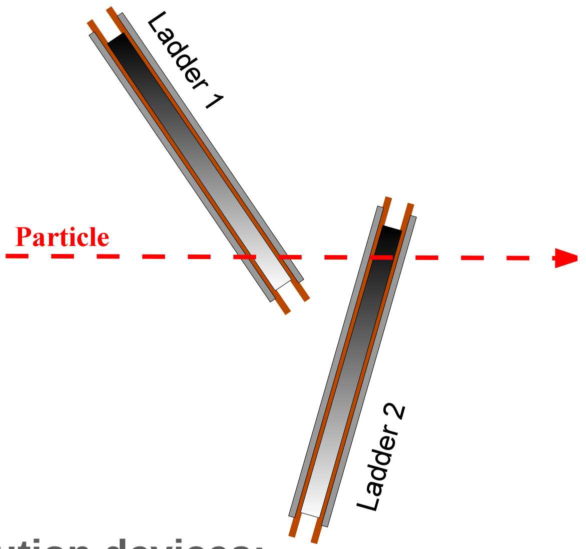


- **Submission expected end fo 2011 or early 2012:**
  - ⋇ bonus: avoid paving fw disks with reticule size sensors
    - ⇛ dead zones, material, connectics/complexity
  - ⋇ synergy with forward disk projects on collider experiments (e.g. EIC project at BNL)
  - ⋇ 6 sensors will compose a beam telescope at CERN (AIDA project deliverable)
    - ▷ few ns time stamping resolution associated to each hit by TLU (scintillator)

Back-Up: VTX Oriented Infrastructures in AIDA

- AIDA $\equiv$ EU FP-7 Integrated Infrastructure project : approved $\rightarrowtail$ starts Feb. 2011
- **On-beam (CERN-SPS) test infrastructure:**
  - ⋇ Large Area beam Telescope (LAT) $\rightarrowtail$ 5$\times$5 cm^2 stitched sensors
  - ⋇ Alignment Investigation Devices (AID):
    - ◇ box hosting pairs of ladders (e.g. PLUME) and unsupported pixelated systems (SERWIETE)
    - ◇ box front panel contains removable target



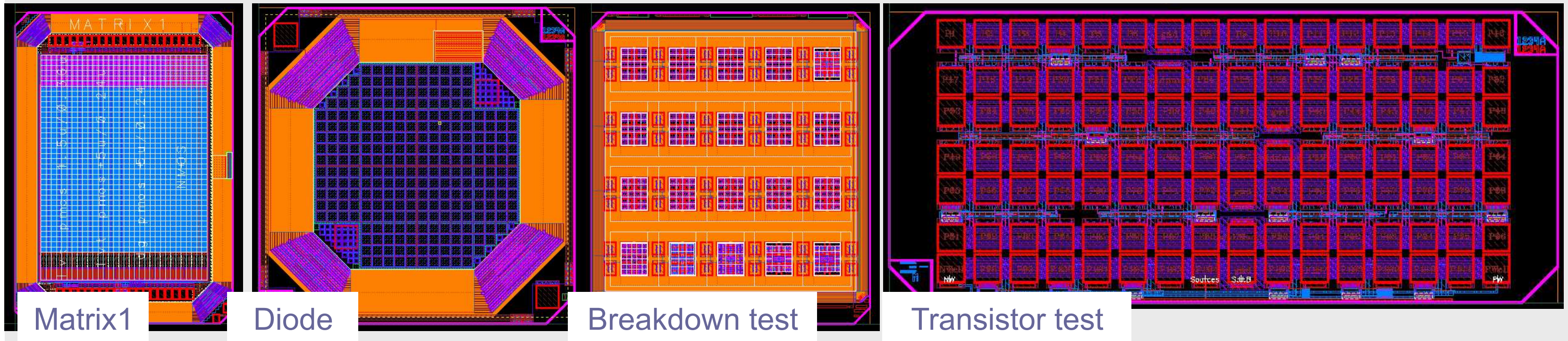


- **Work program topics ▷▷▷ relevant for numerous high resolution devices:**
  - ⋇ alignment capabilities: dedicated equipment and particle tracks
  - ⋇ vertex reconstruction accuracy
  - ⋇ track reconstruction with different devices (high spatial resolution combined with fast detectors)

Back-Up : Long-Term CMOS R&D with High-Resistivity Substrate

LePIX: monolithic detectors in advanced CMOS

- Submission for fabrication just finalized
  - Several issues: ESD, special layers and mask generation, guard rings
  - Still need to discuss some outstanding fabrication issues with IBM
- 7 chips submitted :
  - 4 test matrices
  - 1 diode for radiation tolerance
  - 1 breakdown test structure
  - 1 transistor test: already submitted once in test submission
- Will require very significant testing effort for which we need to prepare (measurement setup, test cards…)



W. Snoeys, CERN-ESE-ME, 2010