

35th International Conference on High Energy Physics Paris, 22-28 July 2010

Online tracking at colliders





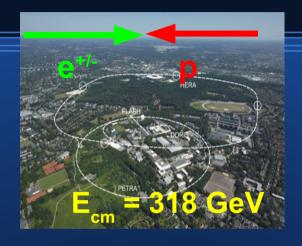
A good trigger system needs to combine **data reduction** with **sophisticated physics selection** to increase the purity of the collected sample.

Online tracking allows accurate reconstruction of crowded events (high luminosity --> pile-up) in time for a trigger decision:

- a calorimetric tower integrates energy from all the particles in the event --> it cannot distinguish between hard scattering and pile-up
- online tracking can distinguish particles based on their z and p_T

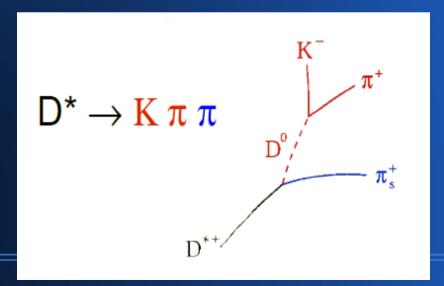
Online tracking is challenging!

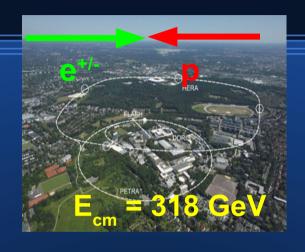
- Time constraints: track reconstruction in few μs at L1, ~ tens of μs at L2
- High number of readout channels
- High occupancy --> large combinatorics



 $L = 2 \cdot 10^{31} \text{ cm}^{-2} \text{s}^{-1}$

Fast Track Trigger (FTT, 2004-2007)



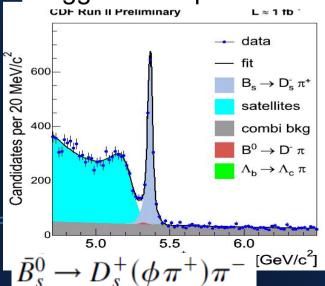


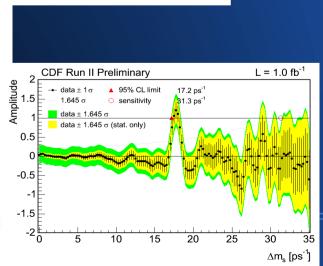
 $L = 3 \cdot 10^{32} \, \text{cm}^{-2} \, \text{s}^{-1} \, \text{intle}$

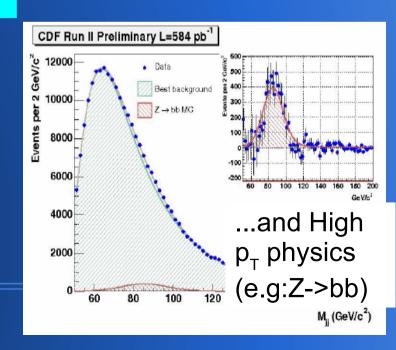
Silicon Vertex Tracker (SVT)

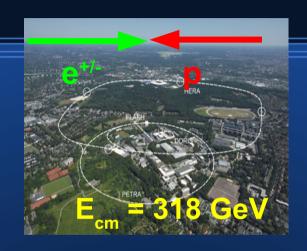
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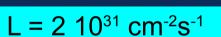
Trigger on displaced tracks for B

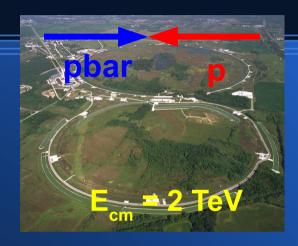






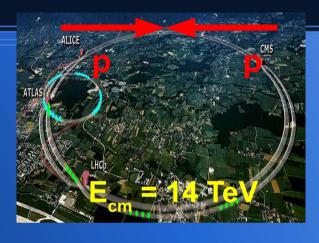




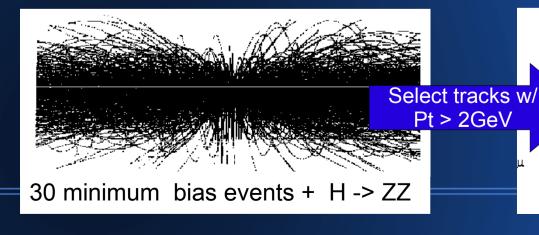


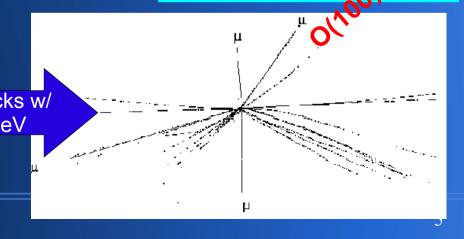
L = 3 10³² cm⁻² s⁻¹

ATLAS and CMS proposals for SLHC 5

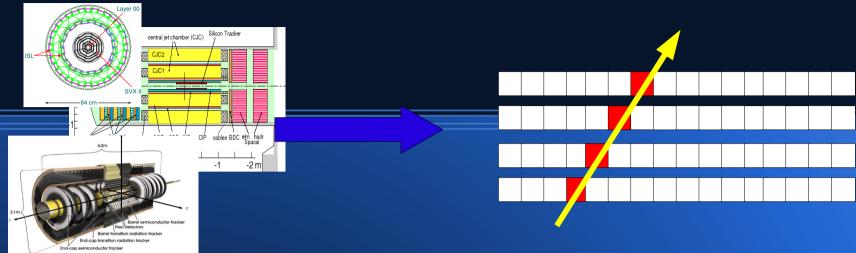


LHC: 10³⁴ cm⁻² s⁻¹
SLHC: 3 10³⁴ cm⁻² s⁻¹
10³⁵ cm⁻² s^Q



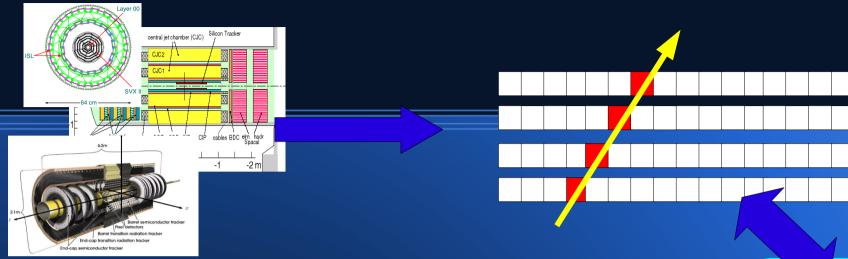


Track identification: Pattern Matching



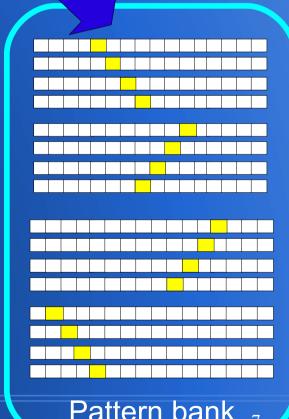
- Tracking detectors = layers segmented into bins
- Each charged particle generates a hit pattern

Track identification: Pattern Matching

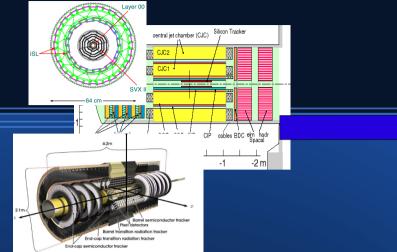


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- All possible hit patterns stored in memory (pattern bank)
- Hit pattern matching a precomputed pattern =

Candidate Track



Track identification: Pattern Matching

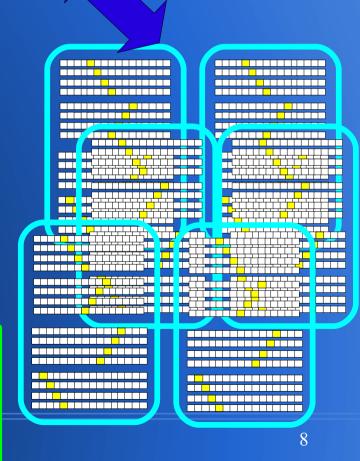




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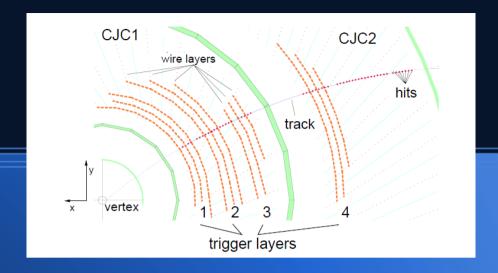
Candidate Track

High degree of parallelism (Associative Memory or commercial Content Addressable Memories) to increase speed.



The Fast Track Trigger @ H1

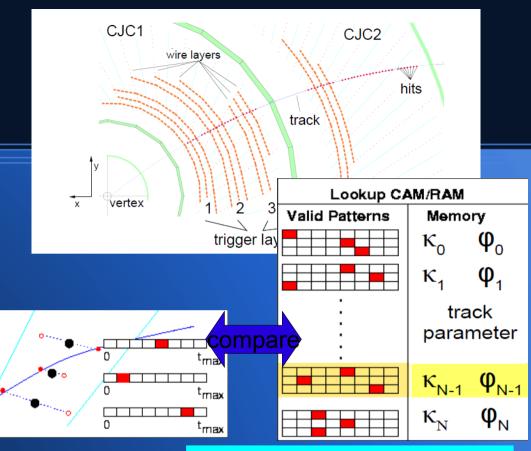
L1 bandwidth is limited → use only a subsample (12/56) of the drift chamber layers



The Fast Track Trigger @ H1

L1 bandwidth is limited → use only a subsample (12/56) of the drift chamber layers

- L1: Find track segments and link them into tracks.
- L2: Repeat linking step at full resolution,3D fit
- L3: reconstruct complex objects (invariant masses, jets)



CAMs in high density FPGA (Altera)
Working frequency 100 MHz

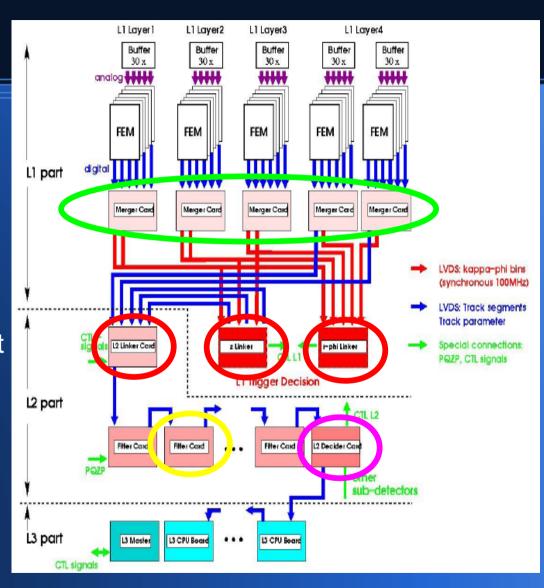
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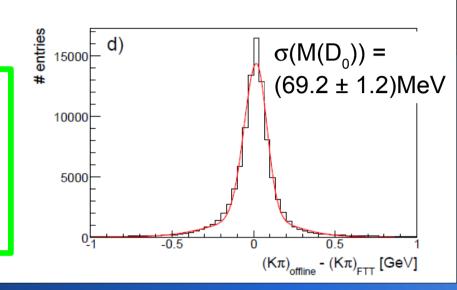
Based on a single flexible, multipurpose board (MultiFunctional Processing Board) that can

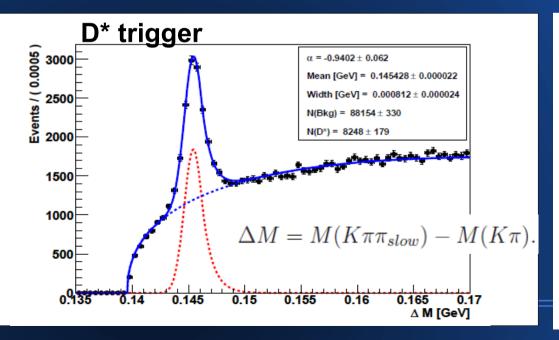
- Merge data streams
- Link track segments at L1 and L2
- Fit tracks at L2
- Make L2 decision

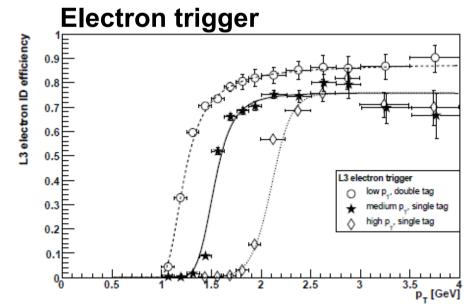


FTT performance

- Fit up to 48 tracks per event w/ pt > 100 MeV
- Resolutions:
 - 1/p_t → 2.2%/GeV
 - $\vartheta \rightarrow 50 \text{ mrad}$
 - $\phi \rightarrow 2.5 \text{ mrad}$







The Silicon Vertex Tracker @ CDF

1) HIGHLY PARALLEL

2) PATTERN RECOGNITION w/ custom VLSI Associative Memory

ARCHITECTURE



Hit finder Detector Data

Hits

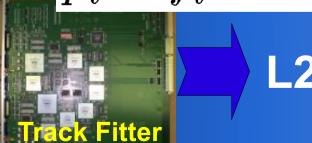


Hit buffer



3) LINEARIZED FIT in fast **FPGA**

$$p_i = \vec{f}_i \cdot \vec{x} + q_i$$



- Latency ~ 20 μs
- eff $\sim 80\%$ ($p_{\tau} > 2$ GeV, $d_{0} < 1$ mm)
- $\sigma_{d0} \sim 35 \mu m$
- $\sigma_{nT} \sim 0.003 \text{ pt}^2$
- $\sigma_{a} \sim 1 \text{ mrad}$

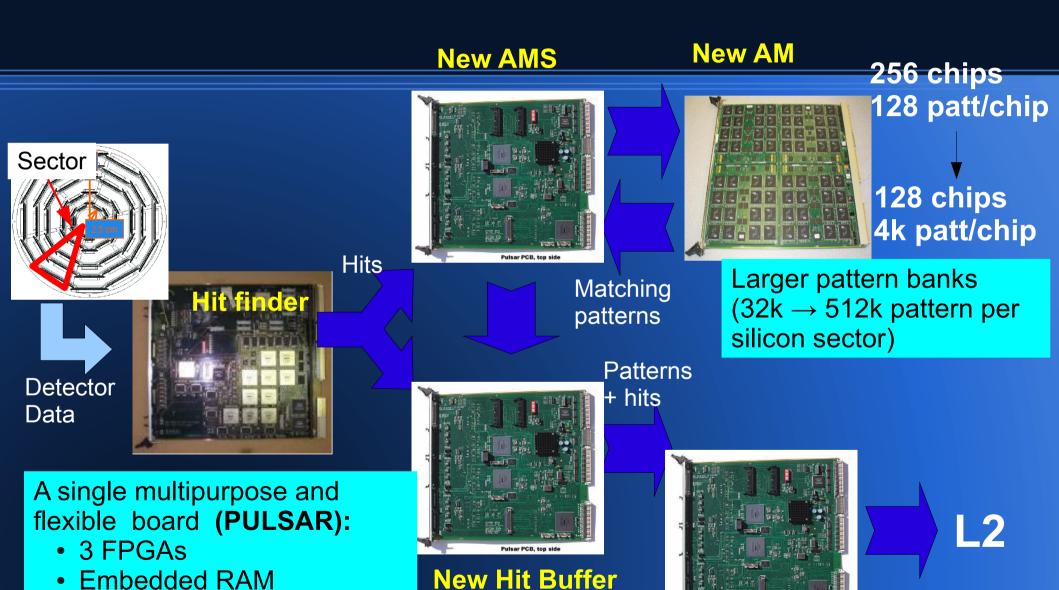


SVT (2006)

Interface w/ any user data

cards

through custom mezzanine

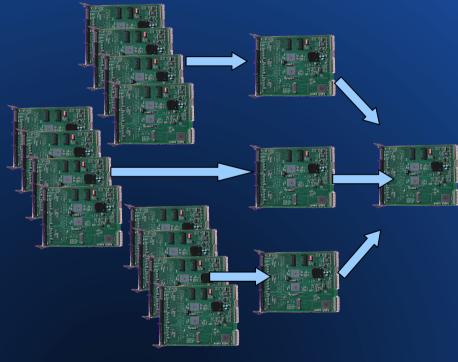


New Track Fitter

14

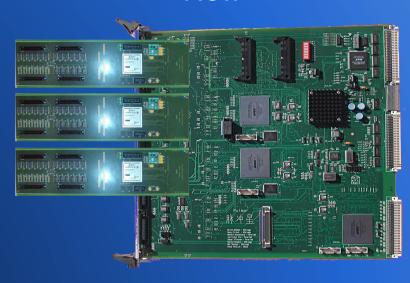
SVT (2010): the Gigafitter upgrade

Old Track Fitter system



16 boards

New



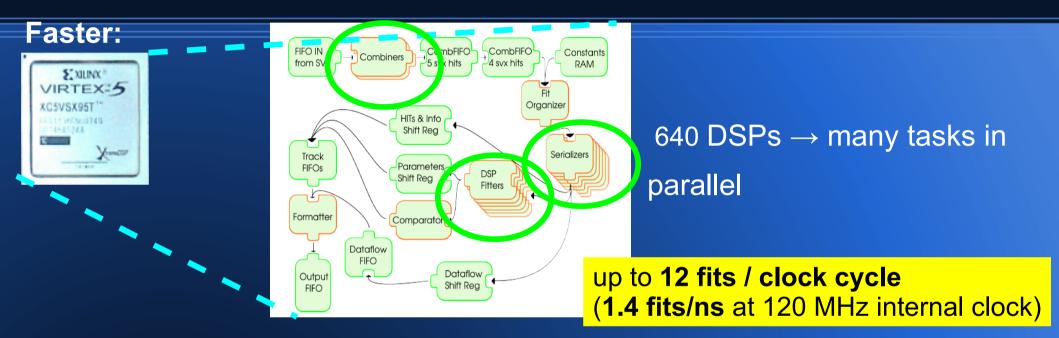
1 Pulsar board + 3 Mezzanine cards equipped with

Xilinx Virtex-5 FPGA with

• 640 DSP (25 x 18 bit multiplier + 48 bit adder)

• 8.2 Mb Ram

The Gigafitter: advantages over the old system



More available memory:

Extension of the SVT acceptance in track Pt and impact parameter d

 $d < 1.5 \text{ mm} \rightarrow d < 2-3 \text{ mm}$

Pt > 2 GeV → Pt > 1.5 GeV

Improvement in b-tagging capabilities and lifetime measurements

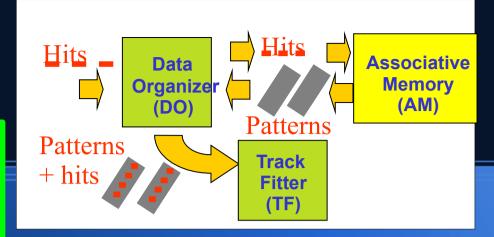
Fast TracKer (FTK) @ Atlas

Goal: reconstruct offline-like tracks in

time for **L2 decision** @ 100 kHz (L1 rate).

How: adapt SVT (+GF) experience

to Atlas



	SVT	FTK
L1 output rate	30 kHz	100 kHz
Detector layers	5	11 (3 pixel+8 SCT)
# patterns	6M	>800M

Fast TracKer (FTK) @ Atlas

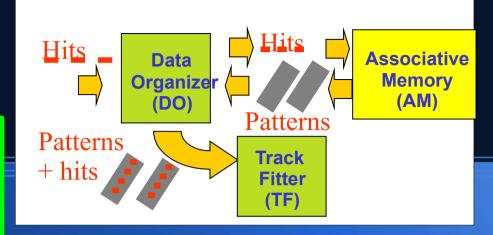
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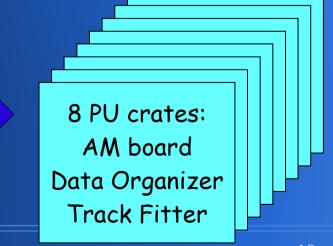
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Processor Unit





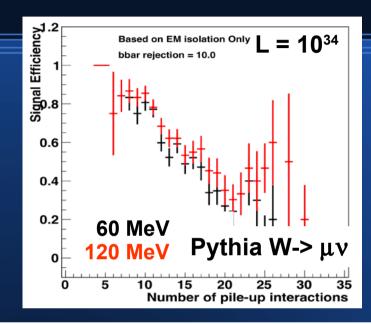
FTK expected performances

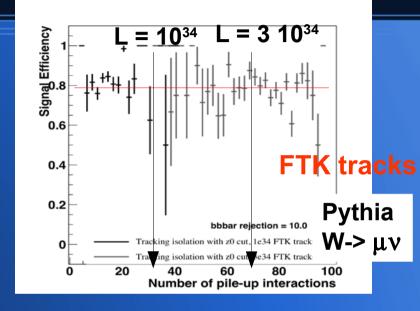
LIGHT JET IMPACT PARAMETER

EM calorimeter isolation only

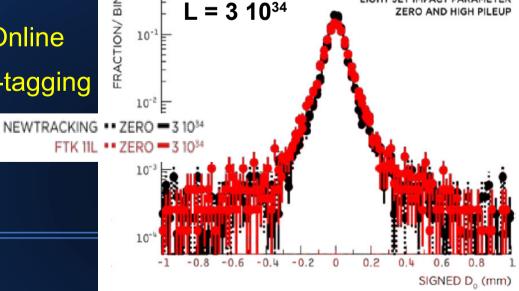
Track isolation (w/ z₀ cut)

Isolated muon triggers

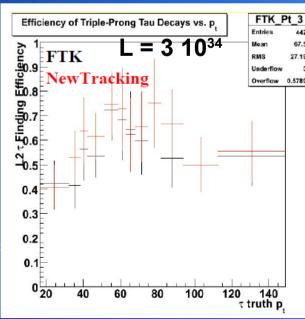




Online b-tagging



Online tau reconstruction



CMS tracking @ L1

LHC

LHC

- Calorimeters
- Muon detectors

100 MHz, 4 µs

High level Trigger
(HLT)
- Offline-like objects

100 Hz, 40 ms

SLHC new tracker & new L1 track trigger

Main challenge is data volume: data rates ~ 10-20Gb cm⁻²s⁻¹ to read out a silicon detector layer at 10 cm! *On-detector data reduction* is needed.

CMS tracking @ L1

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100 MHz, 4 μs

High level Trigger (HLT)

• Offline-like objects

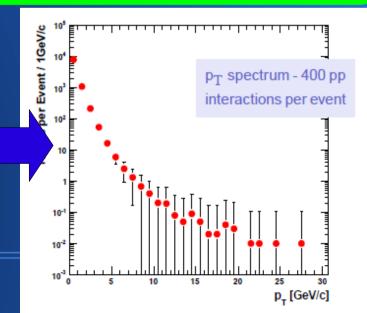
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SLHC

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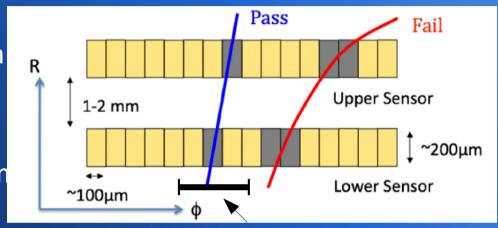
Possible solution: use for L1 decision only tracks with Pt > 1 GeV/c, reject low momentum ones.



CMS tracking @ L1: possible solutions

STACKED TRACKING

- Correlate hits between closely separated sensors using a simple matching algorithm
- High Pt tracks = hits within a specific search window.
- With multiple sensors pairs, matched hits from different pairs can be correlated to forn raw tracks.

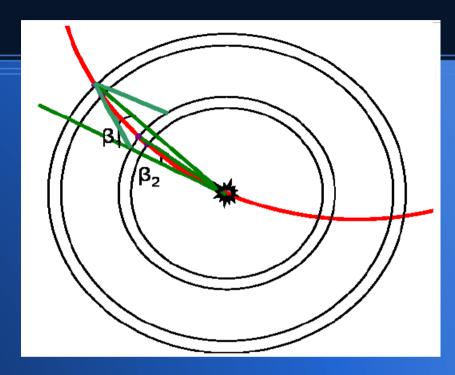


Search window

CMS tracking @ L1: possible solutions

STACKED TRACKING

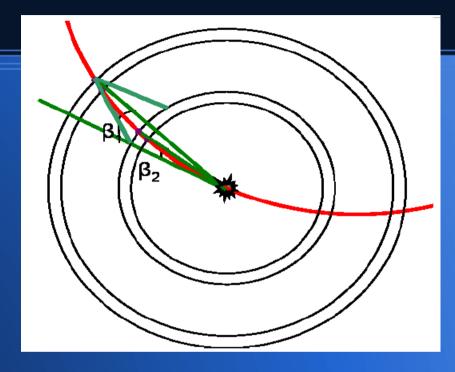
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CMS tracking @ L1: possible solutions

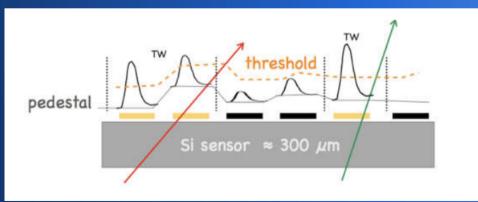
STACKED TRACKING

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- High Pt tracks = hits within a specific search window.
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CLUSTER WIDTH DISCRIMINATION

- Four strip sensor layers at radii 25-50 cm.
- Cut on cluster width to reduce data rate.
- Correlate clusters from 3 out 4 layers using CAM or FPGAs



Conclusions

A good online tracking system is important to increase the physics reach of experiments at hadron colliders.

What do we learn from the past (H1) and the present (CDF)?

The online tracking system has to be

- FAST and EFFICIENT → data reduction, pattern recognition, parallelism, high density FPGAs
- FLEXIBLE, to be easily adapted to different luminosity conditions → multipurpose boards.

Both CMS and ATLAS are facing the challenge: R&D activity ongoing for SLHC.

References

FTT

- A. Baird et al, A Fast High Resolution Track Trigger for the H1 Experiment, arXiv:hep-ex/0104010v1
- D. Meer et al, A Multifunctional Processing Board for the Fast Track Trigger of the H1 experiment, arXiv:hep-ex/0107010v1
- A.W.Jung et al, First Results from the Third Level of the H1 Fast Track Trigger, Proceedings of 15th IEEE-NPSS Real Time Conference (2007)

SVT

- M.Dell'Orso, L.Ristori, VLSI Structures for Track Finding, NIM A278 (1998) 436-440
- J.Adelman et al., The Silicon Vertex Trigger Upgrade at CDF, NIM A572 (2007) 361
- S.Amerio et al., The Gigafitter: Performance at CDF and Perspectives for Future Applications, 2010 J.Phys.: Conf.Ser. 219 022001

FTK

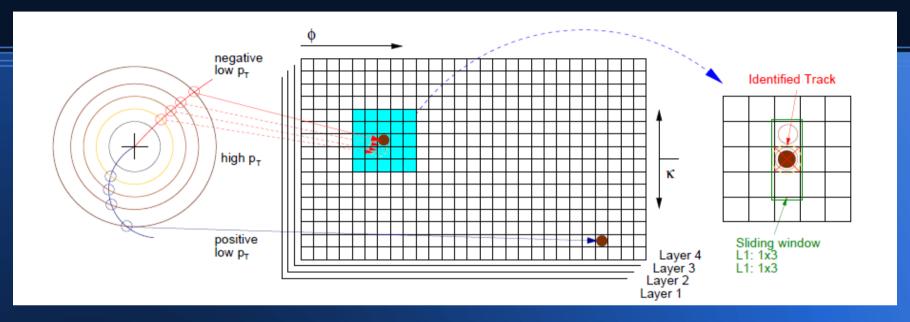
- A.Annovi et al., Associative memory design for the Fast Track Processor (FTK) at Atlas
- A.Andreani et al., The FastTrack Real Time Processor and Its Impact on Muon Isolation, Tau and b-jet Online Selections at ATLAS, both in Proceedings of 17th IEEE NPSS Real Time Conference, Lisbon, Portugal, 24-28 May 2010

CMS

- G.Hall, Design of a trigger module for the CMS tracker at SLHC, Proceedings of TWEPP-09
- F. Palla, Proposal for a First Level Trigger using Pixel Detector for CMS at Super-LHC, 2007 JINST 2 P02002
- J. Jones et al, A Pixel Detector for Level-1 Triggering at SLHC, arXiv:physics/0510228 26

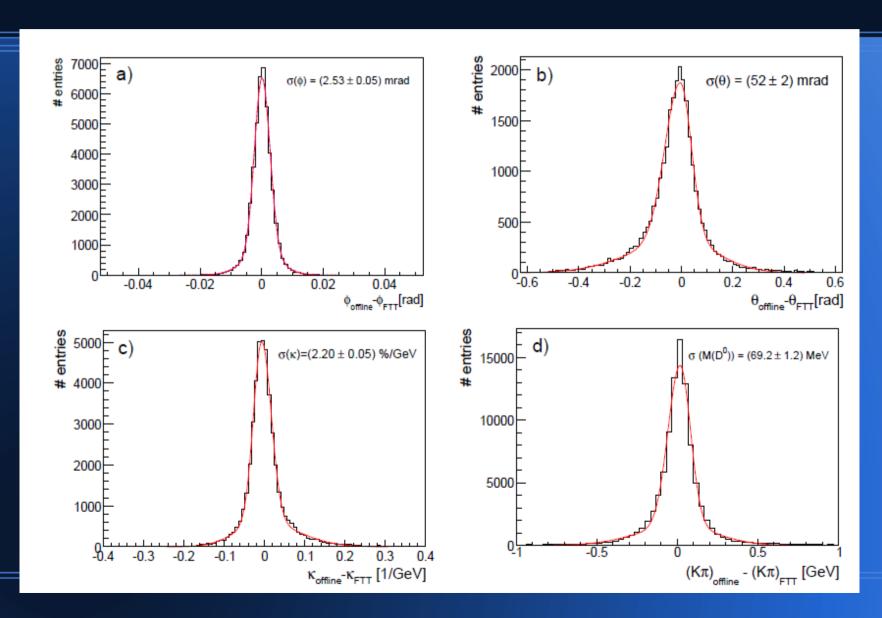
BACKUP

FTT track linking and fit

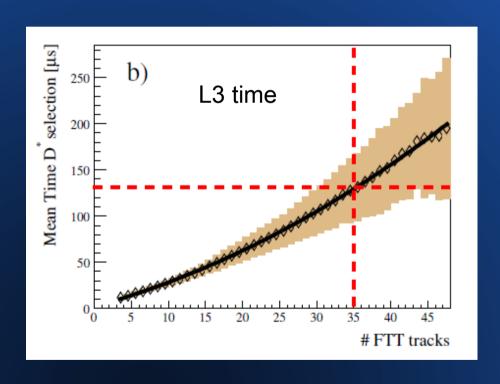


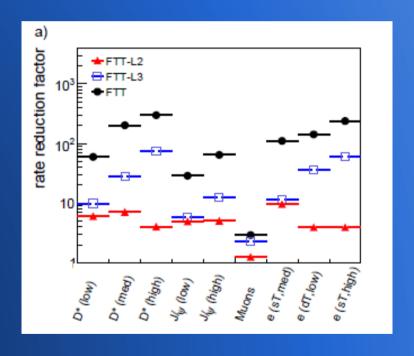
- Track segments from the 4 trigger layers are filled into four corresponding k-phi histograms (size 16 x 60 @ L1, 60 x 640 @ L2).
- A sliding window technique is used to link track segments to tracks: coincidence of at least 2 out of 4 trigger layers.
- @ L2 the track is fitted. A primary vertex constraint is applied. Each DSP performs up to 2 track fits.

FTT L2 track resolution



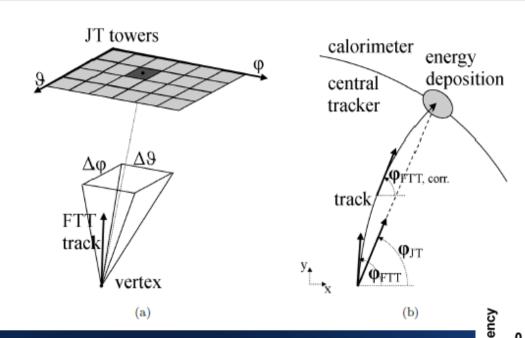
FTT timing and reduction rate

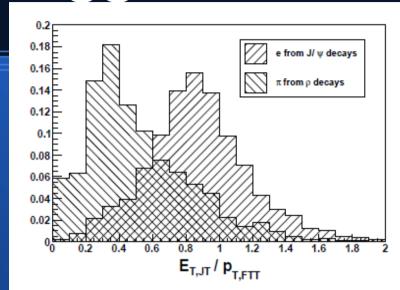


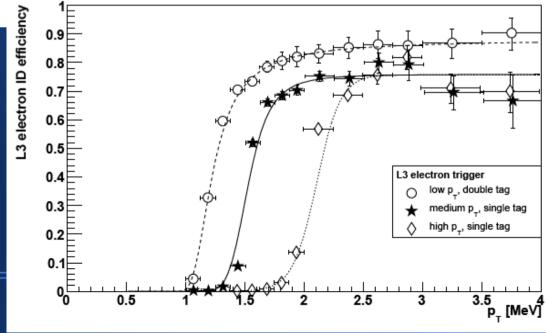


Rate reduction factors

FTT electron trigger







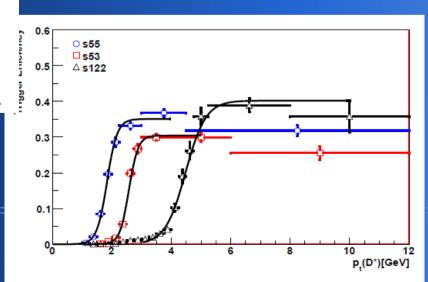
D* reconstruction @ H1

Subtrigger	triggerelement	definition
	level 1	
s55, s53, s122	cipmul>4 & cipsig>2 & FTT_mul_Ta>5 & FTT_mul_Tc>2 & FTT_mul_Td>1 & FTT_mul_Te>0	N(ctr) + N(bwd) + N(fwd) > 10 $N(ctr) > 2 \cdot (N(bwd) + N(fwd))$ $\# tracks > 5$, with $p_t > 100 MeV$ $\# tracks > 2$, with $p_t > 400 MeV$ $\# tracks > 1$, with $p_t > 900 MeV$ $\# tracks > 0$, with $p_t > 1.8 GeV$
	level 2	
s55	& FTT_Et_1 & FTT_mul_Te>1 & FTT_zVtx>2	total transverse energy $> 5.0 \text{GeV}$ #tracks > 1 , with $p_t > 900 \text{MeV}$
s53	& FTT_Et_2 & FTT_mul_Te>1 & FTT_zVtx>2	total transverse energy $> 6.5 \text{GeV}$ #tracks > 1 , with $p_t > 900 \text{MeV}$
s122	& FTT_zVtx>2 & FTT_mul_Te>1 & FTT_zVtx>2	#tracks > 1, with $p_t > 900 \text{MeV}$
	level 3	
s55 s53 s122	& low_pt_D*_untagged & medium_pt_D*_untagged & high_pt_D*_untagged	$p_t(D^*) > 1.5 \text{ GeV with } \Delta M \le 180 \text{ MeV}$ $p_t(D^*) > 2.5 \text{ GeV with } \Delta M \le 180 \text{ MeV}$ $p_t(D^*) > 4.5 \text{ GeV with } \Delta M \le 280 \text{ MeV}$

• Trigger efficiency vs D* pt for 3 different triggers (low, medium and high transverse momenta)

@L3:

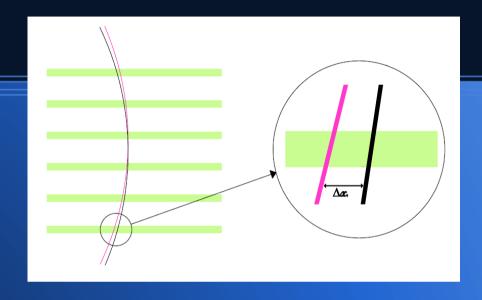
- 2 tracks with mass consistent with D0 meson mass
- 3^{rd} track corresponding to π + mass
- Mass difference (around 145 MeV)

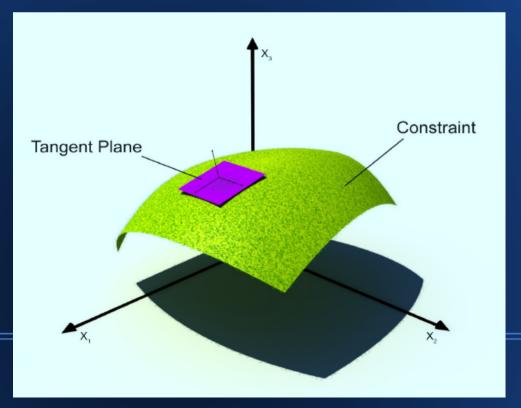


SVT – Track Fitter

Non linear geometrical constraint for a circle \rightarrow F(x1, x2, ...) = 0

For small displacements \rightarrow F(x1, x2, ...) \sim a0 + a1 Δ x1 + a2 Δ x2... (ai = constant)



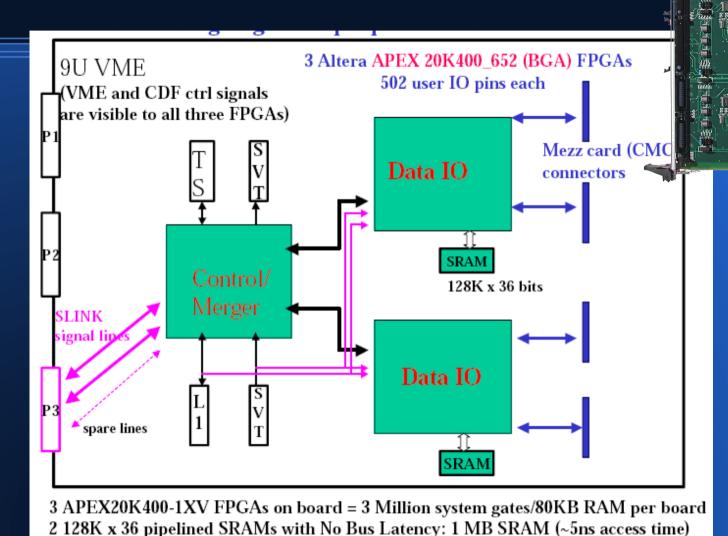


6 coordinates (4 SVX hits + Pt and Phi from XFT) – 3 parameters to fit → 3 constraints that can be locally linearized

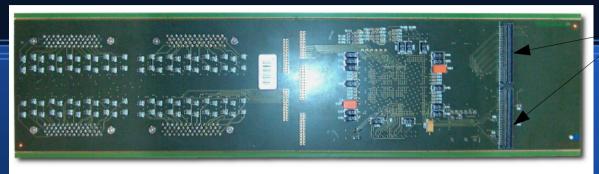
Track parameters
$$\rightarrow$$
 p \sim c₀ + $\Sigma_{i=1,6}$ c_i x_i

A single set on constants c_i is good for a whole detector wedge (30° in ϕ)

The Pulsar board

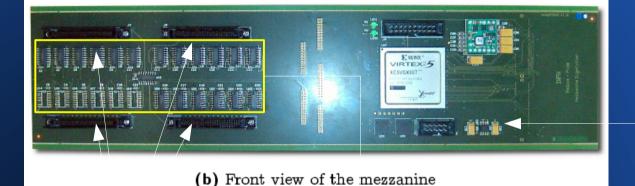


The GF mezzanine



Interface with the Pulsar based on 2 64 pins PMC IEEE 1386 connectors

(a) Back view of the mezzanine

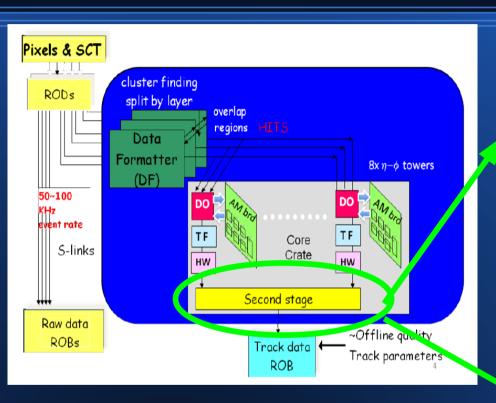


EEPROM to program the FPGA at every startup

Connectors (52 pins KEL_8830E-052-170S) to receive the SVX+XFT inputs

24 receivers and 1 driver to allow the▶ translation from LVDS to TTL signals

FTK architecture

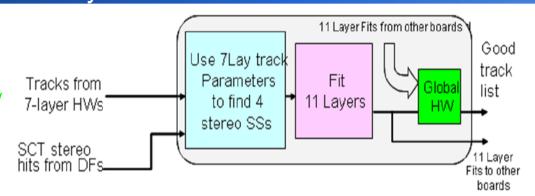


Pattern matching and track fitting with 11 layers not feasible at high lumi (3 10³⁴cm⁻²s⁻¹): AM size and # of fits increase rapidly with the number of layers.

Need to divide the track reconstruction in 2 stages.

Option A:

- Pattern matching w/ 3 pixel + 4 SCT axial layers.
- Chi2 cut --> extrapolation into the SCT stereo layers
- 11-layers fit

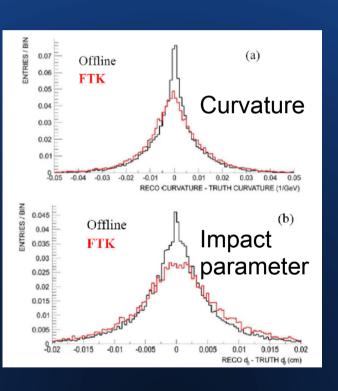


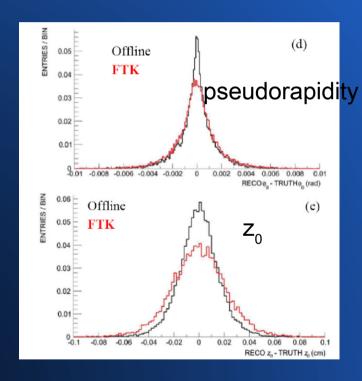
Option B:

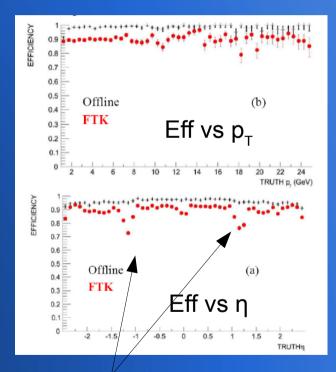
- Pattern matching w/ 8 SCT layers
- Chi2 cut --> track = "pseudohit"
- 4 layers AM (pseudohit + 3 pixel layers)
- 11-layers fit

FTK expected performances (I)

Single track efficiency and resolution





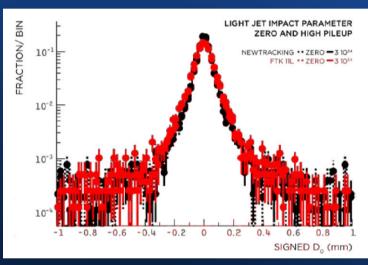


Single muon events, no pile-up FTK settings to be used at high lumi.

Drop in efficiency between barrel and forward regions

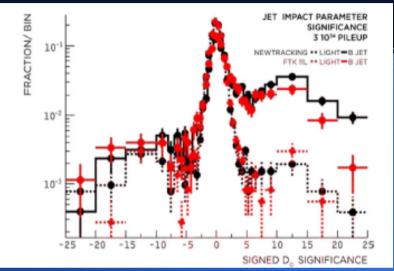
FTK expected performances (II)

B-tagging

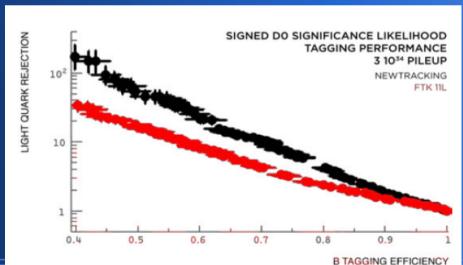


Impact parameter for tracks in light quark jets.

WH sample (M_H = 120 GeV, H->bb/uu) Offline cuts for very high lum: Nhits \geq 9, Npixel holes = 0, NSCT holes \leq 2, $|d_0| < 1$ mm, $|z_0| < 15$ cm)



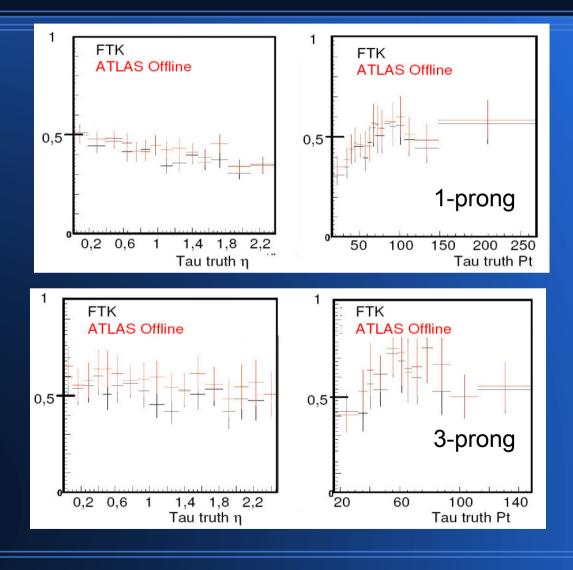
Impact parameter significance for b- and light jets.



Light quark rejection vs b-tagging efficiency

FTK expected performances (III)

Tau reconstruction



CMS stacked tracker module

Pixel size = 100 µm x 2.5 mm 1 module = 256 rows x 32 columns Active sensor size = 25.6 mm x 80 mm = 8192 pixels

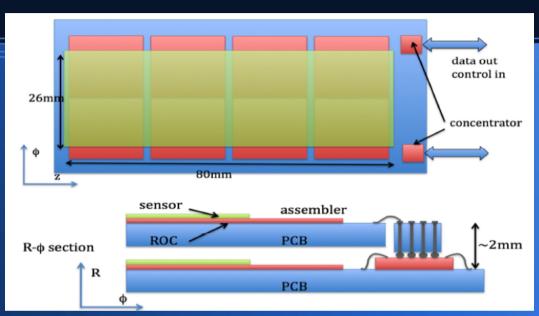
Sensors thickness = $200 \mu m$

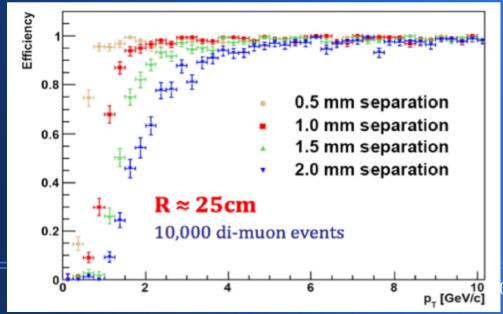
Read out from a column of 128 pixels

Readout Asic = 128 channel front- end element + assembler where comparison of patterns between the two layers are made.

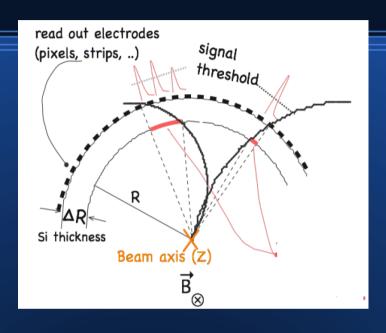
High speed radiation hard bidirectional optical links

Power consumption: 250 μW/channel, 10 kW for 40M pixels at 25 cm radius





CMS L1 tracker based on cluster width discrimination



4 layers between R = 25 cm and R = 50 cm

Hybrid pixel modules equipped with radiation hard fibers

Independent engines working on different azimuthal sectors

Each engine receives hits from each layer and produces track candidates using Associative Memory.

25kpatterns per engine for tracks with Pt > 5 GeV/c

To sustain data flux from the detector, 40 AM chips per engine working in parallel on 40 events at the same time.

160 boards with 40 AM chips (new generation) each.