ATLAS Upgrade for the sLHC: meeting the challenges of a five-fold increase in collision rate

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For the ATLAS Collaboration

Outline

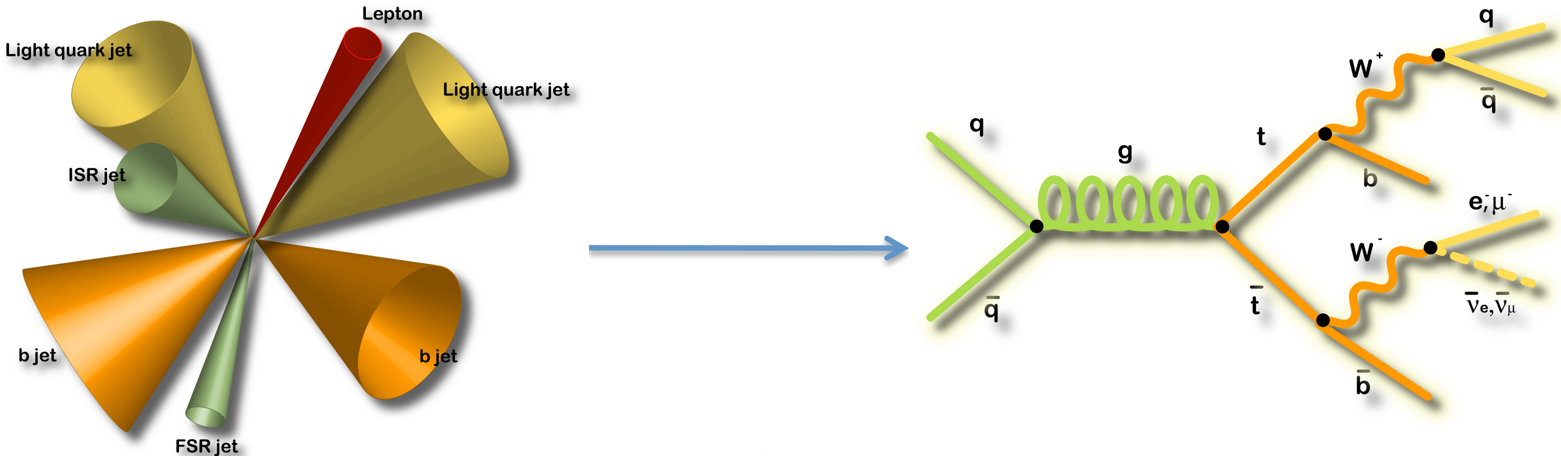
- Motivation
- Schedule
  - Phase 0
  - Phase I
  - Phase II
- Summary

Disclaimer:

- *This talk is intended to be mostly illustrative: don't have time to go into details*
- *I will omit far more than I can include*

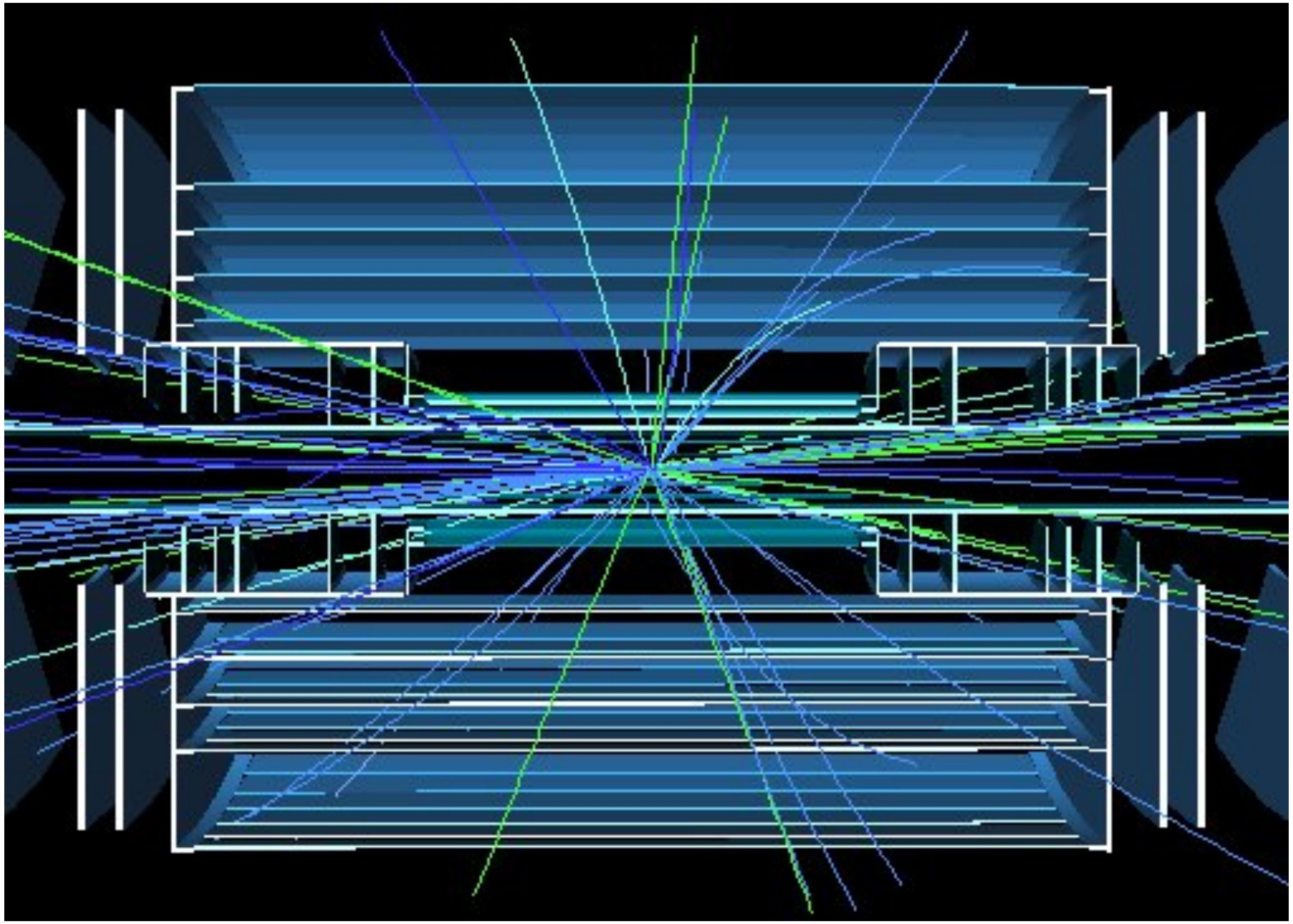
Motivation

- At the sLHC conditions one need to cope with
  - The pile-up / increased intensities and hence higher event rates
    - ⇒ Faster electronics
    - ⇒ Higher granularity subdetectors
    - ⇒ Reduce non-collision backgrounds
  - Radiation damage
    - => radiation hard components
- Physics-wise: precision measurements and extend/continue searches (add your favorite topic)
- "The goal is to achieve the same performance (resolution etc.) at the sLHC as at the LHC, despite the large increase in event rate" (ATLAS Upgrade CERN page)



Motivation

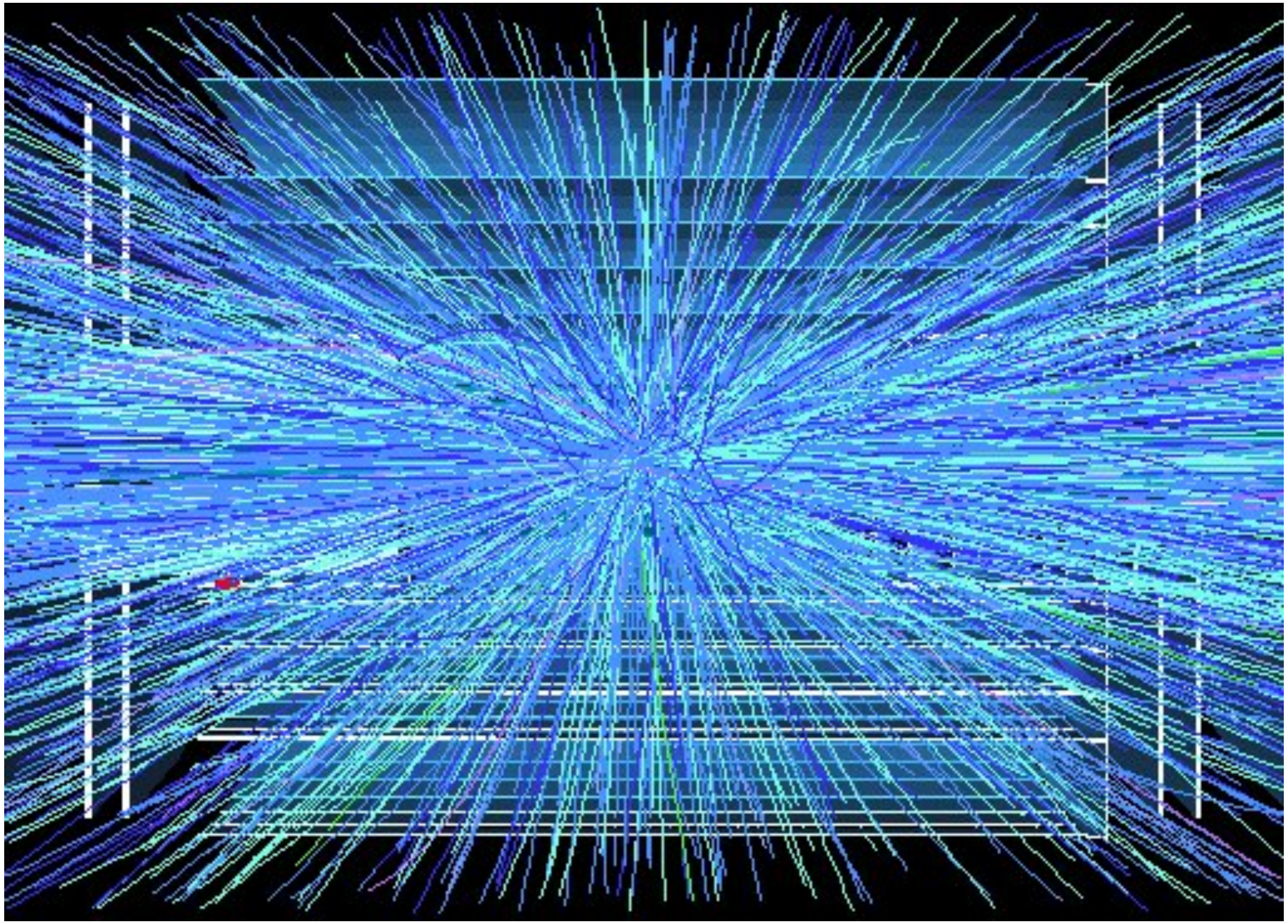
0.2×10^{34} cm^{-2}s^{-1}



Plots from Abdel Abdesselam, June 2010

Motivation

$10 \times 10^{34}\ cm^{-2}s^{-1}$



Plots from Abdel Abdesselam, June 2010

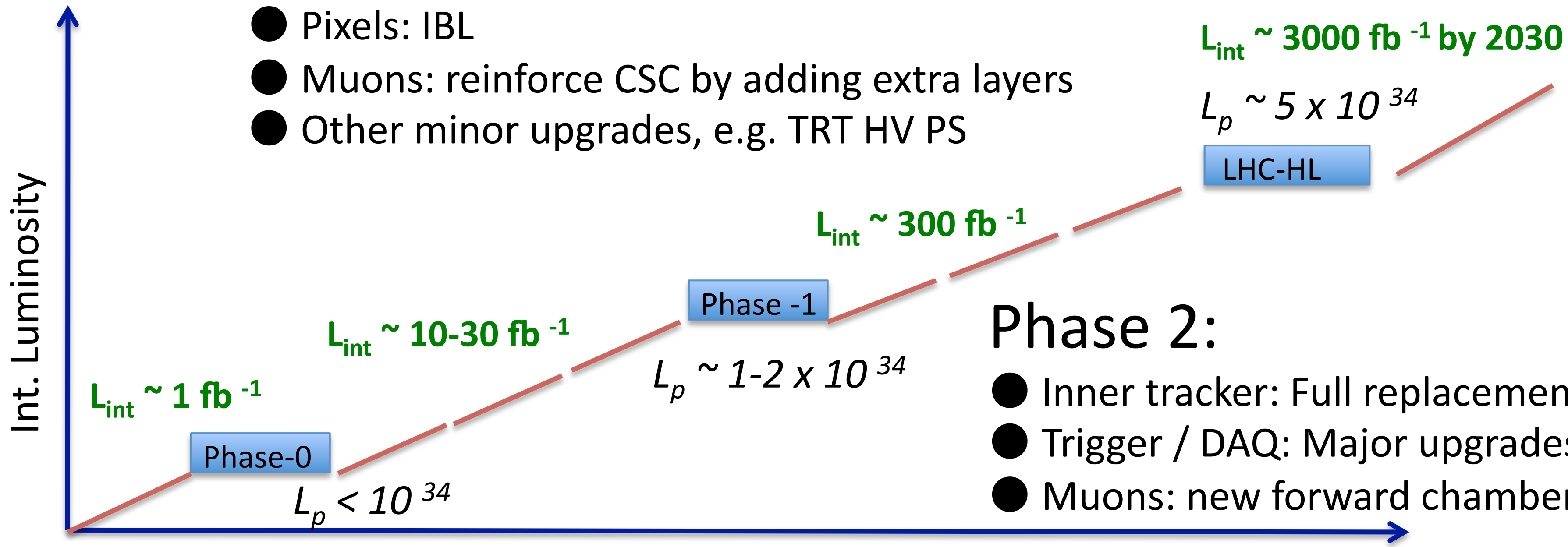
Schedule

Milestone	Date
Straw Man & options fixed	Dec 2006
R&D towards inner detector conceptual design	2007-2011
LoI	Dec 2010
LHC Shutdown to go to 14 TeV	2012
Technical Proposal, Initial MoU and Costing	April 2013
New Insertable B-layer Installation	Ready end 2014, install 2016 if all OK
Inner Tracker TDR	Dec 2014
Production readiness reviews and ramp up production	2015
Procure parts, Component assembly	2015 - 2017
Machine shut-down for Phase-I upgrades	2016
Surface assembly	September 2017 - end 2018
Surface testing	2019
Stop LHC	Dec 2019
Remove old detectors, install new ones	Jan 2020 - Mar 2021
Commission new detectors	Apr 2021 - Jun 2021
Take data	July 2021

ATLAS Upgrades

Phase 1:

- Trigger / DAQ: Moderate upgrades
- Pixels: IBL
- Muons: reinforce CSC by adding extra layers
- Other minor upgrades, e.g. TRT HV PS



Phase 2:

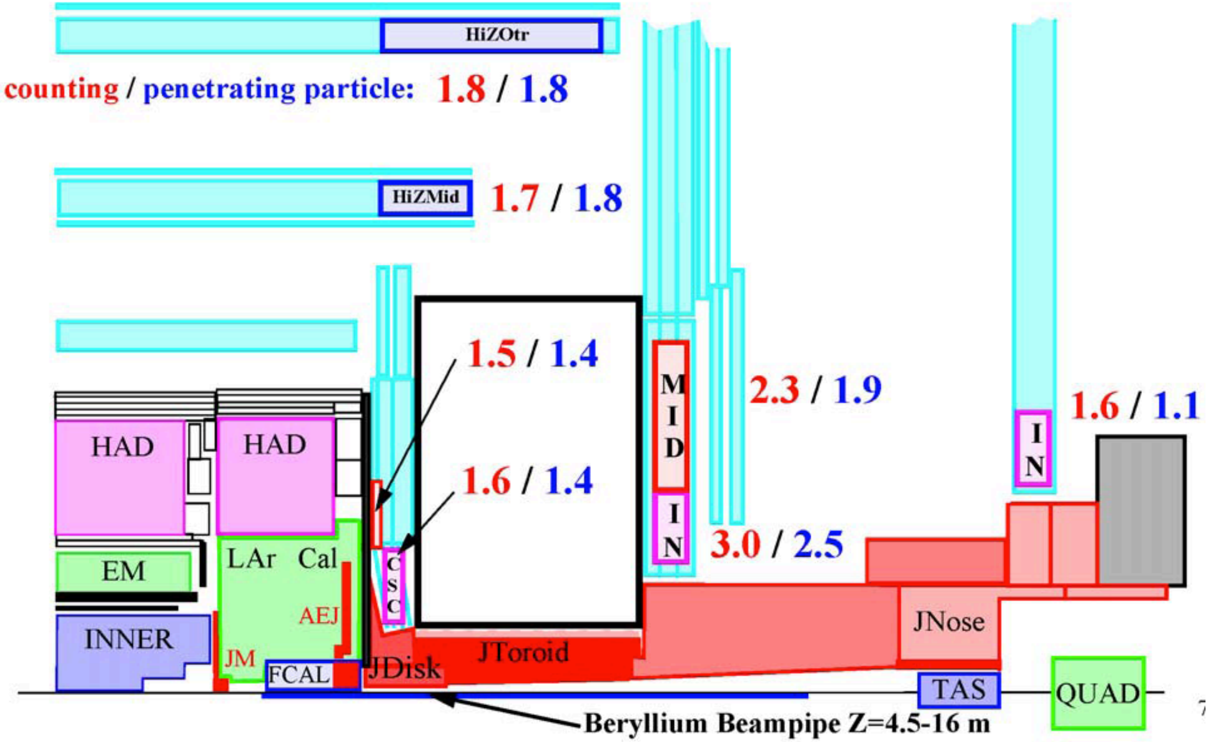
- Inner tracker: Full replacement
- Trigger / DAQ: Major upgrades
- Muons: new forward chambers
- LAr calorimeters
  – Electronics in barrel
  – New forward elements
- Tile calorimeters: Electronics

Phase 0:

- All-Be Forward Beampipe

Phase-0 : 15 months: ***2012 to spring 2013***
Phase-1 : 12 months: ***entire 2016***
Phase-2 : 18 months: ***end of 2019-early 2021***

Phase 0: All-Be Forward Beampipe



- All-Be beam pipe reduces muon bkg considerably (factor of 2)
  - Expensive, but **much** cheaper than new muon chambers
- The present shielding layout has been optimized for years and there is no simple improvement of the shielding that would give a large reduction in background rate. Even drastic and very costly / time consuming changes will not reduce the rates by more than a factor of 3

Phase I: IBL

New b-layer around a smaller beampipe, stave structure, 160 MHz readout, (CO_2) evaporative cooling

- **Planar sensors:**

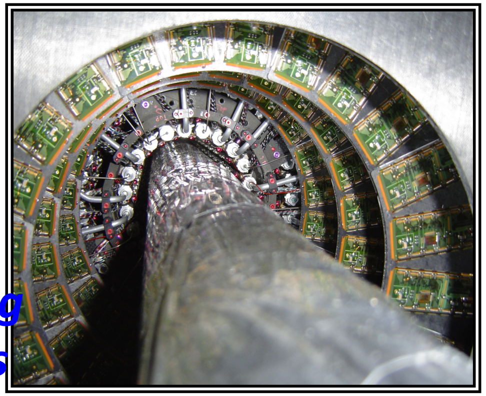
the lowest operating T
high bias voltage
low cost / high yield
well understood manufacturing sources ,mechanical properties

- **3D sensors**

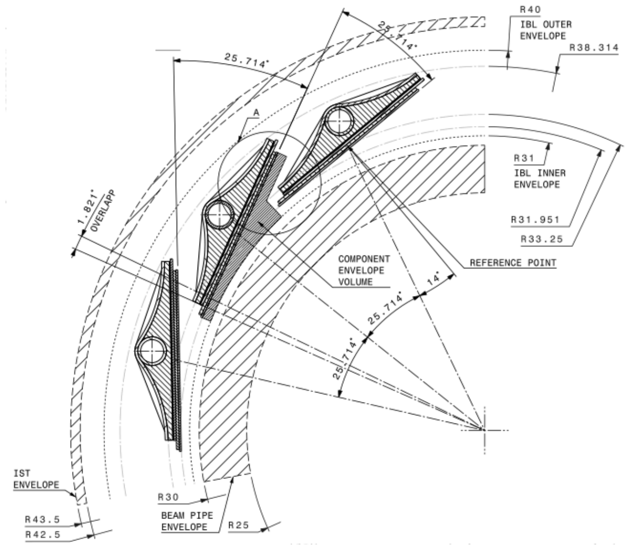
intermediate operating T
the lowest bias voltage
highest geometrical acceptance due to the active edges
manufacturability with high yield / good uniformity**???**

- **Diamonds**

the least cooling
have low leakage current and capacitance
similar bias voltage requirements as planar sensors
manufacturability with high yield, moderate cost, good uniformity**???**



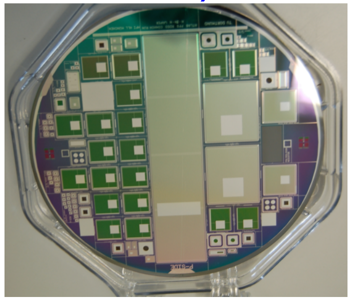
- Improves ATLAS vertexing
- Backup in case of problems with current B-layers
- TDR being prepared



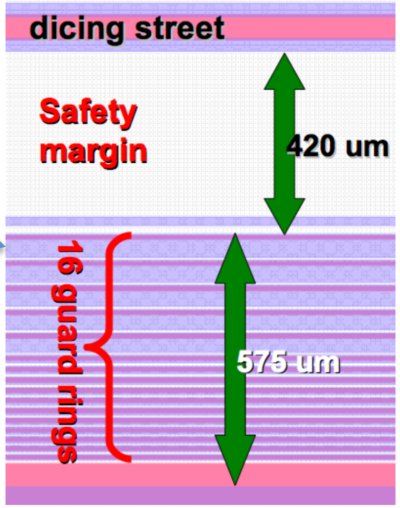
the sensors facing the beam-pipe

The ATLAS Planar Pixel Sensors R&D

- Aim: Explore the suitability of planar pixel sensors for highest fluences (IBL: $5 \cdot 10^{15}$ n_{eq}/cm^2, SLHC: 1-2 $\cdot 10^{16}$ n_{eq}/cm^2)
- Approved ATLAS R&D project since 2009: 17 institutes, > 80 scientists
- Main areas of R&D:
  - Radiation damage studies with n^+-in-n and n^+-in-p sensors (next slide)
  - Improved sensor design for future readout chips (FE-I4, …)
    - both n-bulk and p-bulk sensors designed
    - First FE-I4 compatible sensors already available
    - FE-I3 compatible sensors with (almost) identical design for radiation studies being produced



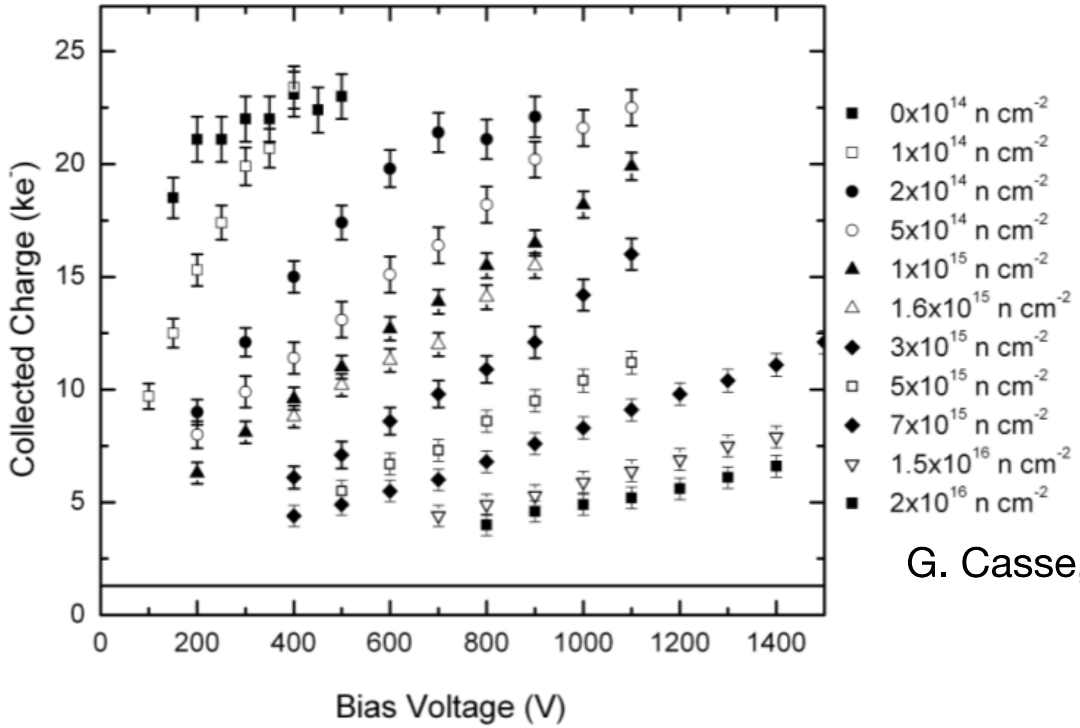
  - Device simulations of radiation-damaged silicon (backup)
  - Reduction of inactive edge width (backup)
    - Current ATLAS design: ~1000 µm
    - Flat module arrangement for IBL needs < 450 µm
  - R&D on cost reduction to enable large-radius pixel layers



The ATLAS Planar Pixel Sensors R&D

Radiation damage studies

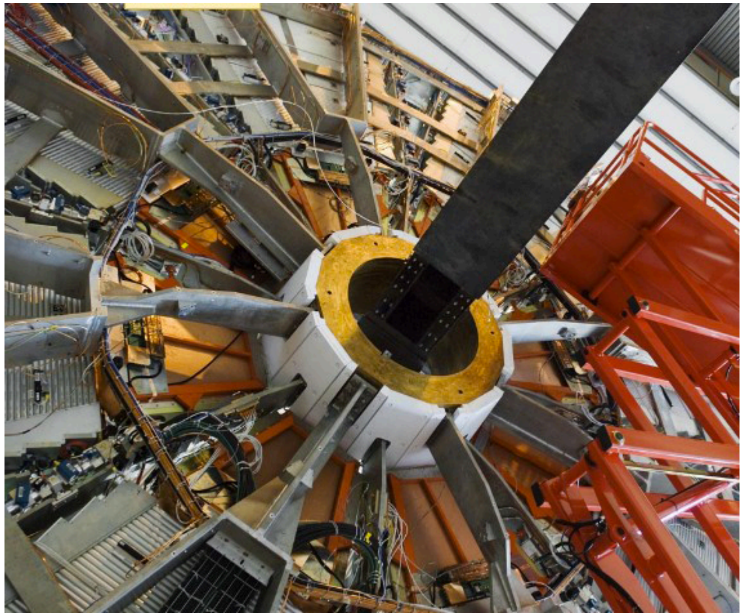
- Planar sensors withstand extremely high fluences:
  - Charge amplification effects observed after high fluences at high bias voltages
  - Increasing leakage current demands sufficient cooling
  - Testbeam studies with irradiated pixel sensors ongoing
- Preliminary conclusion: Planar pixel sensors
  - can be safely operated at IBL-fluences and with sufficient cooling even at sLHC fluences.
  - collected charge goes down → readout-chip threshold becomes important!

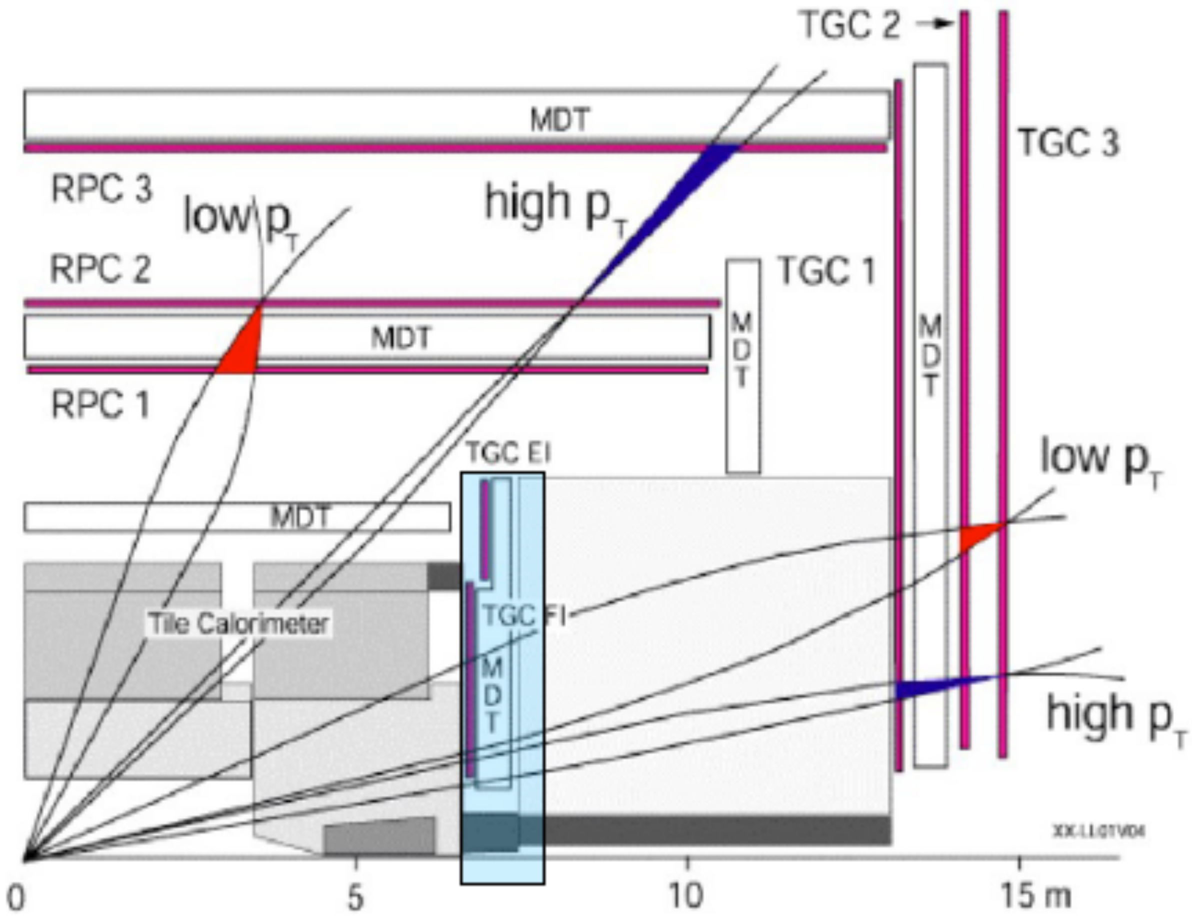


G. Casse, Vertex2010

Phase I: Muons

• The performance is background driven, not signal driven. Large uncertainty on rates – safety factor of 5 used in design
• New small wheels, recover staged CSCs with new detector technologies
• New electronics for trigger improvements / considering bringing MDT into trigger



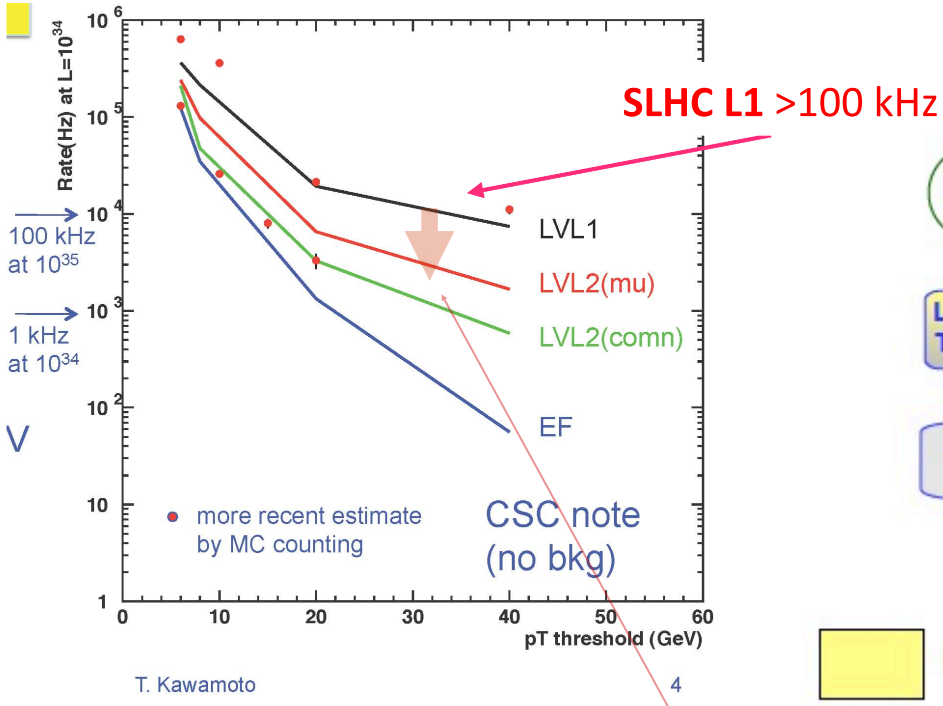


• R&D into new technologies that would also work for Phase II (e.g. Micromegas)

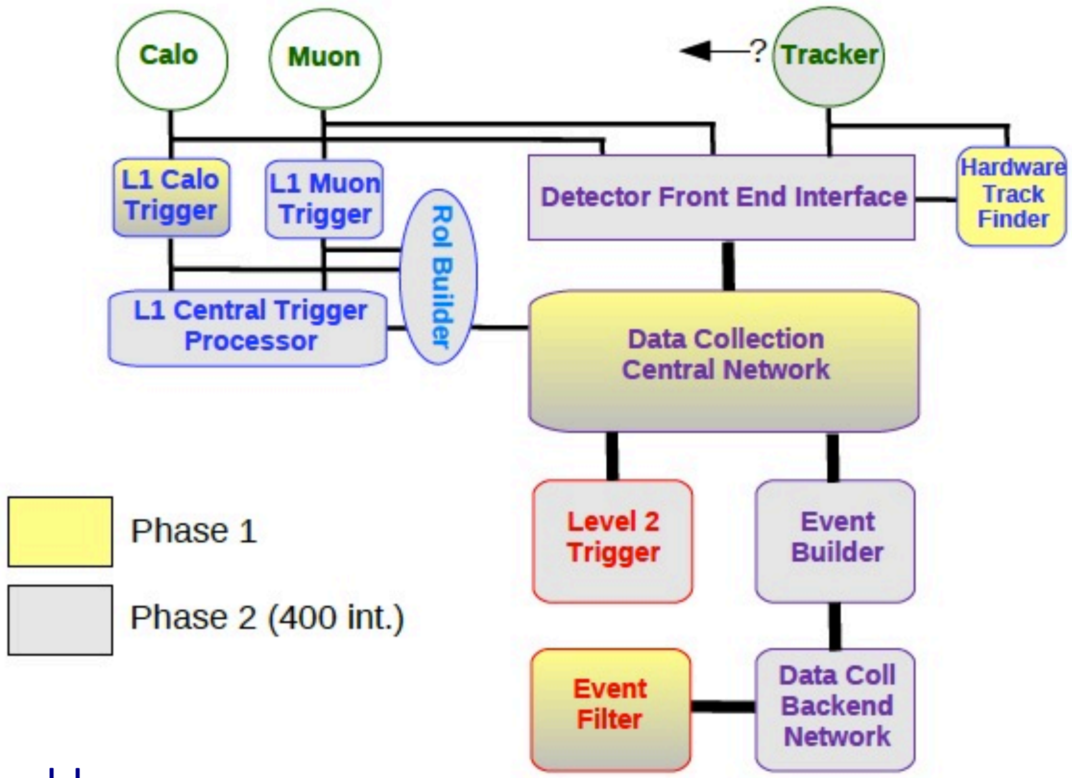
Phase I: TDAQ/Trigger

- Level-1 sensitivity to low-pt leptons, despite pileup & cavern background
- DAQ able to read out and transport larger events
- The trigger hardware is outside the experimental cavern => accessible/can be upgraded.

Muon inclusive high-pt trigger



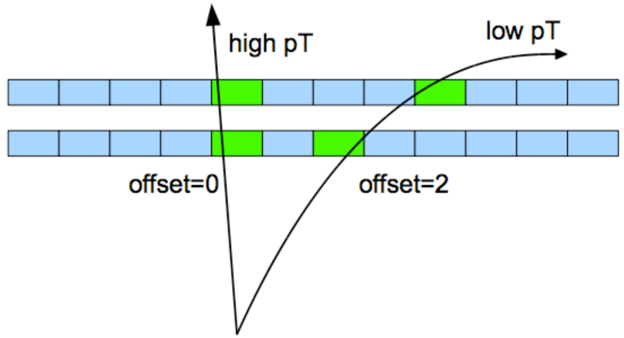
One more mu trigger layer would reduce significantly this rate (under study now)



An ID track segment with Pt > 20 GeV would reduce a trigger rate by 1 order of magnitude.

Phase I: TDAQ/Trigger

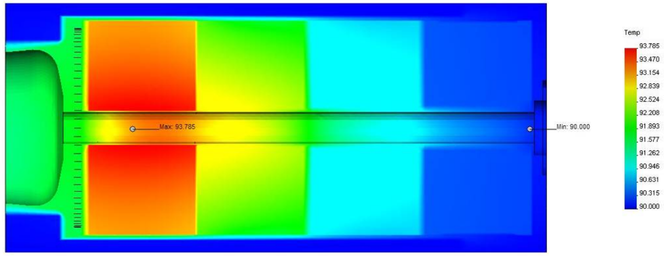
- Various projects being pursued / reviewed:
  - Track trigger
    - Fast Track Finder (FTK), hardware track finder for ATLAS (at L1.5)
    - ROI based track trigger at L1
    - Self seeded track trigger at L1

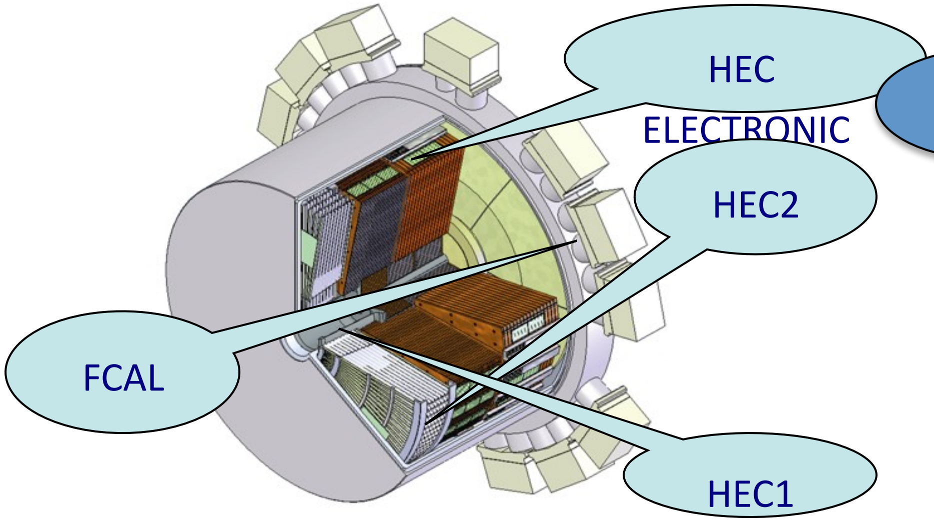


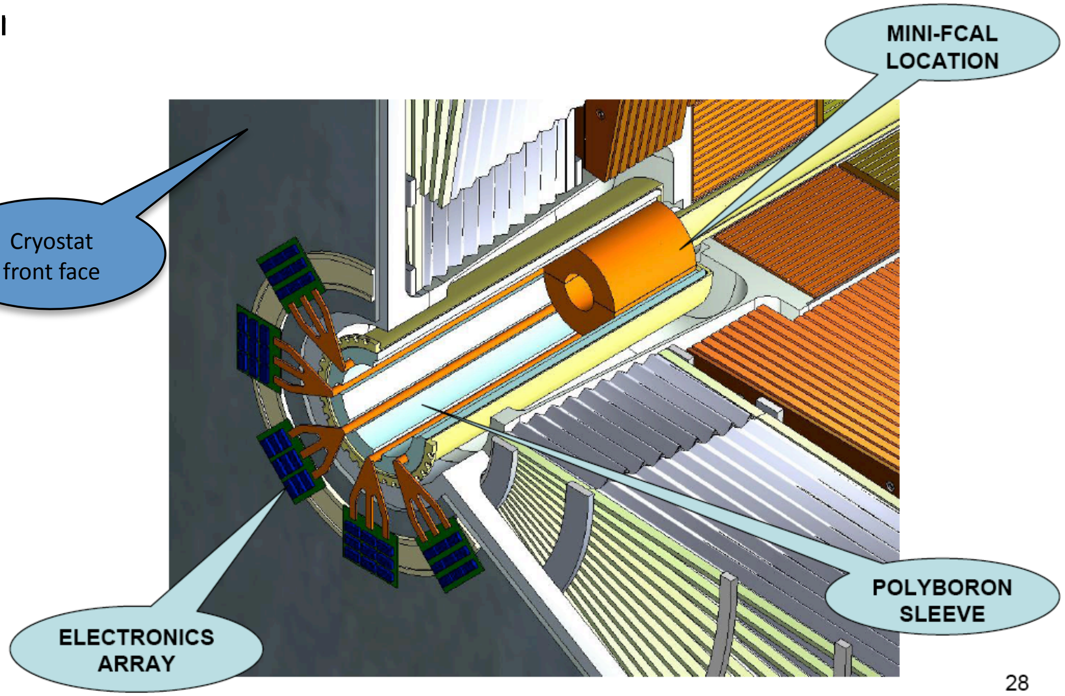
  - Combining trigger objects at L1 and topological “analysis”
  - Full granularity readout of the calorimeter (requires new electronics)
  - Changes in muon systems (small wheels), studies of an MDT based trigger, and changes in electronics
  - Upgrades of HLT farms
- Some of the changes are linked to possibilities that open when electronics changes are made (increased granularity, improved resolution and increased latency)

Phase II: Calorimeters

- Electronics changes being foreseen – for better performance and granularity
  - Trigger improvements might give a strong motivation for electronics changes
- Forward calorimetry in particular might suffer from radiation effects
- ATLAS forward LAr calorimeter:
  - Boiling of LAr, ion build up between electrodes, voltage drop over HV resistor
  - Studies underway; If these show action is needed, two solutions considered:
    - Warm calorimeter in front of current calorimeter (Cu/Diamond)
    - Open cryostat, insert new FCAL with sı



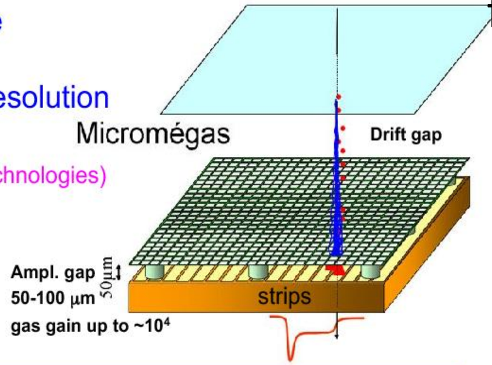




Phase II: Muons

Micromegas for tracking + trigger

- Very high rate tolerance
  measured in kHz/mm^2
- Good spatial and time resolution
- Low cost (potentially)
  Bulk MicroMegas (industrial technologies)
  - use of wire mesh
  - PC board technology



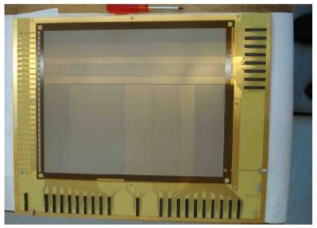
Goal:
$\sigma_x < 100\ \mu m$
$\sigma_t < 5$ ns
size ~ 1x2 m^2

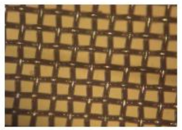
For EI (+ inner EM) region, with tracking + trigger in a single detector unit. (good, because of the limited space).

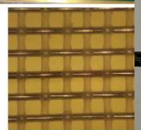
12.02.2008 T. Kawamoto 9

- Already used on CAST experiment (looking for axions from the sun)

Prototype chambers 45 x 35 cm^2 (2 of the bigg

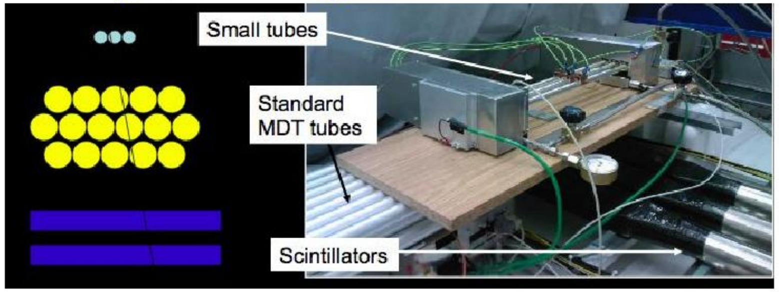


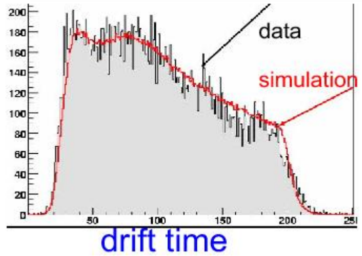




Thin tube MDT

Prototype, cosmic-ray tests 15 mm tube

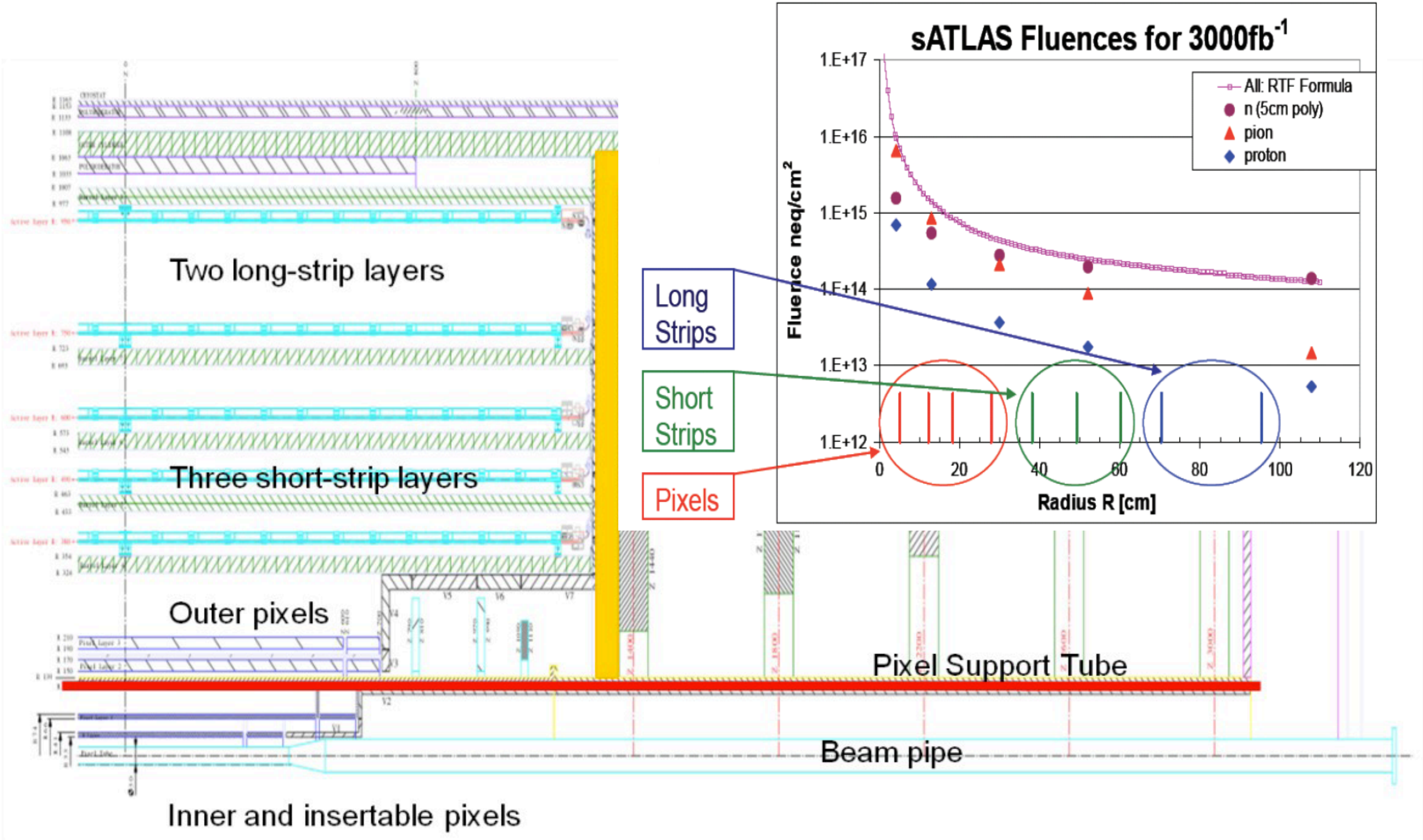




Outlook

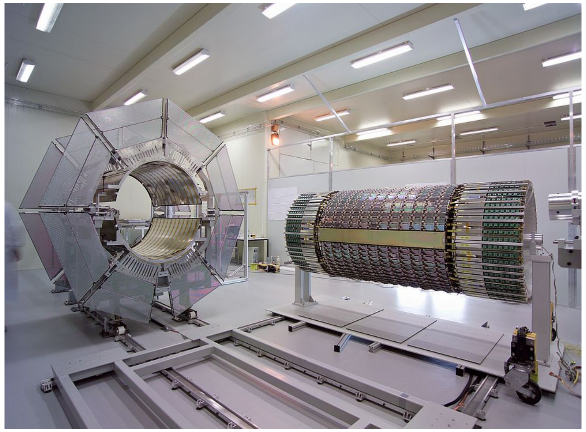
- 15 mm tube : x10 higher limit
- Cosmic ray test results promising
- Further tests at GIF planned in 2008

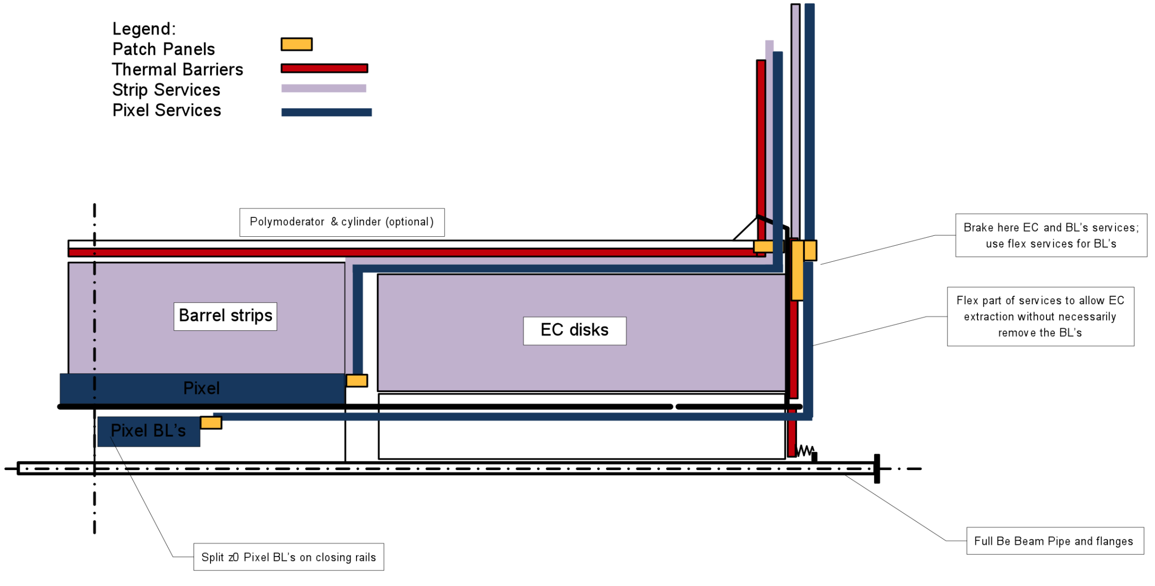
Phase II: Inner Detector



Phase II: Inner Detector

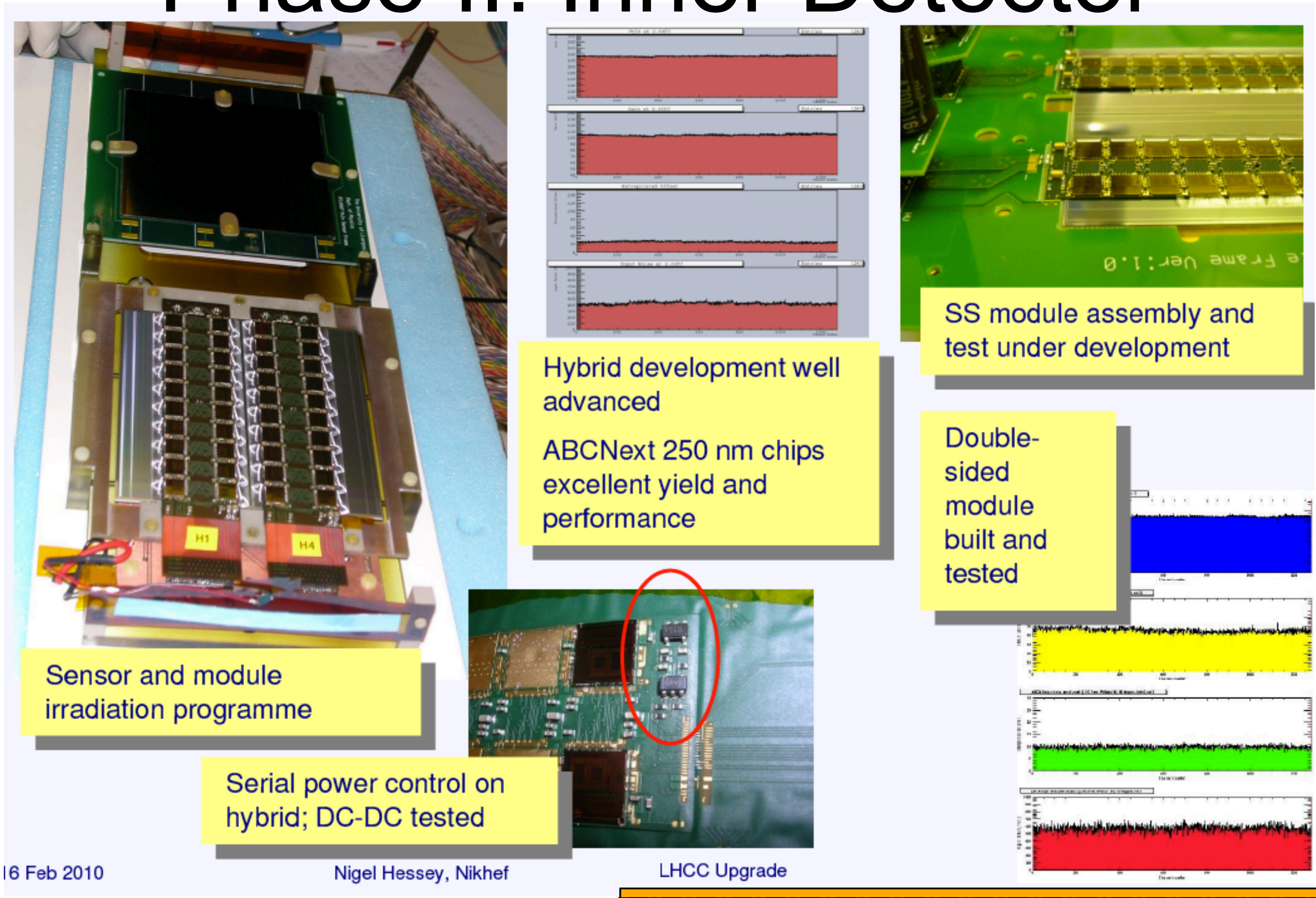
- Critical parts: sensors, ASICs and system engineering
- Develop and buy silicon sensors for few 100 of m^2 silicon sensors (need finer granularity):
  - Extend previous studies from LHC to SLHC fluence – large irradiation programs needed
  - Extend previous studies to include n-on-p (can operate not fully depleted after irradiation)
  - Study biasing, guard rings, isolation methods, substrate variations

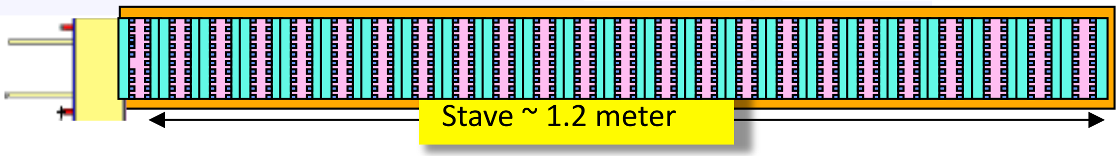




Also for the ID one can consider to make it such that barrel, EC and PIXEL systems are individual units, allowing at least some access in case of problems, and also some flexibility in installation

Phase II: Inner Detector





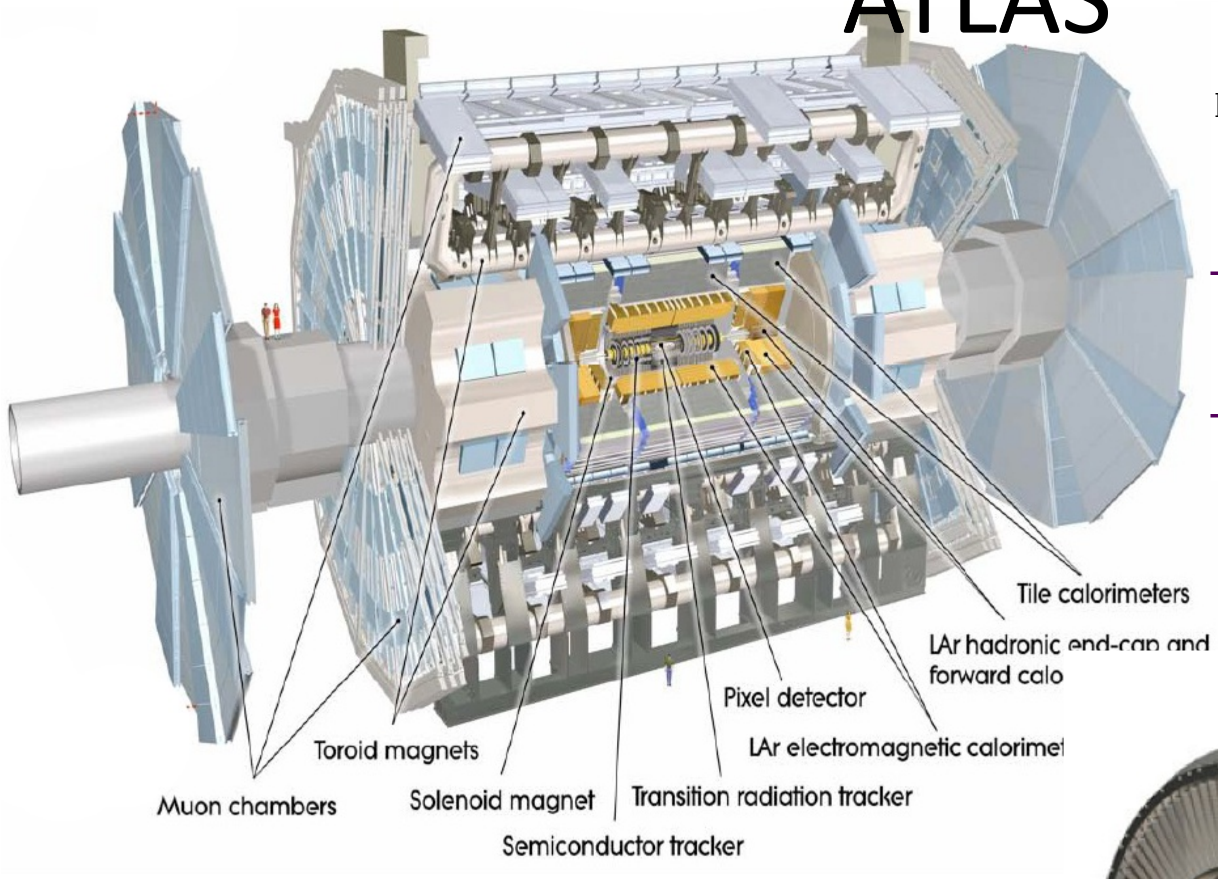
Various silicon strip tracker developments

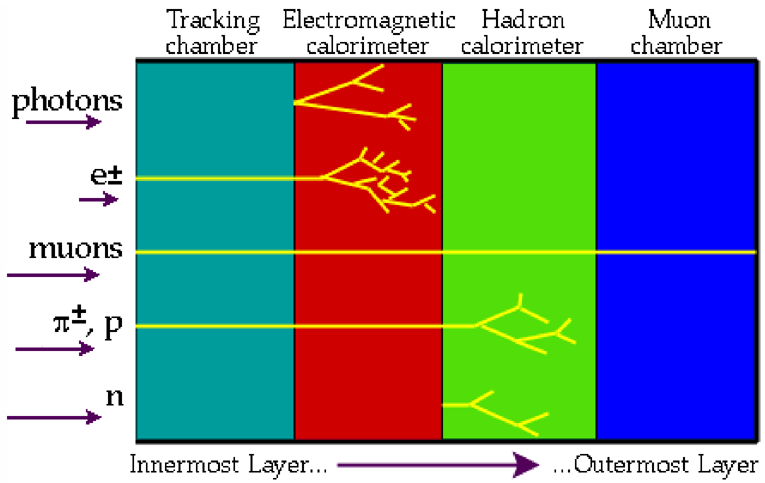
Summary

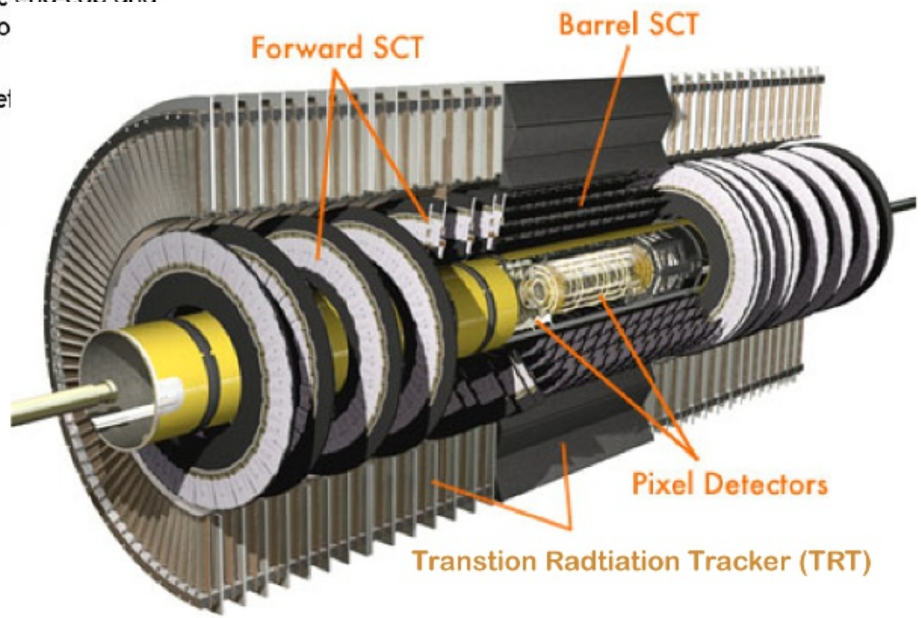
- 10 years of R&D, construction, commissioning on the way to the sLHC
- Main focus are inner detector, electronics and trigger changes, and in the forward direction
  - Focus on detector performance, not only on replacing parts that are expected to fail due to radiation or luminosity increases
  - The ID replacement is needed due to radiation damage
  - Muon detectors
  - LAr calorimeter
  - Electronics and Trigger changes (for L1) allow ATLAS to maintain its performance at the sLHC
- Upgrade projects are being formed, the IBL is the first example
- Learning by doing:
  - IBL => ID replacement
  - Micromegas @ CAST => Micromegas @ ATLAS

Backup

ATLAS







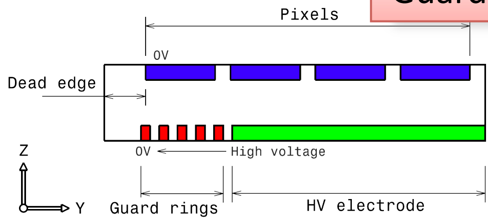
Detectors and identified objects:

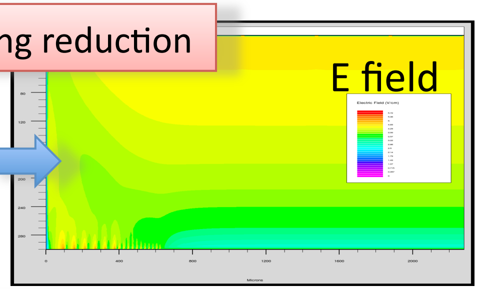
- Trackers: e, mu, jets, photons
- Calorimeters: e, mu, jets, MET, photons
- Muon Detectors: mu

TCAD simulation is used to

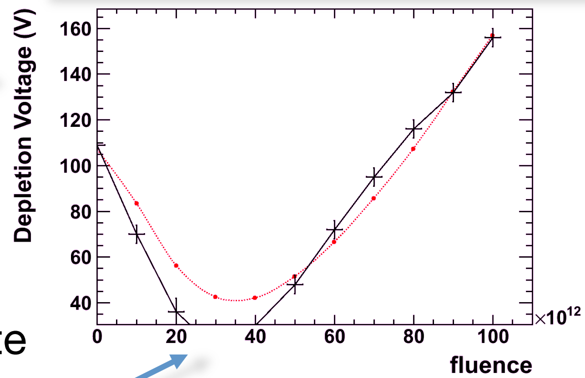
- Optimize Sensor geometry to reduce inactive edges and breakdown voltage
- Understand physics of irradiated devices
  - Charge multiplication
  - electric field distribution, double junction
- A set of experimental measurements is currently being performed to calibrate simulation and radiation damage model
- Calibrated model will be used for the simulation and optimisation of PPSU and IBL planar sensors
  - Reduce number of GRs
  - Enhance CCE at high fluences and bias voltages
  - Increase breakdown voltages

Guard ring reduction

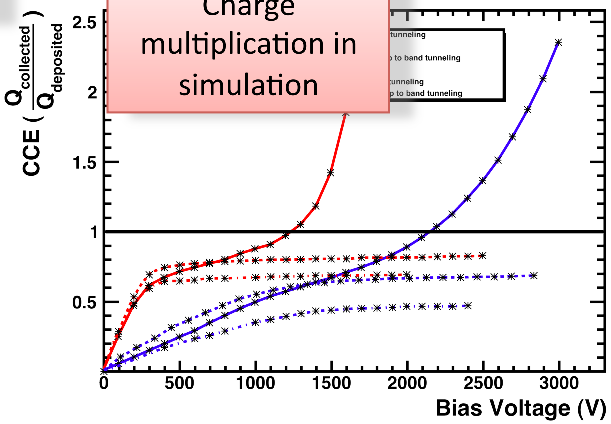




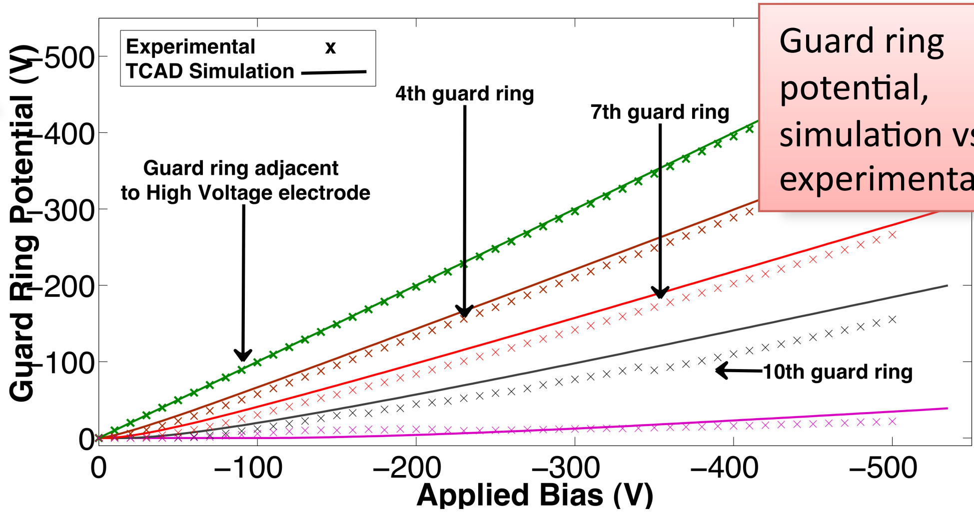
Vfd vs fluence, simulation vs experimental



Charge multiplication in simulation



Guard ring potential, simulation vs experimental



M. Benoit

Phase II: Trigger improvements

Upgrade options

The ATLAS detector is rather accessible and several upgrade scenarios are studied to improve the L1 trigger for SLHC

Calorimeters

Full readout of calorimeters (LAr and TileCal) → full granularity already at L1

Topological triggers

TileCal rear sampling in muon sector logic

Muon chambers

New high rate and granularity muon chambres (small wheels)

Muon Drift Tube (MDT) readout in L1 trigger

Trackers

Fast TacKer (FTK), hardware track finder for ATLAS (at L1.5)

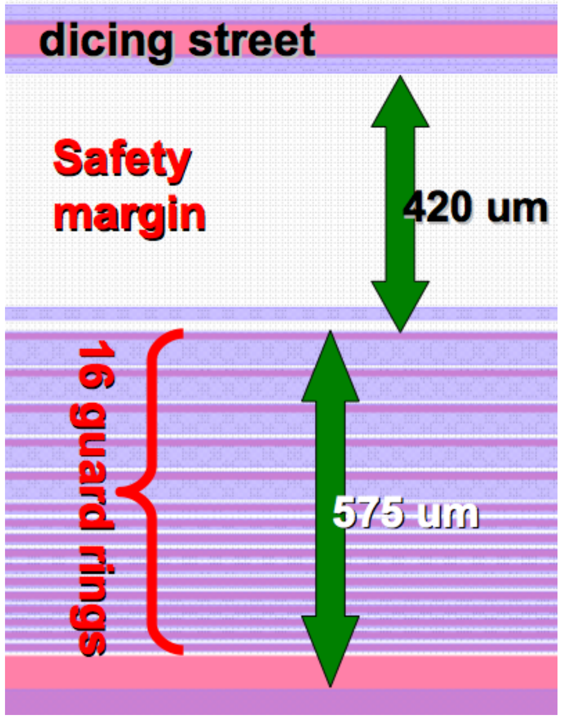
ROI based track trigger at L1

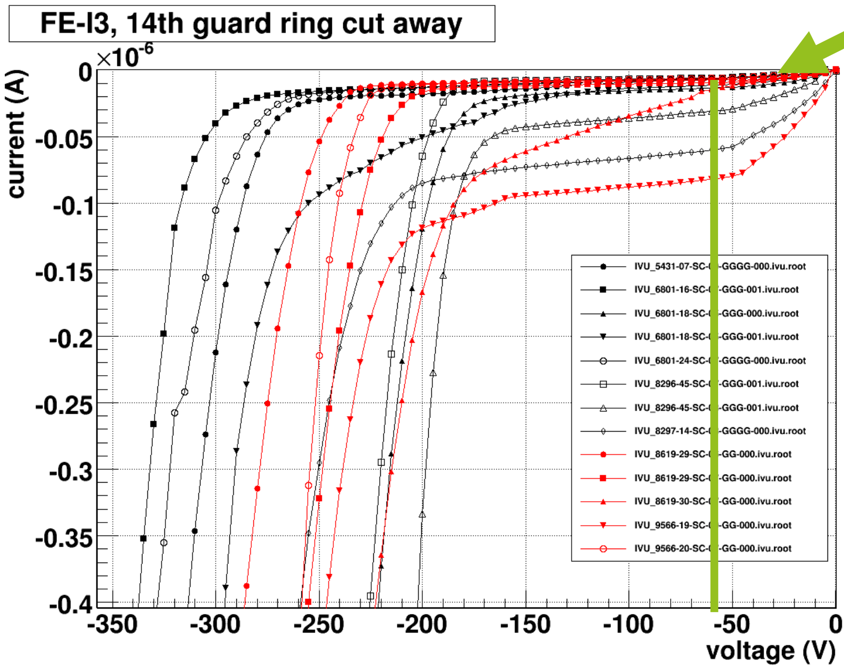
Self seeded track trigger at L1

The ATLAS Planar Pixel Sensors R&D

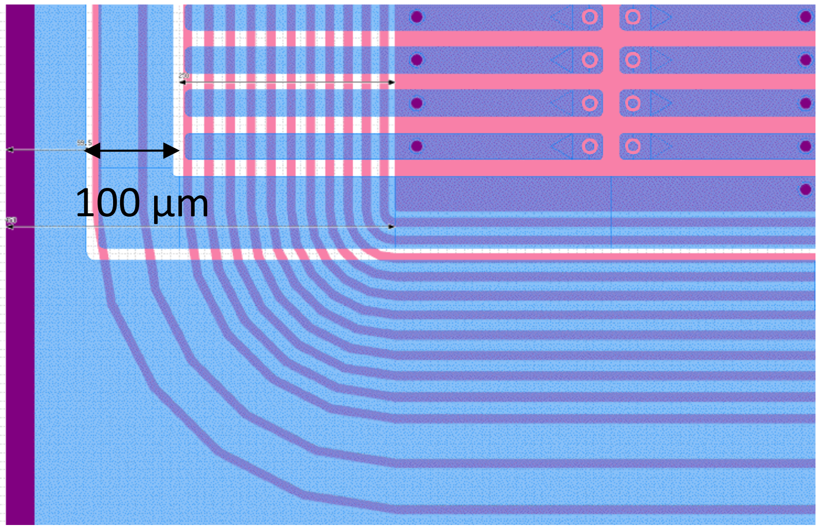
Slim edges

- Current ATLAS n-in-n design: ~1000 µm inactive edge!
- Flat module arrangement for IBL needs slim edges < 450 µm to limit geometric inefficiency
- Ideas:
  - Less guard rings
  - guard rings opposite of pixels
  - less safety margins
- Reduction to 100-200 µm safety margin seems possible with sufficient breakdown voltage ($V_{breakdown} > V_{depletion} + 50V$)





T. Wittig



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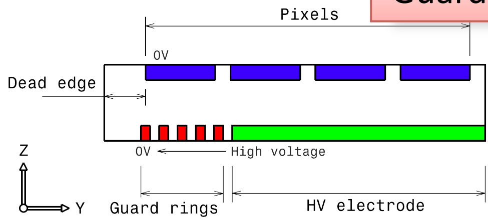

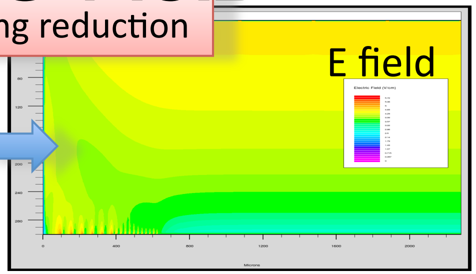

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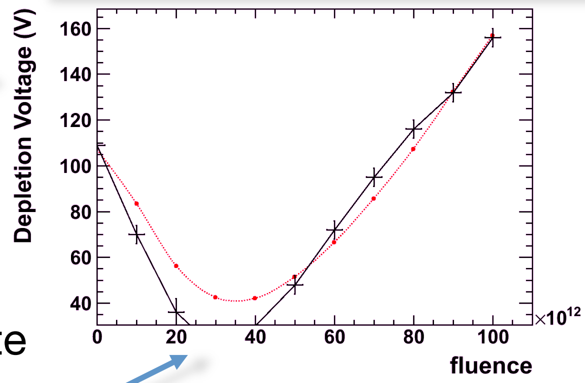
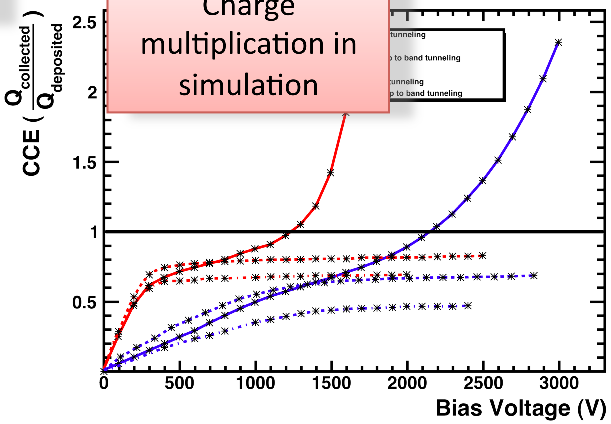


Charge multiplication in simulation



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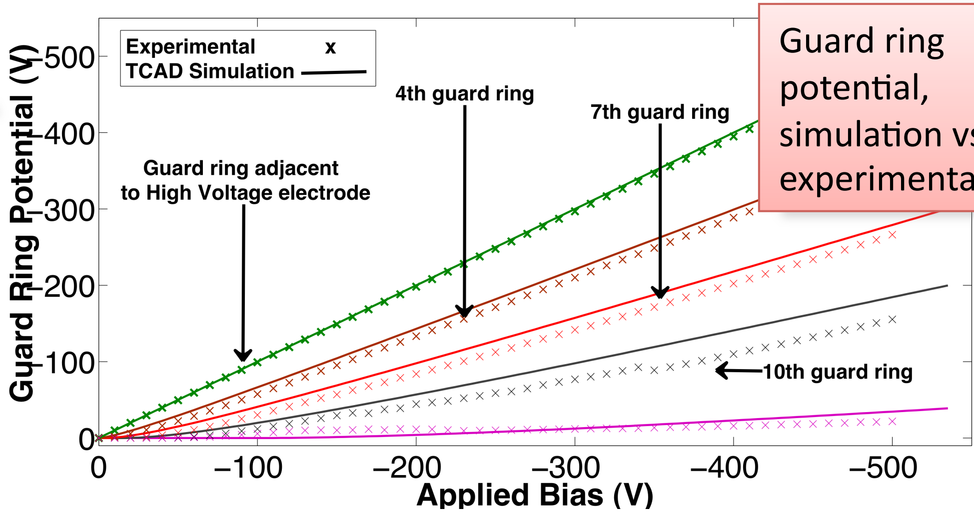

M. Benoit

New Features & Status FE-I4

- New features
  - Biggest chip in HEP to date
    - 20.2mm x19mm (pixel matrix: 16.8mm x 20mm, 336x80 pixels)
  - Greater fraction of the footprint devoted to pixel array
  - Lower power
    - (=> don't move the hits around unless triggered)
  - Able to take higher hit rate
    - (=> store the hits locally in each pixel and distribute the trigger)
  - No need for extra module control chip
    - (=> significant digital logic blocks on array periphery)