

# Announcements

## Working Group-5 on Common Electronics

### WG5 Tasks:

[Definition of front end electronics requirements for MPGDs](#)

[Development of general purpose pixel chip for active anode readout](#)

[Development of large area detectors with pixel readout](#)

[Development of portable multichannel data acquisition systems for detector studies](#)

[Discharge protection strategies](#)

Convenors: Hans Muller CERN PH, Jochen Kaminski, Bonn University

# WEB page of WG5

<https://espace.cern.ch/rd51-wg5/default.aspx>

Administrator: Sorin Martoiu

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Home | Chip Matrix | SRS | wiki

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Chip Matrix

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wiki

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## Working Group 5

### MPGD Related Electronics

The availability of highly integrated electronics and associated readout systems poses a non-trivial problem to many of the modern MPGD applications. Users need an easy-to-use, portable readout system. In a first attempt, characteristics for such a system have been collected in order to synthesize a common-denominator requirement. A side-result of this effort is the comparative Matrix of Frontend ASICs which is available and kept up to date on this Webpage. It quickly turned out however that the large spread in requirements ( examples are: signal polarity, trigger concept, timing resolution, radiation tolerance level, analog versus digital, choice of readout bus, number of channels, power and packaging, bandwidth, data formats, DAQ software ) would not allow for a simple common solution, unless one builds a system with 4 general properties: a.) scalability from small to large system b.) common interface for replacing the chip frontend c.) integration of proven and commercial solutions for a minimum of development and custom hardware d.) default availability of a very robust and supported Data acquisition package. Based on these guidelines, the Scalable Readout System (SRS) was proposed and approved, followed by a design effort for the first SRS prototype system. The SRS systems uses links instead of buses in order to overcome the typical bus scaling limits and to

**Calendar**

23/11/2009 09:00 AM RD51 Collaboration Meeting: 23-25 November 2009 at CERN  
<http://indicobeta.cern.ch/conferenceTimeTable.py?confId=72610#all>

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**Links**

- CERN website
- RD51 Official Webpage
- RD51 General Documents
- All talks WG5 September 24 Miniweek
- RD51 Notes
- All talks from July 09 (Crete) WG5 meeting

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So far active: Chip matrix and Scalable RO system  
Please contribute on more activities

# Email WG5

## rd51-wg5-contacts@cern.ch

Please register, either via the CERN IT page  
-> MMM services, Email groups  
or by sending email request to the convenors

HAVE a nice meeting !