

THE USER "POINT OF VIEW" ABOUT THE VFAT2

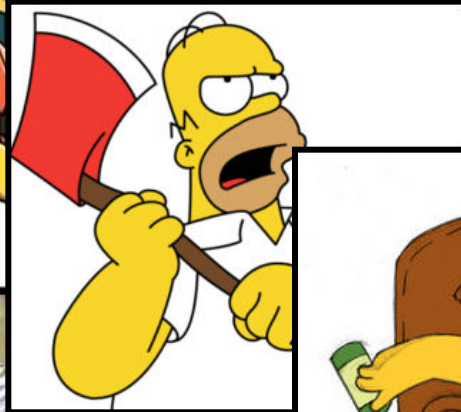
The first day....



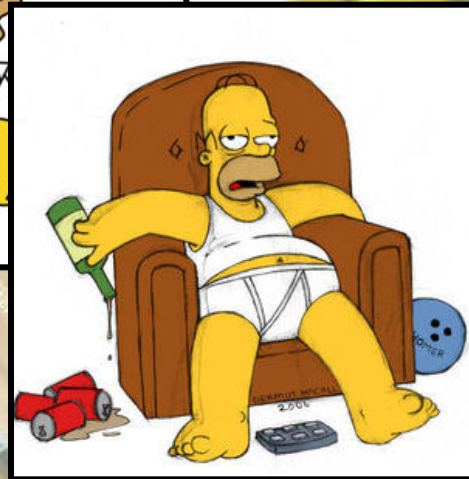
The first week....



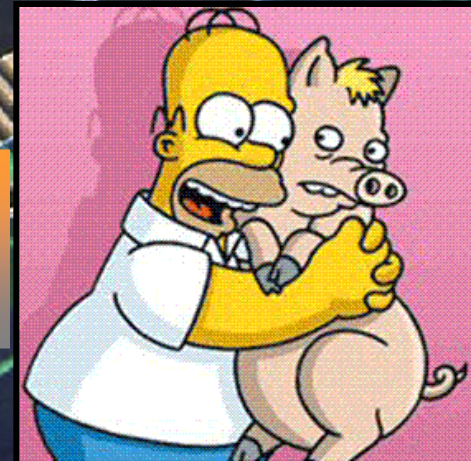
The first month....



The first year...



But at the end you will be a friend of the VFAT2!



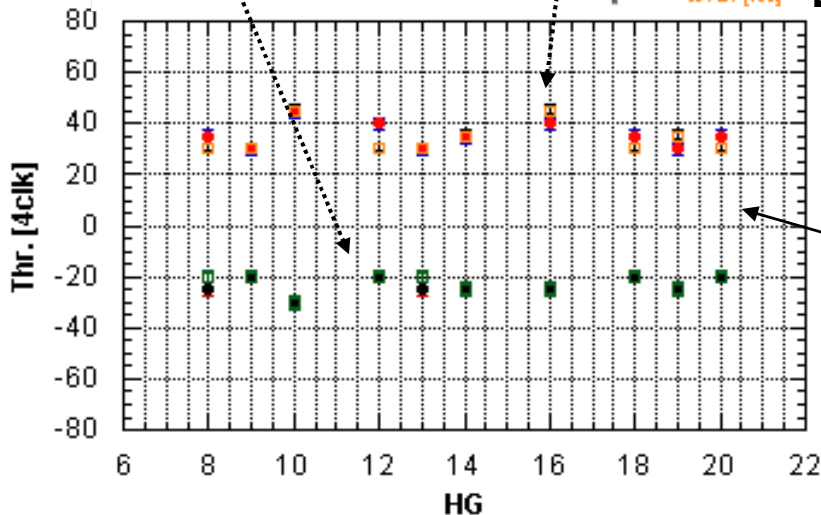
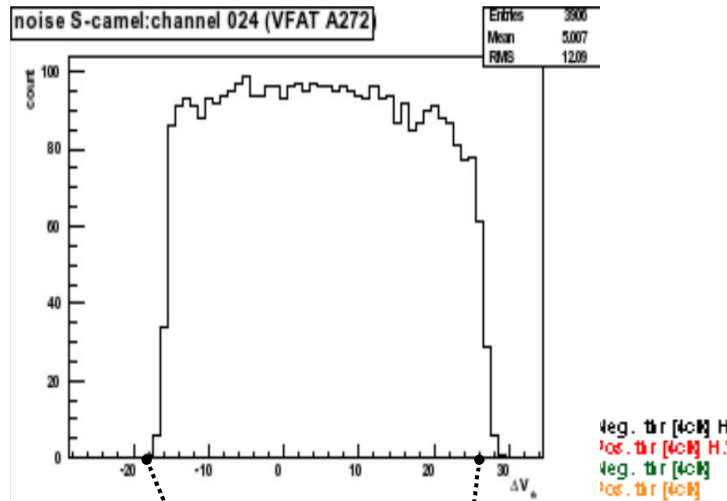
Dear Paul, this is obviously a joke. Please, apologize me.

Some consideration about measurements
and scans with the VFAT2.

All the measurements shown are referred to TOTEM
Triple GEM or RD51 test beam Triple GEM

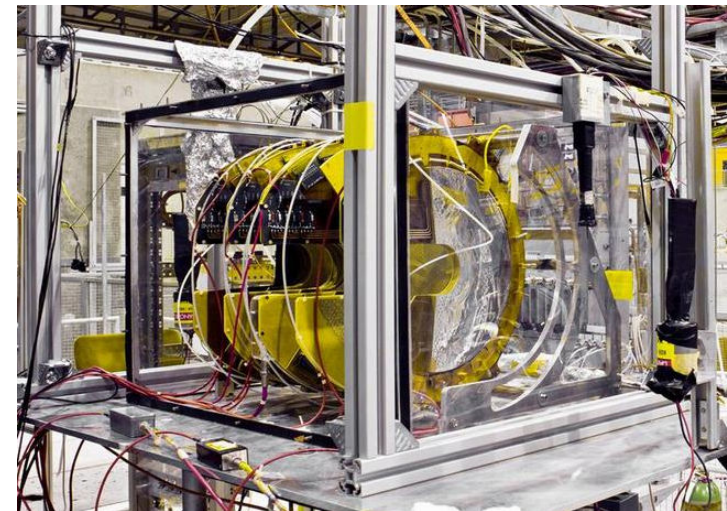
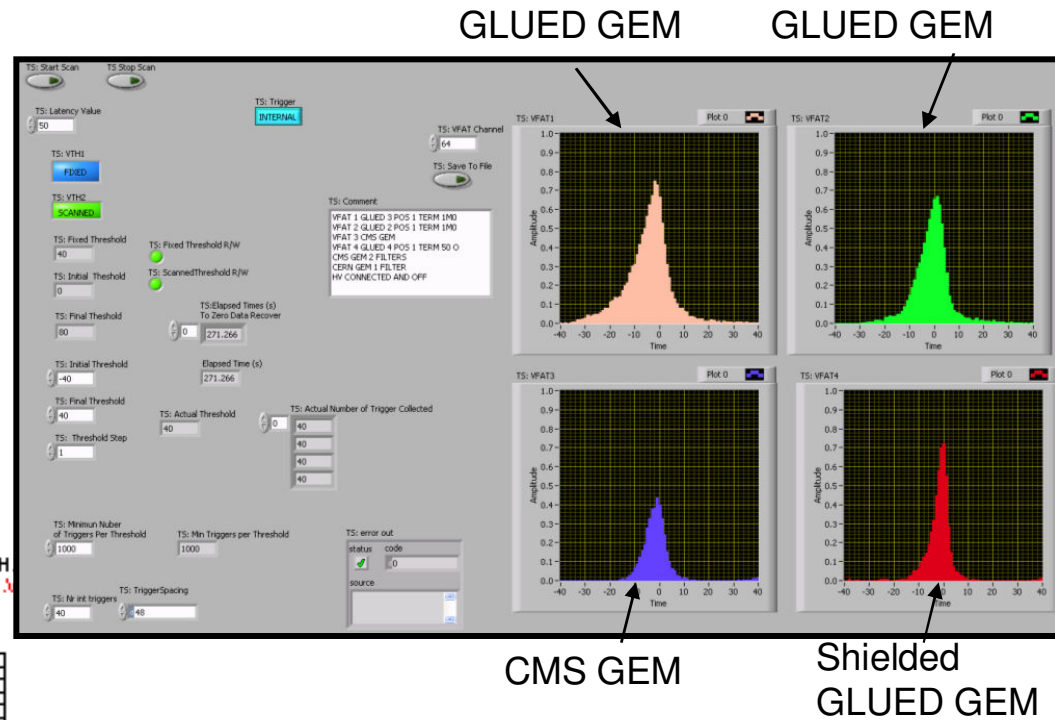
Threshold Scan.

The scan is performed changing automatically the threshold for each acquisition step and the results give you a fast information about your noise condition in all the channels of the vfats.



Threshold scan results for a quarter of T2 (10 Triple GEM)

Threshold scan for one channels of three triple GEM Acquired during the RD51 test beam.



Calibration Pulse Scan.

The scan is performed changing automatically the charge injected by the calibration pulse. This measurement can be performed only on few channel per scan, but the result is very precise and it can show you for example the correlation with the capacitance of the readout electrode.

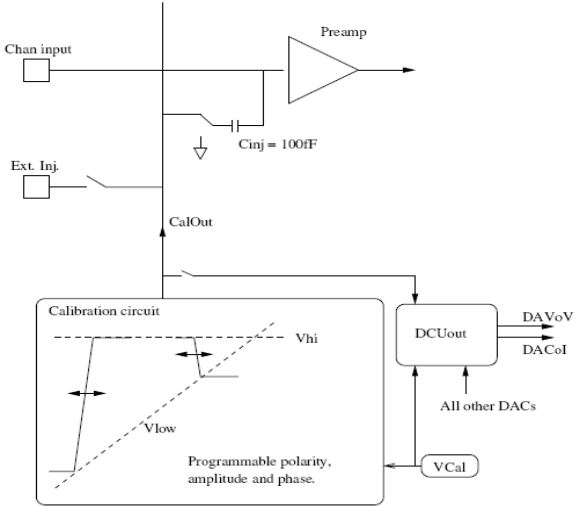
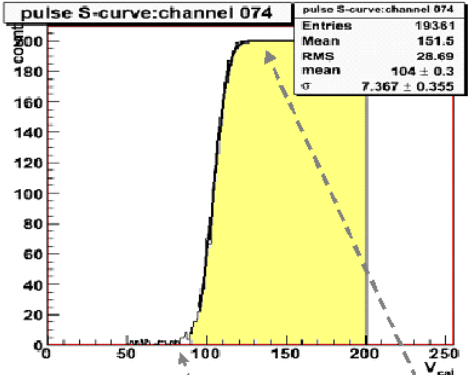
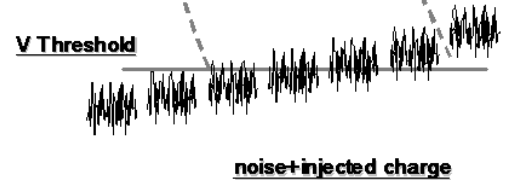


Figure 2: The Calibration pulse amplitude

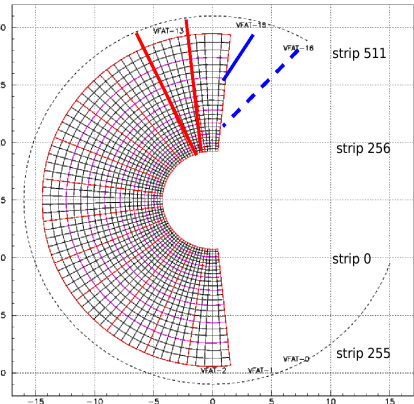
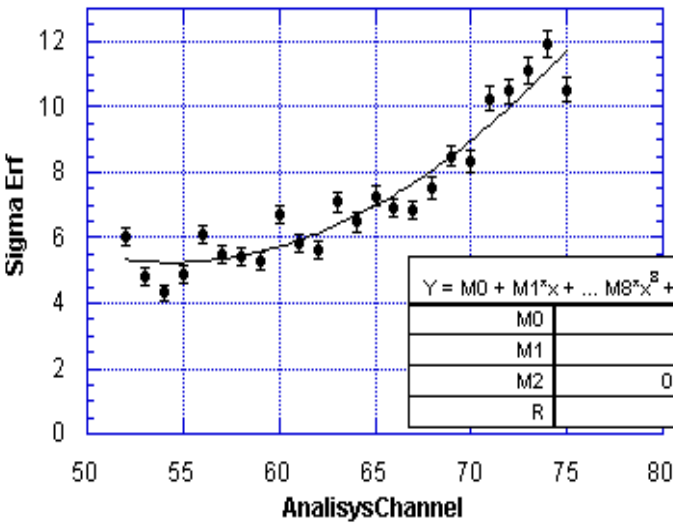


Just to have a qualitative picture....

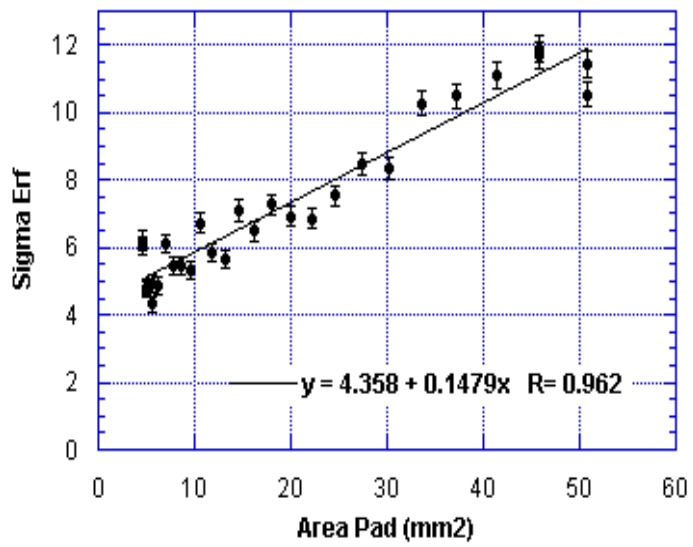


noiset+injected charge

Sigma Erf vs Channel



Sigma Erf vs Area Pad

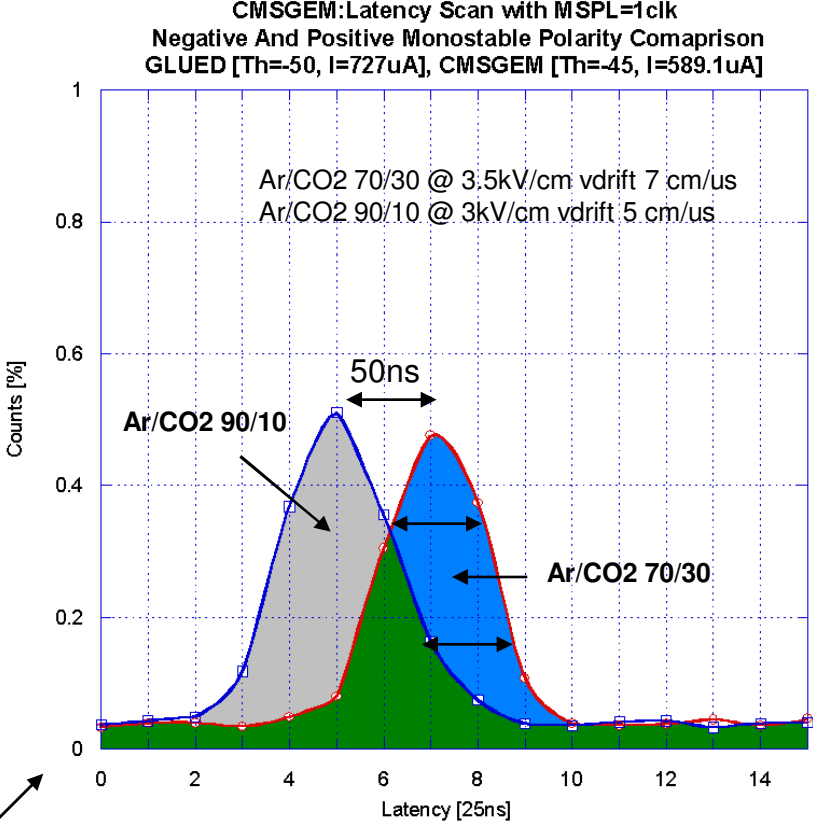
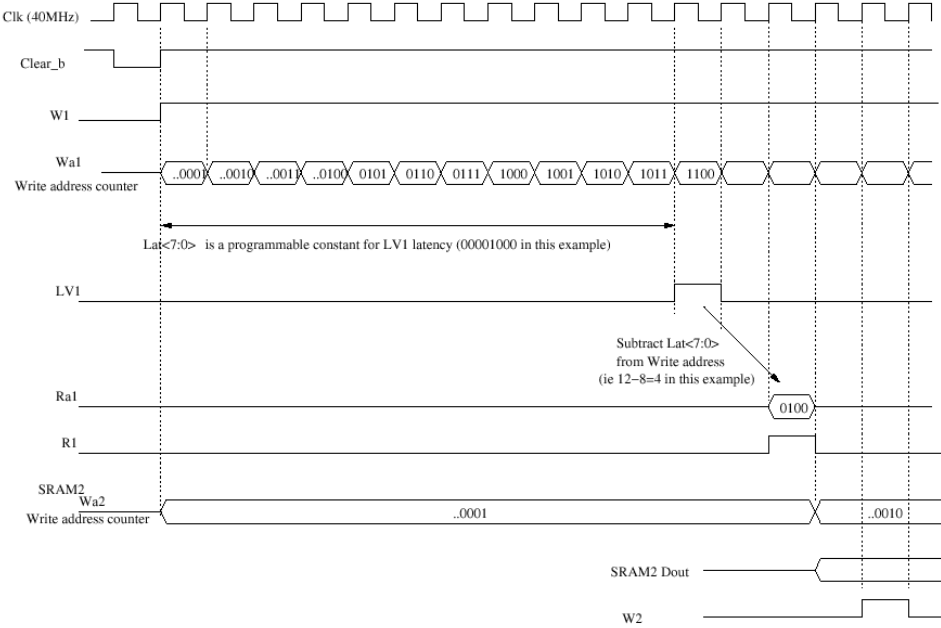


Latency Scan (with Beam or with the internal calibration pulse).

The scan is performed changing automatically the latency to the vaft (i.e. the memory cell read when a trigger is sent to the VFAT2).

5.3 The latency register (LAT)

There is one 8 bit register used for programming the LV1A latency into the chip. Each bit represents one clock cycle of latency. The latency can be programmed from 1 to 256 clock periods (ie. up to 6.4μs). The default setting is 1000 0000 (=128 clock cycles).



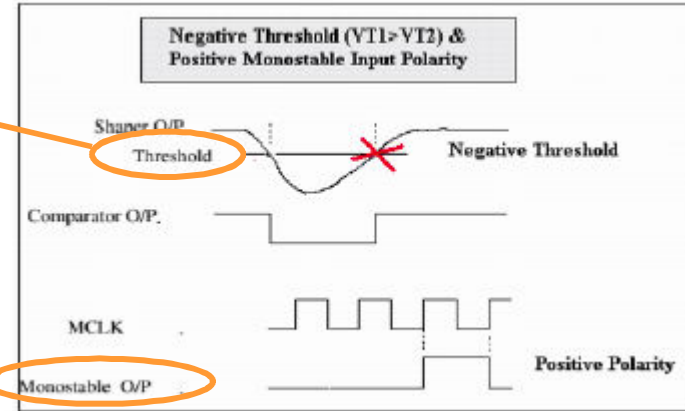
$(0.4\text{cm (transfer gap)}) / (5\text{cm/us}) - (0.4\text{cm}) / (7\text{cm/us}) \sim 80\text{ns} - 57\text{ns} \sim 25\text{ns}$
 Considering the different gains and VFAT internal synchronization, this is compatible with the measurement.

One example from the RD51 Test Beam:

This scan (performed with beam) is necessary to define the right latency that you have to write on the VFAT2 register, but it is also useful to get timing information.

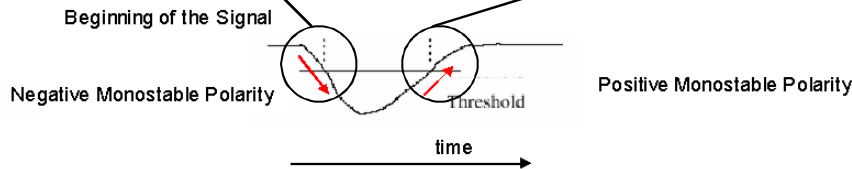
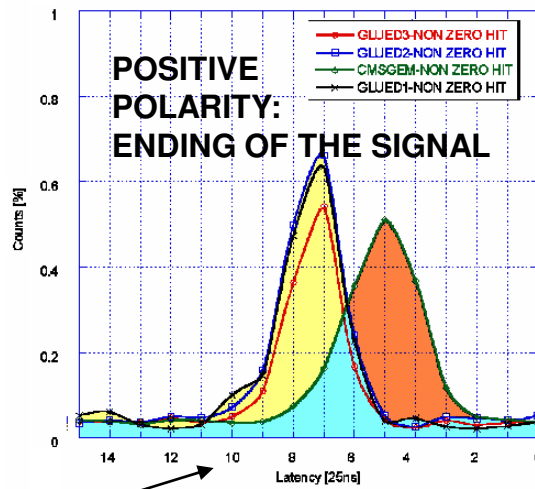
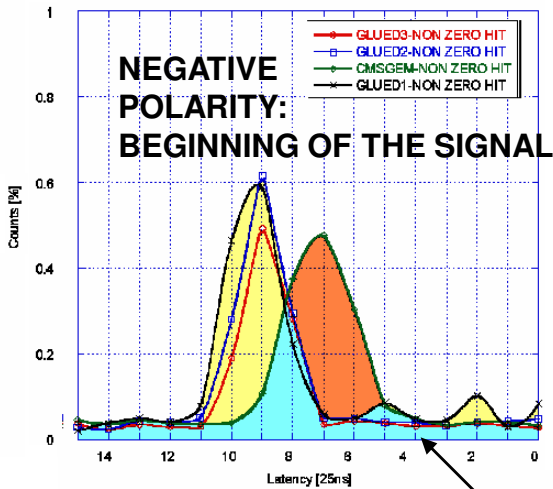
VFAT2 Threshold and Monostable Polarity

Playing with threshold and monostable polarity is like playing with your scope with trigger level (thresh.) and negative or positive slope (monost. Pol.)...



Latency Scan with MSPL=1clk and Negative Monostable Polarity
GLUED [Th=-50, I=727uA], CMSGEM [Th=-45, I=589.1uA]

Latency Scan with MSPL=1clk and Positive Monostable Polarity
GLUED [Th=-50, I=727uA], CMSGEM [Th=-45, I=589.1uA]



idem for positive threshold

...and if you use them properly you could get information about your signal (the duration is one example)

Latency scan performed during the RD51 test beam on two Triple GEM in Ar/CO2 70/30 (yellow) and ArCO2 90/10 (orange) respectively.

Timing Studies: using the fast-OR outputs of the VFAT2 ...

The 8 fast s-bits of the VFAT can be used for an analysis of the timing properties of the detector.

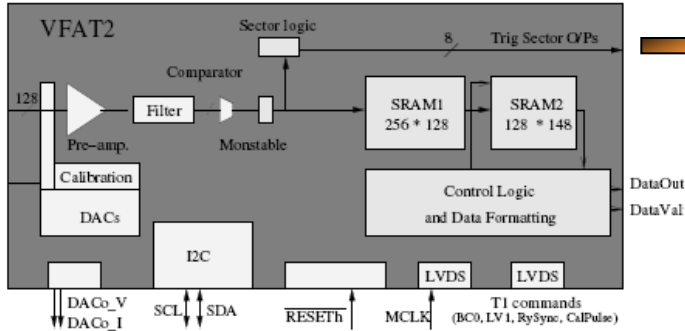


Figure 2: Block diagram of the VFAT2 chip.

FAST
OR
Trigger
lines
S1...S8

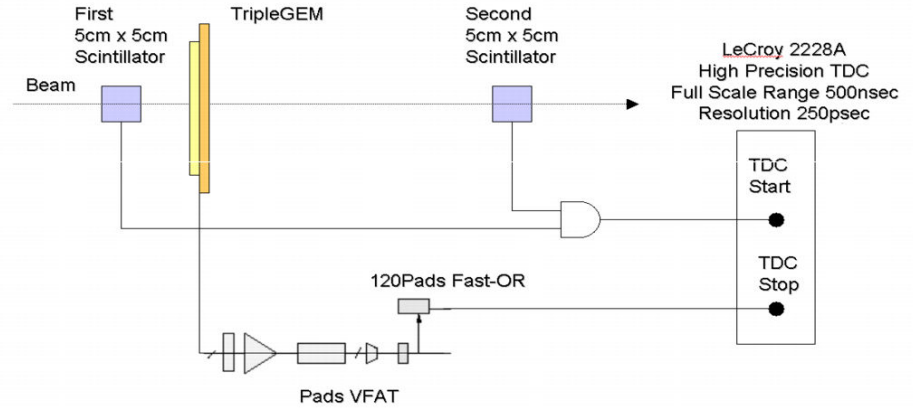
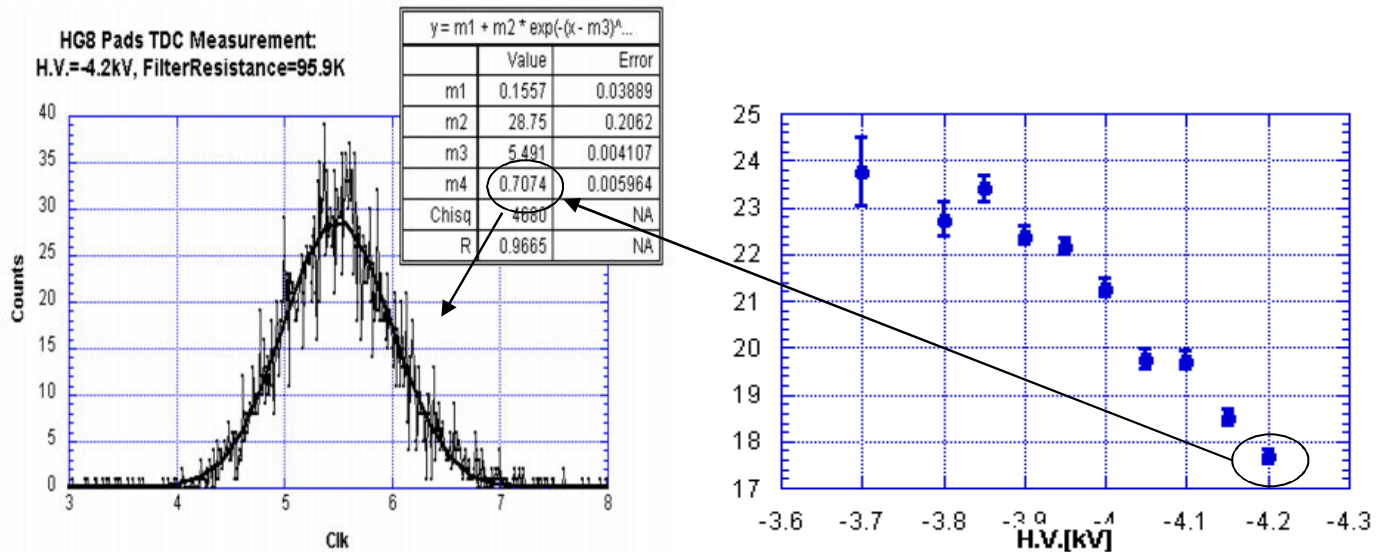


Figure 17: TDC System Setup. For this measurement we used a LeCroy 2228A TDC unit, setting the full scale range to 500ns and using a resolution of 250ps. The coincidence of the discriminated scintillator signals was used as a TDC start signal and the S-bit (trigger output from the VFAT) as the TDC stop signal. In this measurement we have to take into account the we have a clk synchronization step between the comparator and the monostable output inside the VFAT.

Time distribution of the delay between scintillators coincidence and an high level on the s-bit output during a test beam measurements.



The stretching of the monostable (MSPL): very important for not very fast signals

6 The Masked Monostable Block

This block basically consists of a clocked monostable.

Figure 5 shows a block diagram for the channel from the shaper output through to SRAM1.

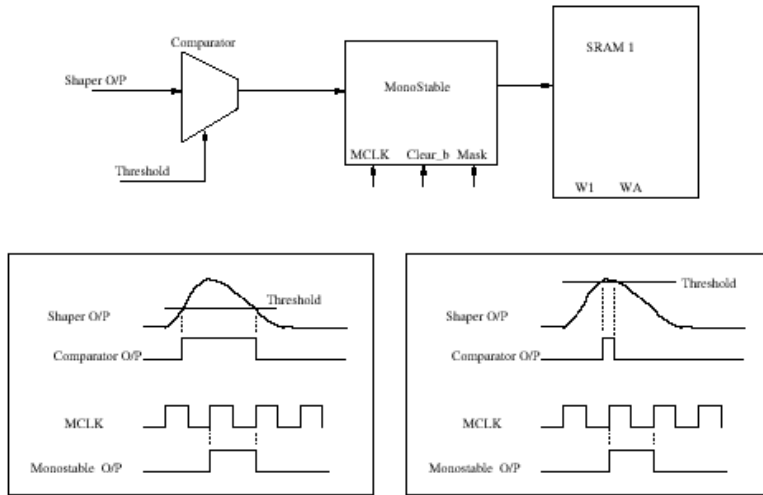
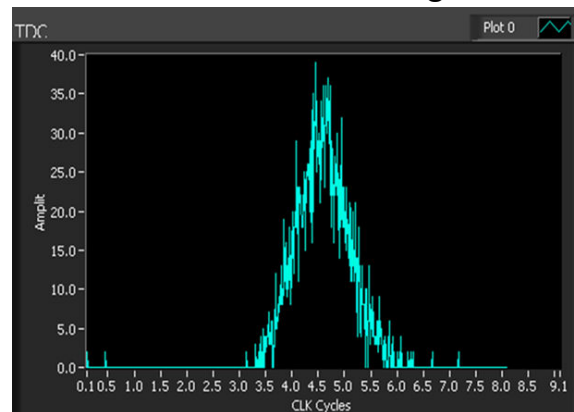


Figure 5: Block diagram of the masked monostable block.

TDC Measurement: Distribution of the threshold crossing time

In this example the first MSPL that guarantees that all the signals are collected is a MSPL of 3CLK [75ns].

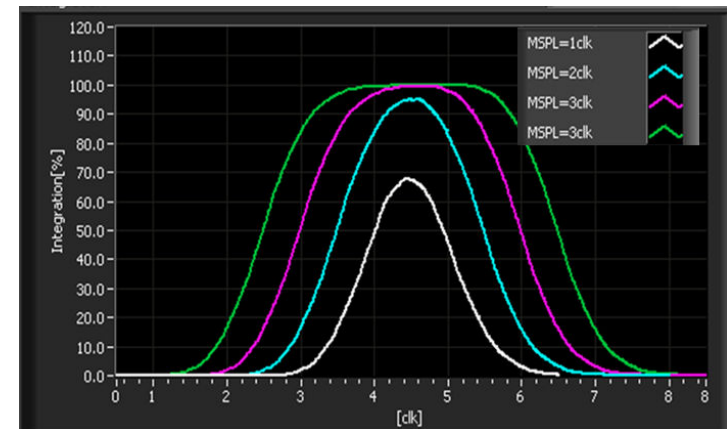


The pulse from the monostable can also be stretched over many clock periods. The length is programmable as in table 19. If the monostable pulse is stretched (to say X clock periods) it is possible that the output of the comparator returns below threshold and a second signal makes the comparator go back over threshold. In this case the monostable output pulse remains high until X clock periods after the last over threshold result from the comparator.

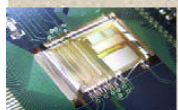
MSPulseLength(2:0)	Function
0 0 0	The MonoStable pulse length = 1 clock period (default).
0 0 1	The MonoStable pulse length = 2 clock periods.
0 1 0	The MonoStable pulse length = 3 clock periods.
0 1 1	The MonoStable pulse length = 4 clock periods.
1 0 0	The MonoStable pulse length = 5 clock periods.
1 0 1	The MonoStable pulse length = 6 clock periods.
1 1 0	The MonoStable pulse length = 7 clock periods.
1 1 1	The MonoStable pulse length = 8 clock periods.

Table 19: Stretching the MonoStable pulse length.

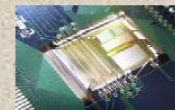
Integration of the previous distribution at different MSPL and Latency



Again for signal like the ones of GEMs detectors:
 When you look at the specs of the VFAT2 you have to take into account aspects concerning your signal properties (if they are different from the silicon ones, you have to rescale the specs. properly).
 One example: the dynamic range and the recovery time.



Simulations of VFAT dynamic range issues



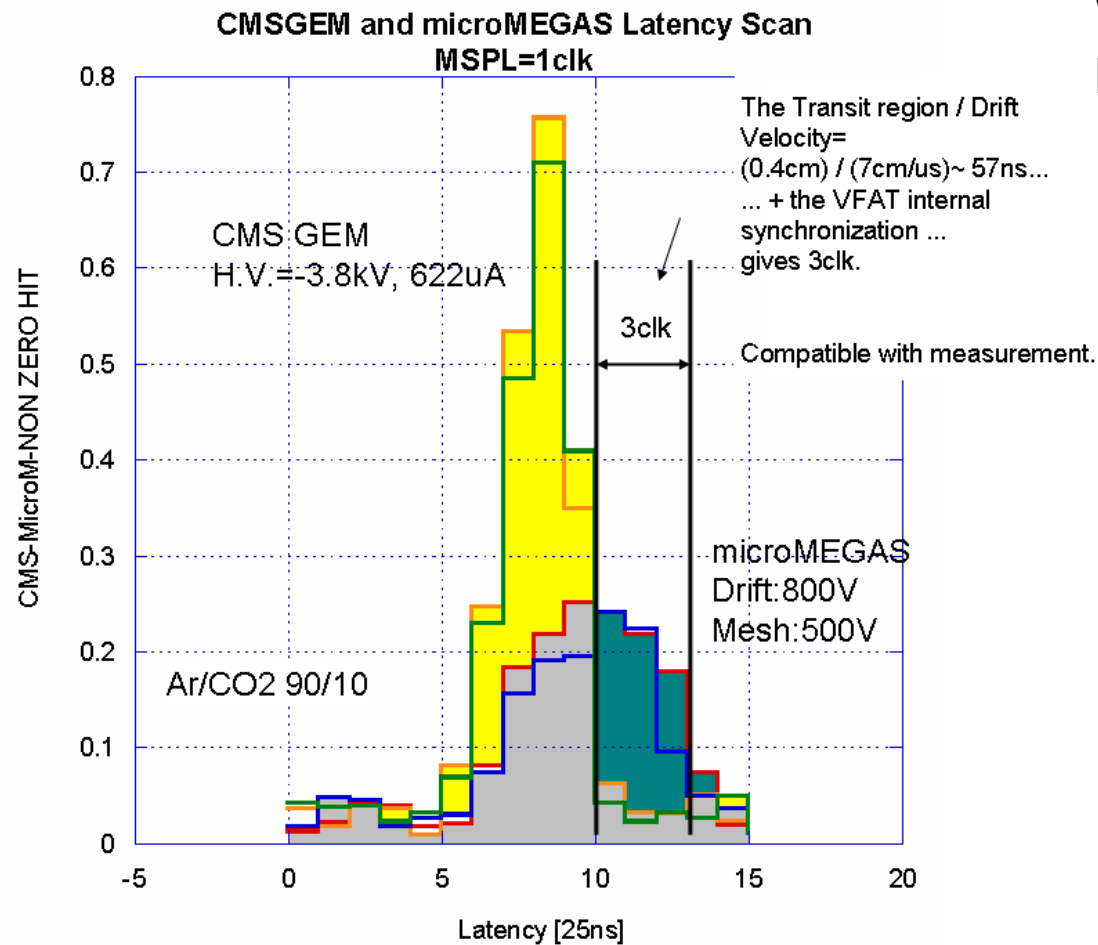
VFAT Dynamic Range for RP	~ 18 fC (5 MIPs)
VFAT Dynamic Range for GEM	35fC to 45fC (~ 2 MIPs pads, ~ 6 MIPs strips)
Threshold range	RP ~ 18 fC Gem ~ 30 fC
Trim-DAC range	~ 40% of dynamic range
Recovery time from very large signals	~1us with a 100fC ideal input signal. ~10us following 10pC of ideal input charge 0.8us for 1pC of GEM input charge

A curiosity more than a measurement:

VFAT2 & MicroMEGAS

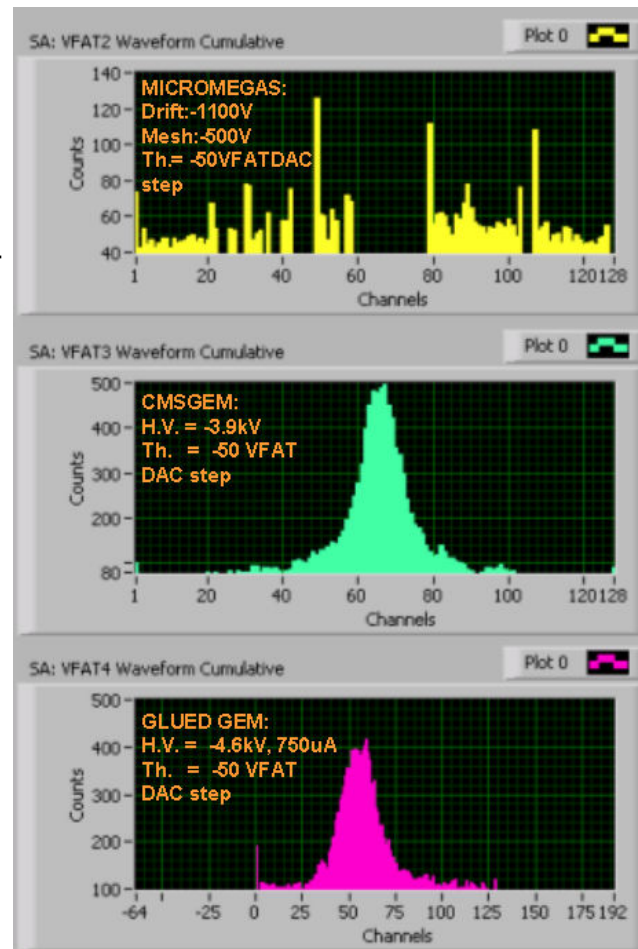
VFAT & MICROME GAS together for the first time.

Faster....



... but dangerous!

We loose the channels in the beam zone after a while!



The channels that disappear in the beam region have been tested directly on the hybrid and they are really dead.

An appropriate protection circuit is needed (the one used for GEM is not enough).

The DAQ system for the VFATs readout
for the RD51 test beam in H4:
A PORTABLE DAQ



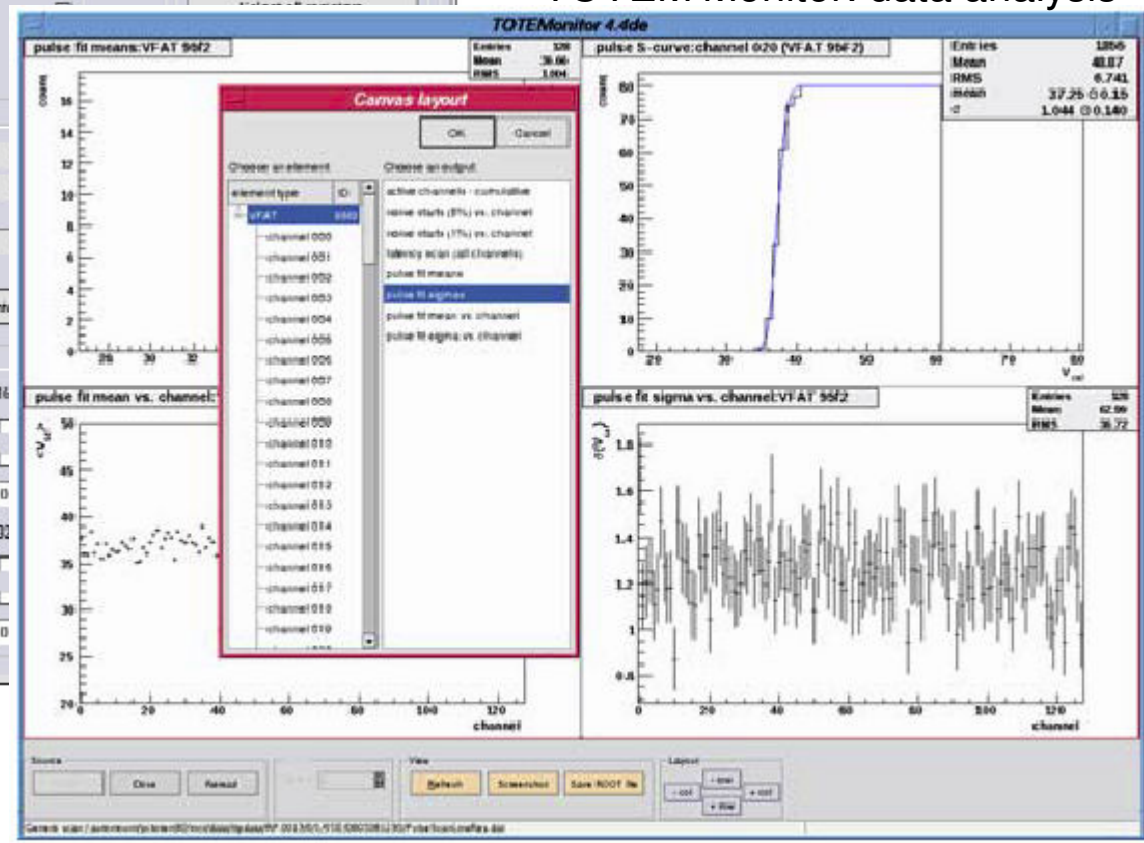
Available software and reference people

VFAT Controller



Access to TTP, VFAT registers and standard acquisition

TOTEM Monitor: data analysis



CMS/TOTEM

TOTEM

Available software and reference people

OS WINDOWS (LabView)

Access to TTP Registers

The screenshot shows the 'Update Trigger Config' window with several tabs: 'TTP Registers', 'VFAT Registers', 'Simple Acquisition', 'Threshold Scan', 'Calibration Pulse', 'Latency Scan', 'Beam Latency Scan', 'Internal Trigger', and 'Fast USB DAQ'. The 'TTP Registers' tab is active, displaying a list of registers (TTP-CTRL1 to TTP-CTRL3) with checkboxes for enabling/disabling various features like 'WFI', 'WFI Protect', 'Internal Trigger', and 'External Trigger'. There are also sections for 'TTP-STATUS', 'TTP-Trigger Latency', and 'TTP-Channel Mask'.

Access to VFATs Registers

The screenshot shows the 'Update Trigger Config' window with the 'VFAT Registers' tab active. It displays configuration options for 'Control Register 0', 'Control Register 1', and 'Control Register 2'. There are sections for 'WriteRead VFAT Registers', 'Update CTRL0', 'Update CTRL1', and 'Update DAC'. The 'DAC-Read' section shows a grid of DAC values for different channels and registers.

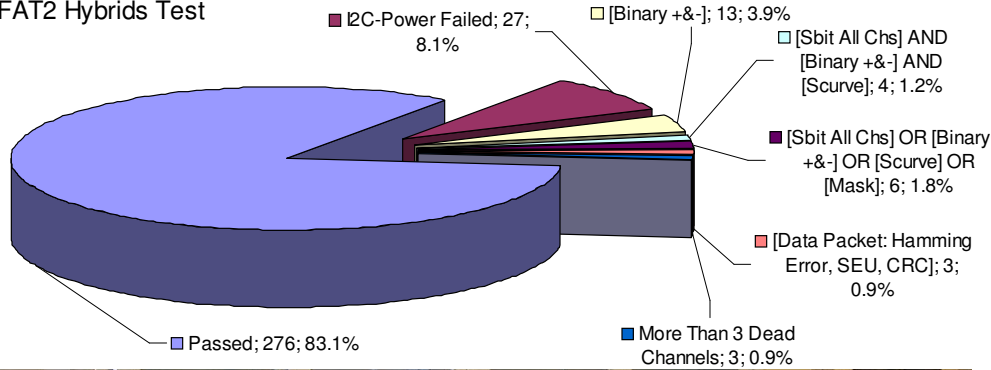
The screenshot shows the 'VFAT Readout Program - v1' window. It features a 'STOP PROGRAM' button at the top. Below it, there are several plots showing 'Counts [%]' versus 'VCAL [VFAT2 DAC step]' for four different channels (VFAT 1, 2, 3, 4). The plots show a distribution of counts across the DAC range. There are also configuration options for 'OP: Start Scan', 'OP: Stop Scan', 'OP: Actual Number of Trigger Collected', and 'OP: VFATs Channel'. A 'Channel Registers' table is visible at the bottom.

CERN
TERA
INFN Pisa/Siena
GDD group

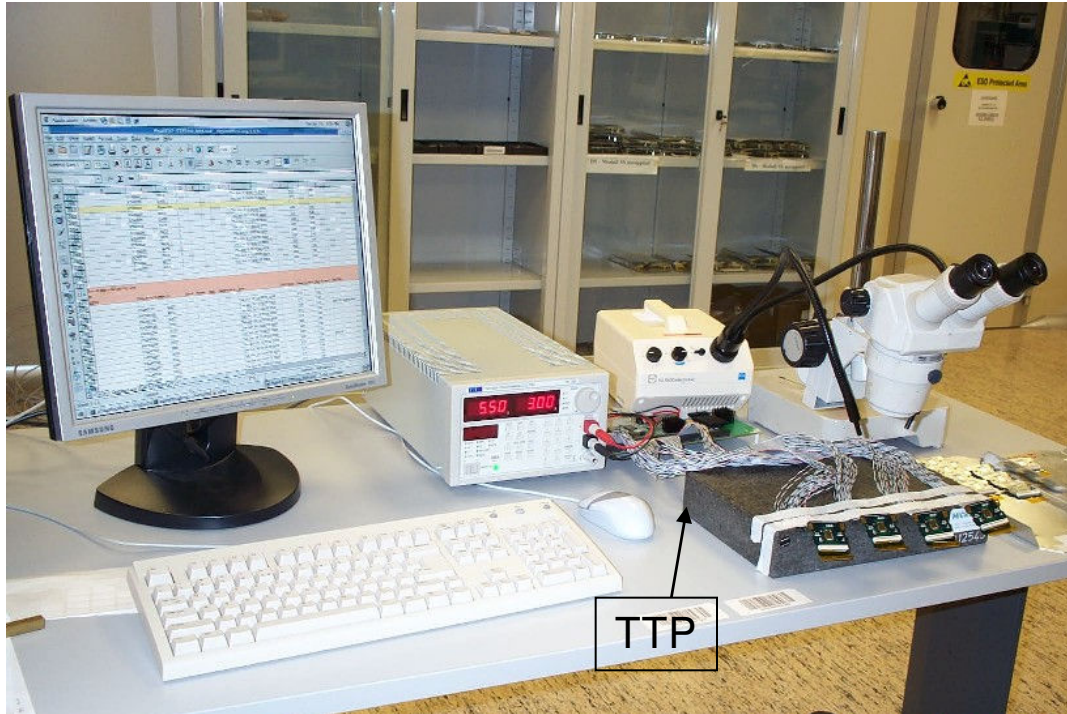
Automated
Measurements:
Threshold Scan
Calibration Pulse Scan
Latency Scan
Simple Acquisition ...
and what you want (more
or less)

TTP: if needed, it can be used also as a tool for an automated chip quality test (Linux OS).

Pads VFAT2 Hybrids Test



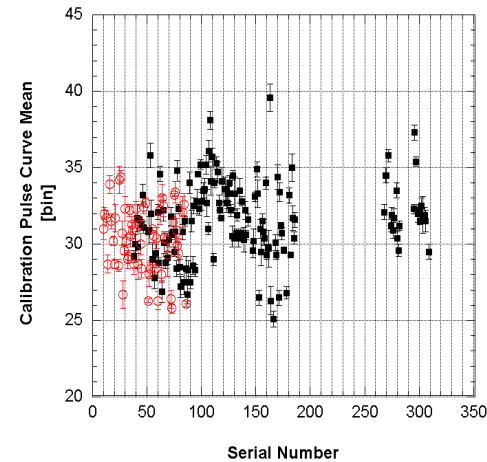
T2 hybrids test result for a bunch of ~300 chips



TTP

Hybrids test set up in the INFN Pisa bonding lab.

High Resolution Calibration Scan: Test on 202 Hybrid That have passed the standard test



PADS AND STRIPS

	Mean HR	err Mean HR
Minimum	25.1	0.1
Maximum	39.599998	1.4
Sum	6304.6	110.3
Points	202	202
Mean	31.210091	0.54802661
Median	31.25	0.5
RMS	31.307683	0.58648309
Std Deviation	2.4581229	0.24086483
Variance	6.0423682	0.057919559
Std Error	0.17295292	0.018932118
Skewness	0.12048595	0.58655733
Kurtosis	0.28306784	0.3335284

PADS

	Mean HR	err Mean HR
Minimum	25.1	0.1
Maximum	39.599998	1.2
Sum	4543.2	77.400001
Points	144	144
Mean	31.55	0.5375
Median	31.55	0.5
RMS	31.648361	0.585828
Std Deviation	2.5019432	0.23381153
Variance	0.2597199	0.054667832
Std Error	0.20849527	0.018449264
Skewness	0.14105216	0.58028819
Kurtosis	0.25895575	0.17959725

STRIPS

	Mean HR	err Mean HR
Minimum	25.798999	0.1
Maximum	34.400002	1.4
Sum	1781.4	32.9
Points	58	58
Mean	30.368966	0.58724138
Median	30.5	0.5
RMS	30.443184	0.62214887
Std Deviation	2.1427322	0.25778287
Variance	4.5913015	0.066451902
Std Error	0.28126453	0.033848527
Skewness	-0.21778102	0.55919822
Kurtosis	-0.54006727	0.49198429

Calibration Scan result for a bunch of ~200 chips automatically measured during the testing procedure

Well, I know that we like to see particles and not to test chips!!! But if you have to do it, you can.

thE enD

Feel free to contact me

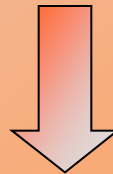
oliveri4@unisi.it

(if you can read my address!?!)

If you need it, you could find documents about VFAT2 and TTP on my public dfs area:

<https://dfs.cern.ch/dfs/Users/e/eoliveri/Public/RD51-4thCM/>

backUp



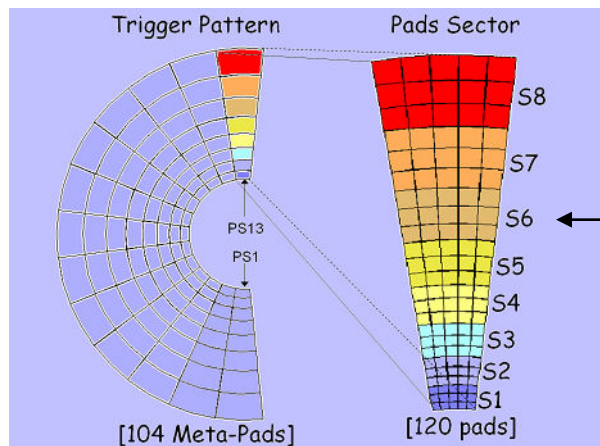
The VFAT2 Trigger: the available patterns

TrigMode(2)	TrigMode(1)	TrigMode(0)	Function
0	0	0	No Trigger (default)
0	0	1	One sector (S1)
0	1	0	Four sectors (S1 to S4)
0	1	1	Eight sectors (S1 to S8)
1	X	X	GEM mode (S1 to S8 as defined in table 10)

Groups of consecutive channels or ...

GEM mode channel assignment					
Sector	Channel assignment to sector				
S1	4	28	52	76	100
	5	29	53	77	101
	6	30	54	78	102
S2	7	31	55	79	103
	8	32	56	80	104
	9	33	57	81	105
S3	10	34	58	82	106
	11	35	59	83	107
	12	36	60	84	108
S4	13	37	61	85	109
	14	38	62	86	110
	15	39	63	87	111
S5	16	40	64	88	112
	17	41	65	89	113
	18	42	66	90	114
S6	19	43	67	91	115
	20	44	68	92	116
	21	45	69	93	117
S7	22	46	70	94	118
	23	47	71	95	119
	24	48	72	96	120
S8	25	49	73	97	121
	26	50	74	98	122
	27	51	75	99	123

Table 9: TrigMode functions.



... the GEM mode channel assignment that in the TOTEM T2 Triple GEM detector gives this trigger pattern

Table 10: Sector configuration for the GEM mode.