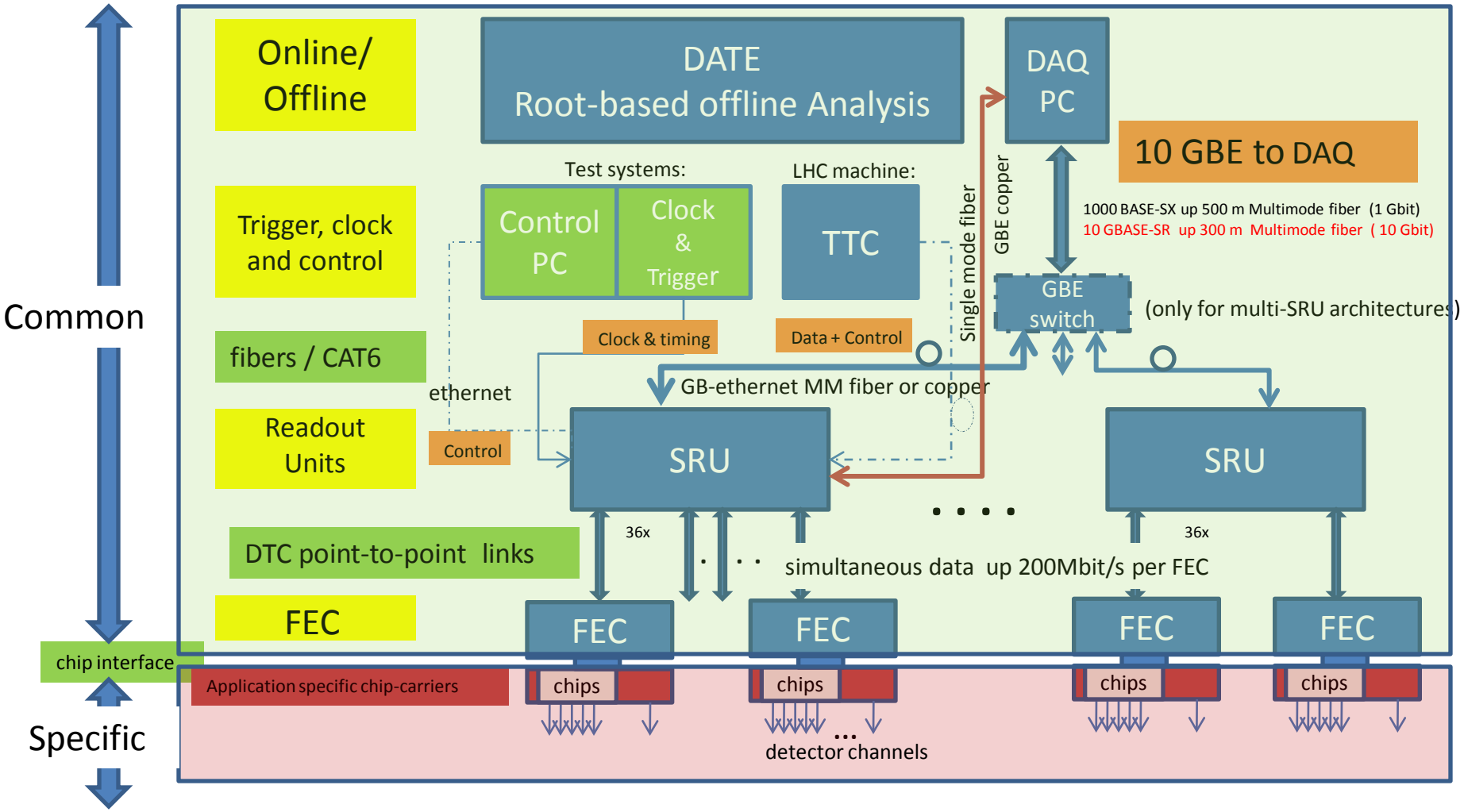
Status of the RD51 Scalable Readout System (SRS)

November 2009

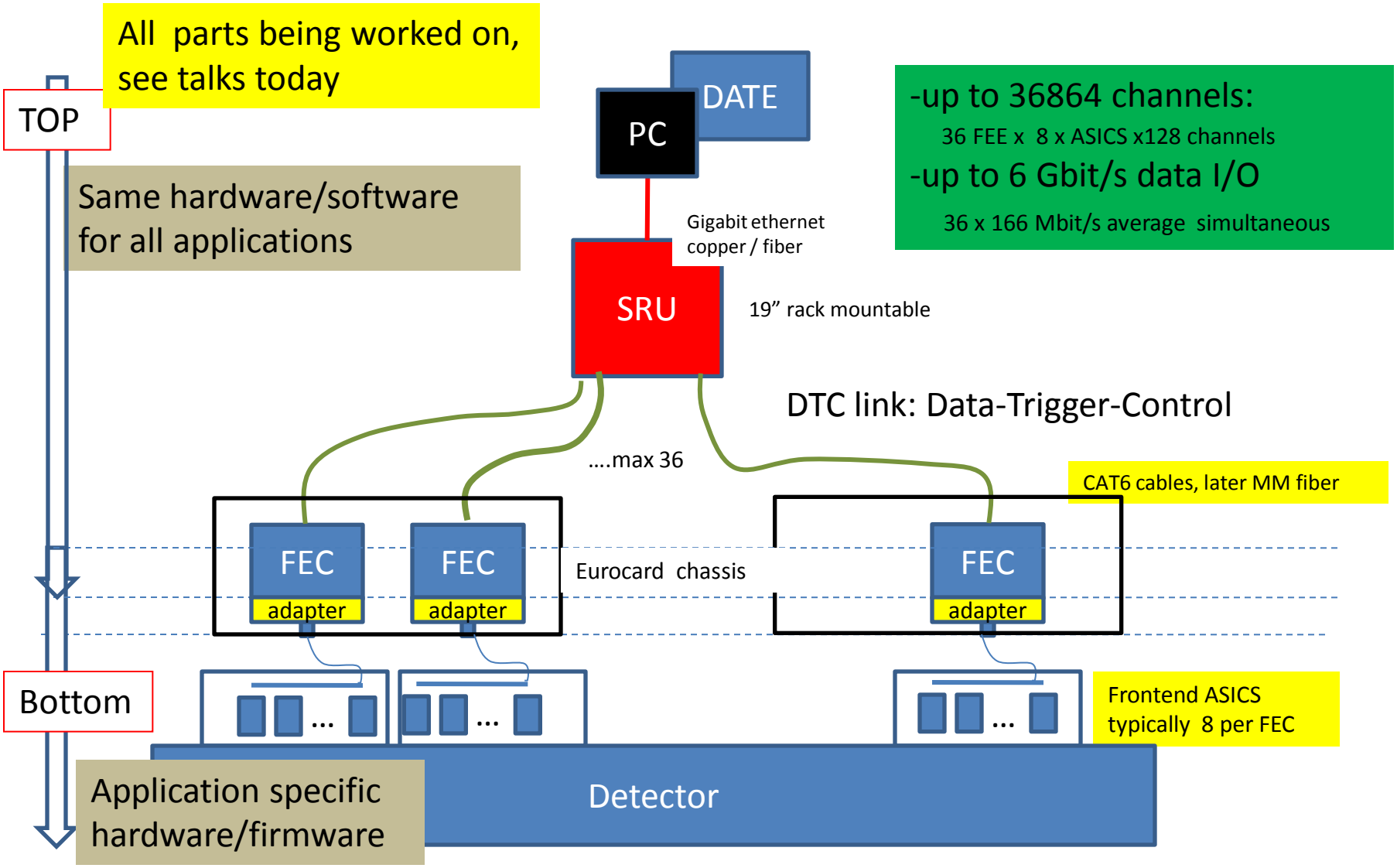
Hans Muller CERN PH

Teams involved: NEXT Collaboration, DATE team CERN, RD51-WG5 team CERN
Huazhong Normal University Wuhan, ATLAS MaMa (MiroMega)
PCB shop CERN ..... more teams invited

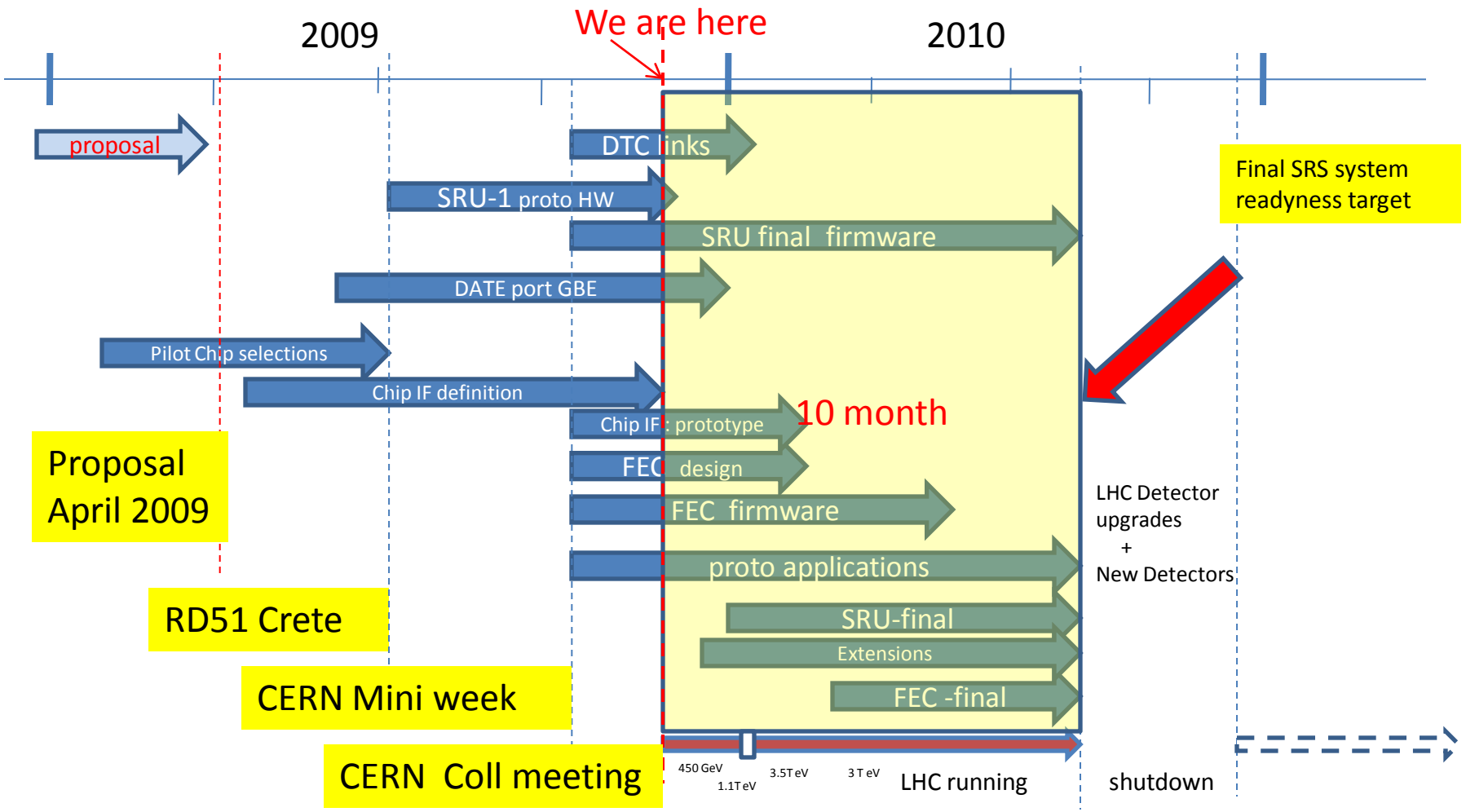
SRS proposal revisited



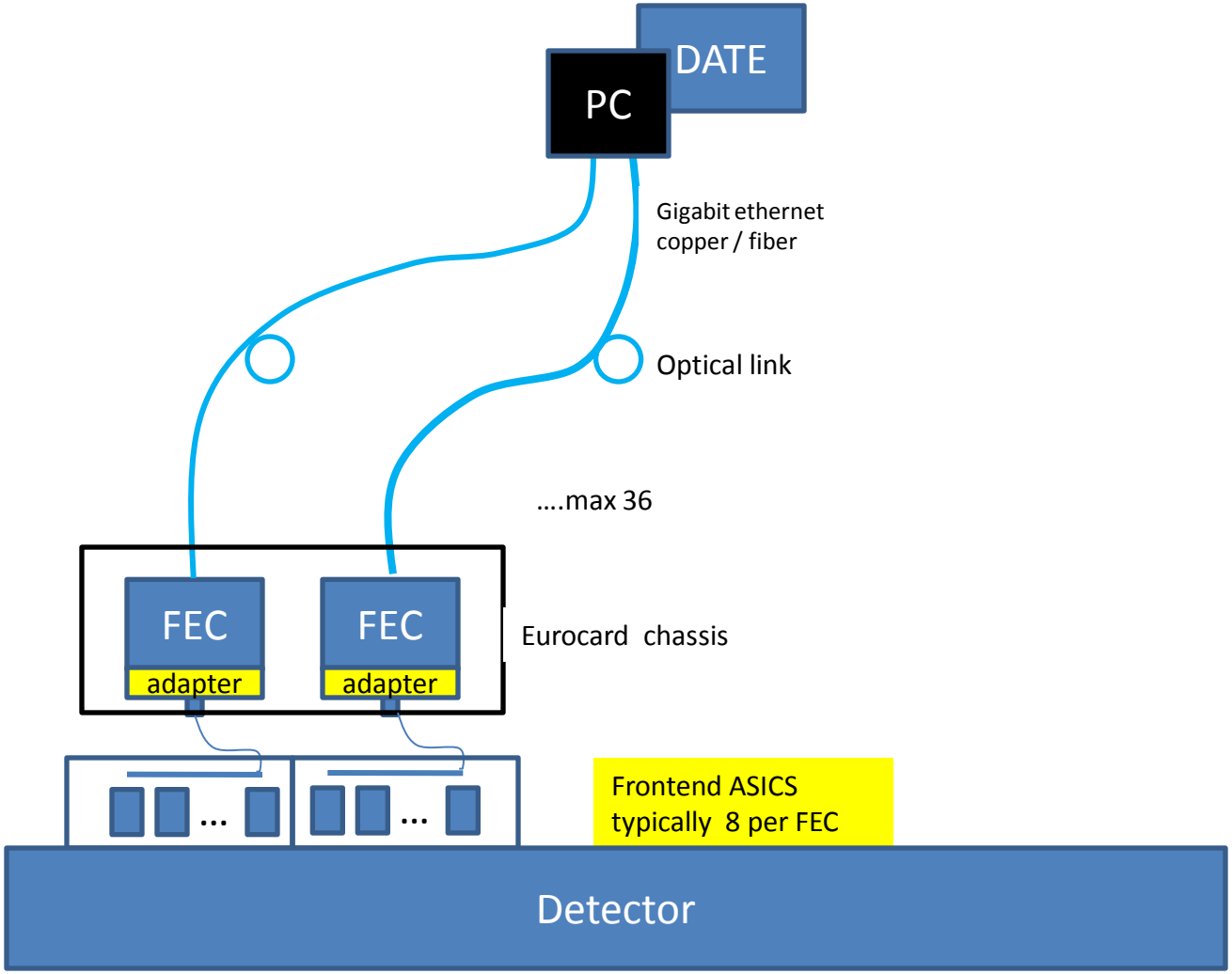
First target 2009: single SRU system 1Gbit



updated SRS project timing
Nov. 23 2009 = @startup of LHC !

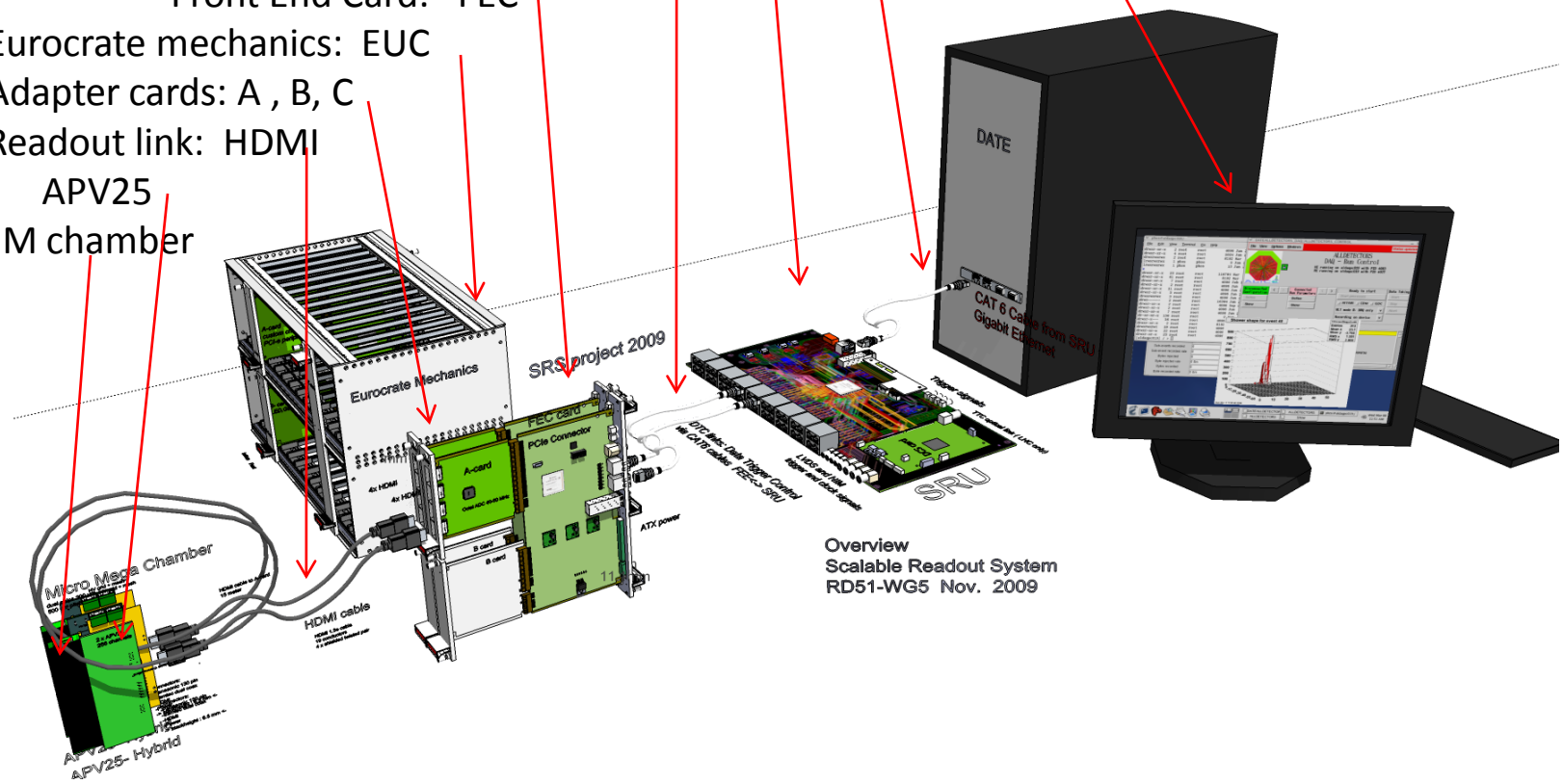


Prototype test system
1 or 2 FEC cards directly connected to DAQ



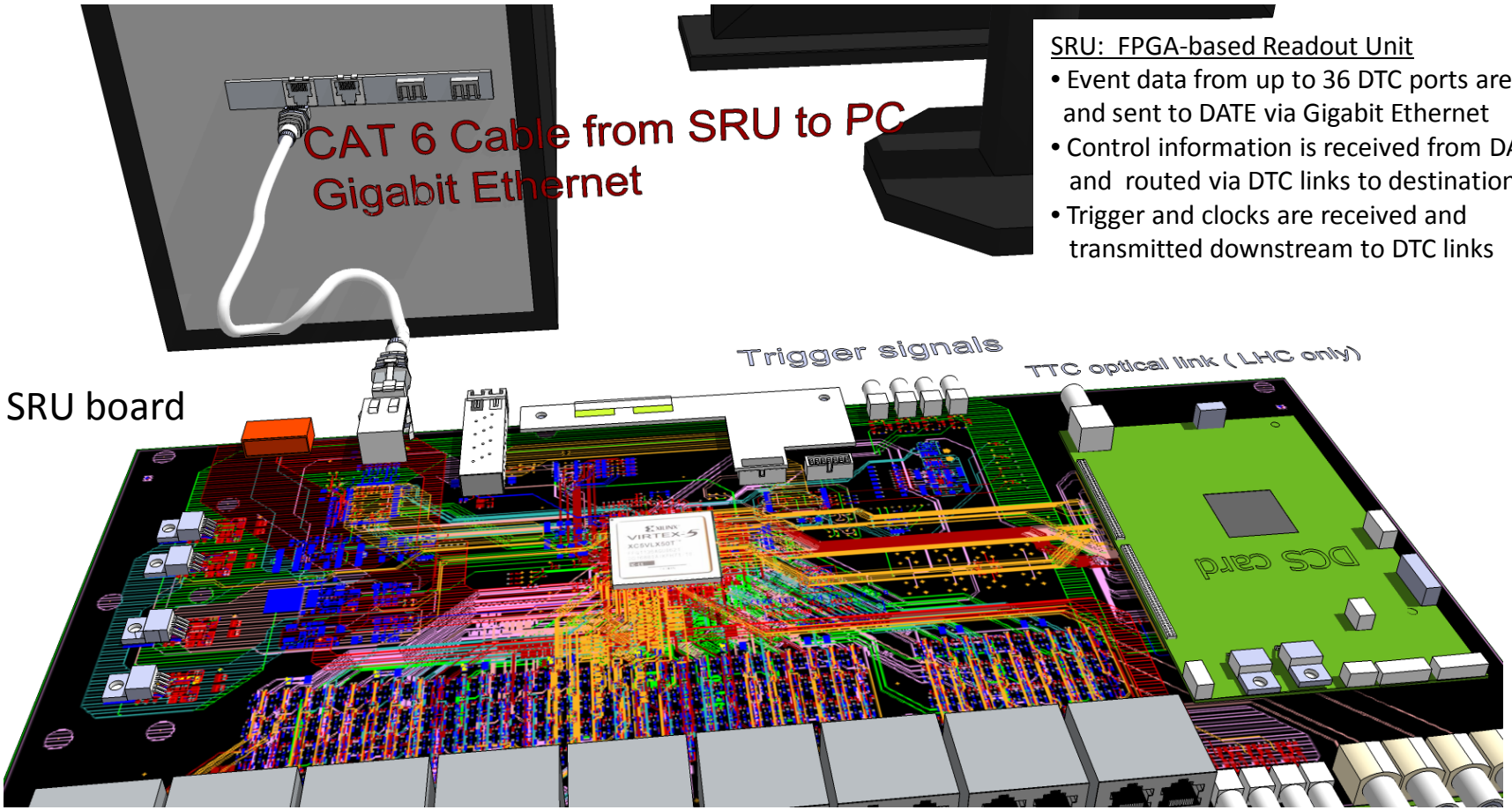
SRS 2009 Overview

Readout DAQ System: DATE
Readout links: (10) Gigabit Ethernet
Large systems link concentrator: SRU
Data Trigger Control links: DTC
Front End Card: FEC
Eurocrate mechanics: EUC
Adapter cards: A , B, C
Readout link: HDMI
Chip carrier: APV25
Detector: MM chamber



(10) Gigabit links to DATE

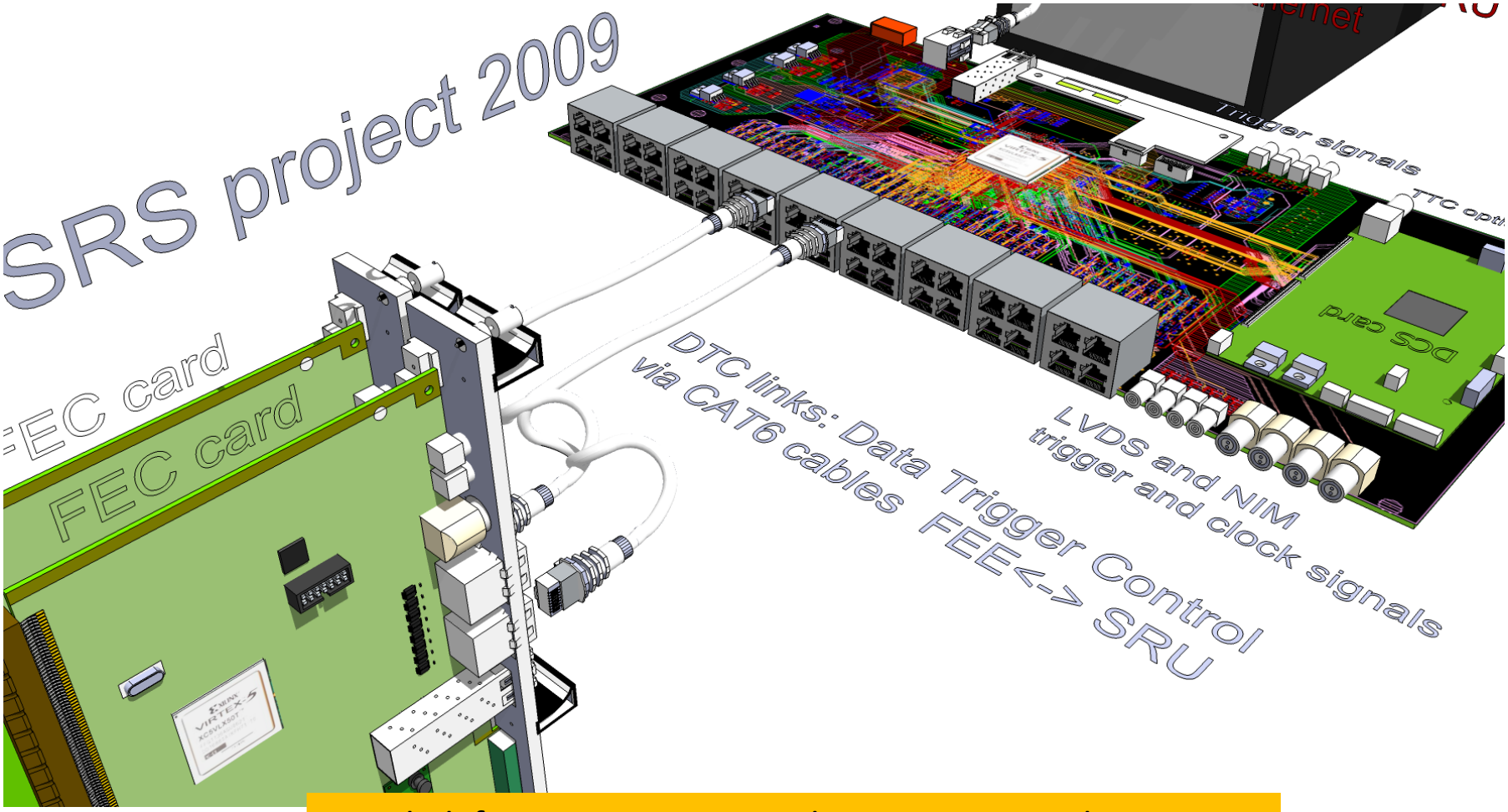
See talks today by Fillipo Costa (CERN DATE team) and Luis Diaz (NEXT collaboration)



SRU: FPGA-based Readout Unit

- Event data from up to 36 DTC ports are formatted and sent to DATE via Gigabit Ethernet
- Control information is received from DATE / DCS and routed via DTC links to destination
- Trigger and clocks are received and transmitted downstream to DTC links

DTC links from SRU to FEC



DTC link firmware on FEC and SRU: CCNU Wuhan
See talk today by Huazhong Normal University, Wuhan

FEC card

WG5 CERN:

Final outlines and connectors

3D models available on request

NEXT collaboration, Valencia:

1st FEC card design ongoing

finalization expected 12 / 09

PCIe connector pinout specified

ATX power specified

On- board power hybrids

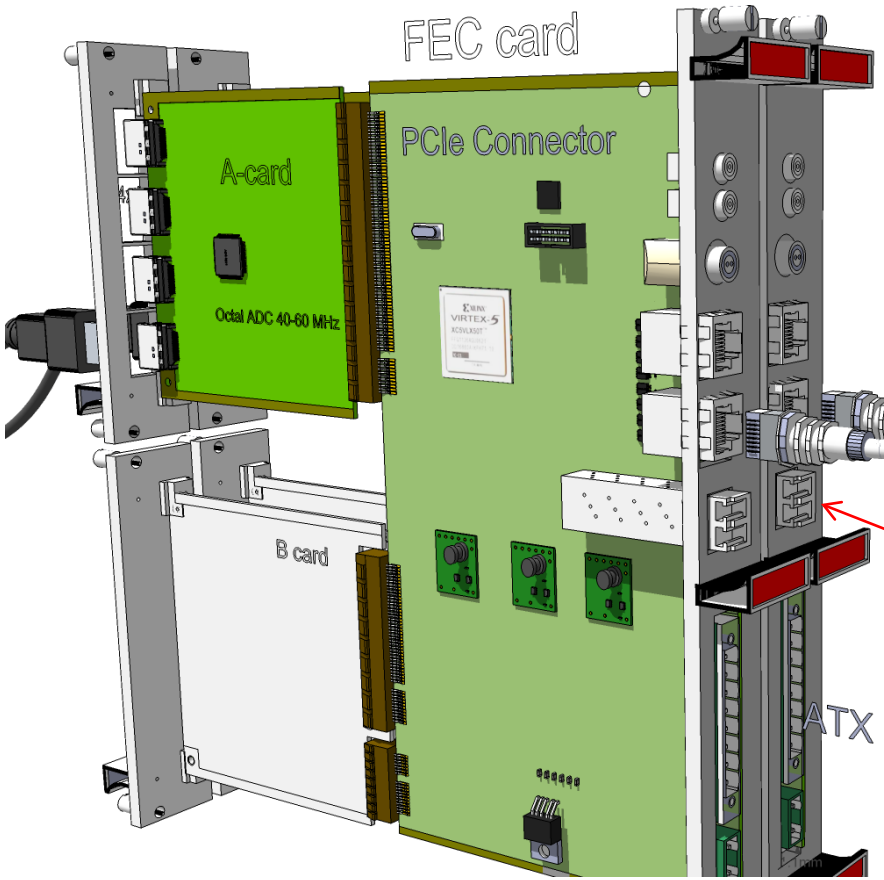
=== Xilinx-Virtex-5 LX50T

=== DDR memory 2 Gbit

=== 1000BASE-T SFP

=== Flash

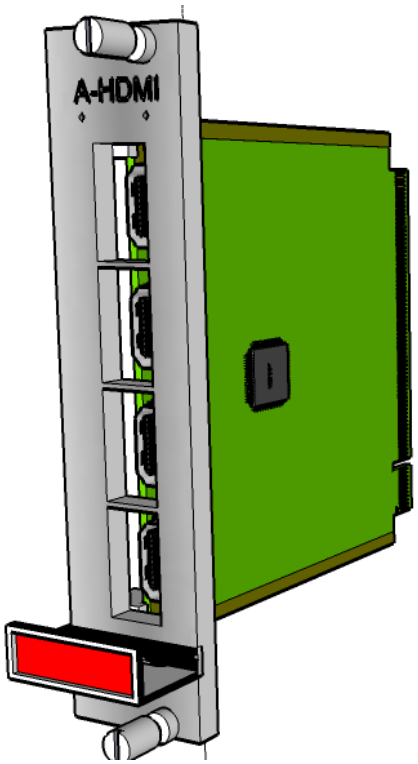
=== PCIe x8



DTC links
(CAT 6 cables)

Optical Gigabit Ethernet link
for direct operation with DATE
(small test system w.out SRU)

APV25 adapter (A card)



Readout of APV25 chip on remote hybrid

-> use 19 wire HDMI cable , 4 shielded twisted pairs
connect 4 hybrids with 2 APD25 each
use noise immune current receivers on A card

Digitize analogue data stream from APV25 chips

up to 8 APV25 can be connected t one A card

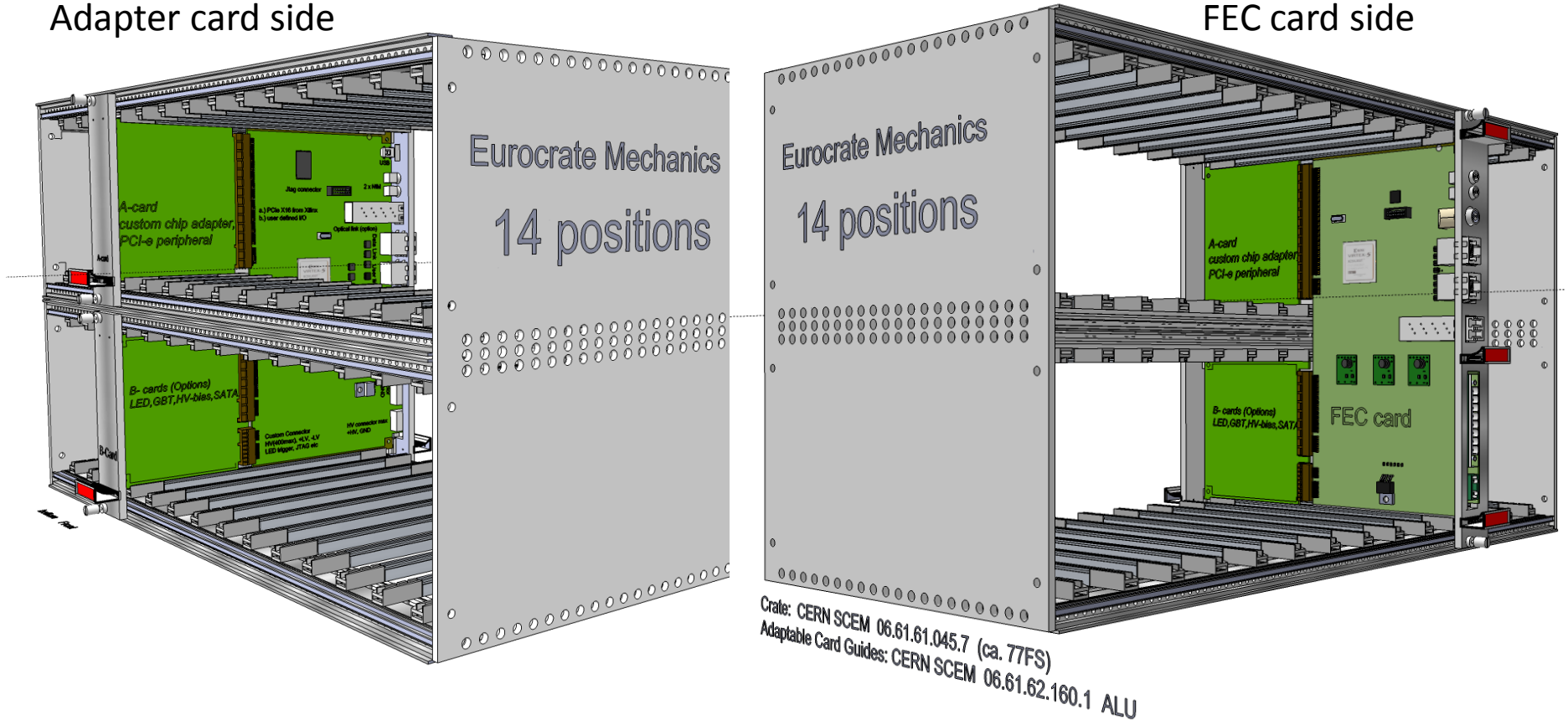
-> use octal ADC, 12 bit, 40 .. 65 MHz (ADS5281)
proven technology from previous projects
8 x serial LVDS outputs from ADC @ 280 MHz
deserializer in Vittex-5 FPGA on FEC card
high speed connectivity via PCIe x8 connector (8 lanes 2 Gbit/s)

See talk today by S. Martoiu , RD51 CERN

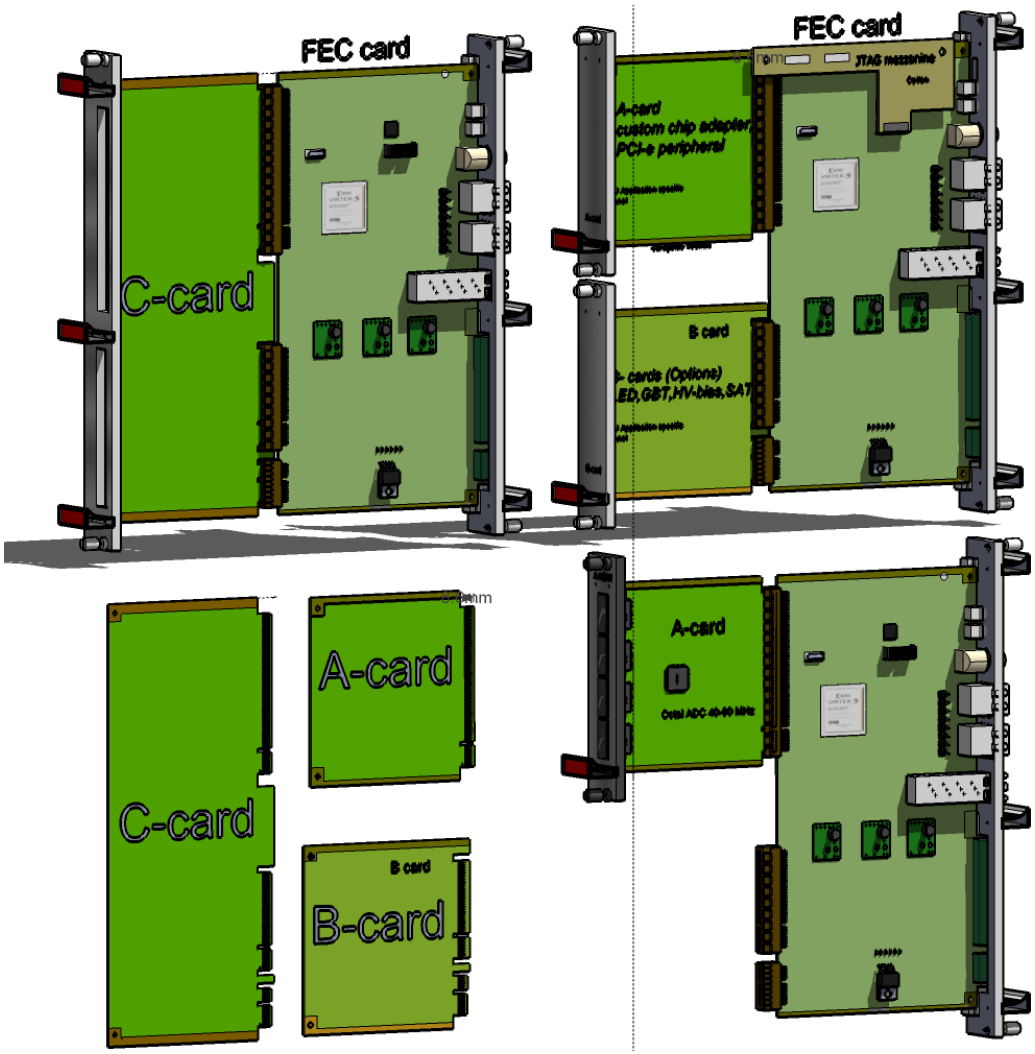
Eurocrate mechanics

Adapter card side

FEC card side



SRS adapter card “Lego”



All dimensions and system-connector are defined now, 3D model avaliable on request

A cards: chip readout adapter

B cards: small size Extensions

NEW:

C cards: large size extensions

1st card will be A card for APV25

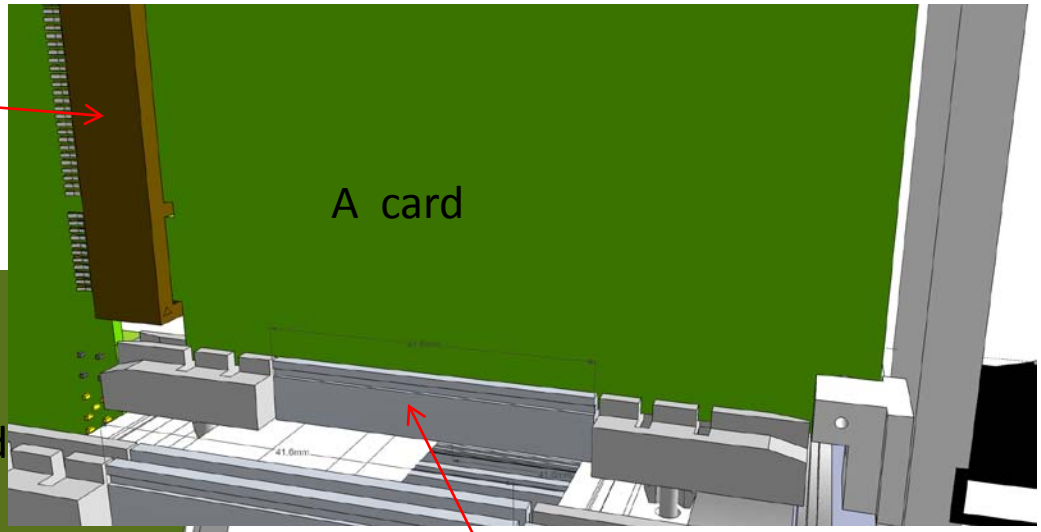
All can in principle be mixed in one EU crate

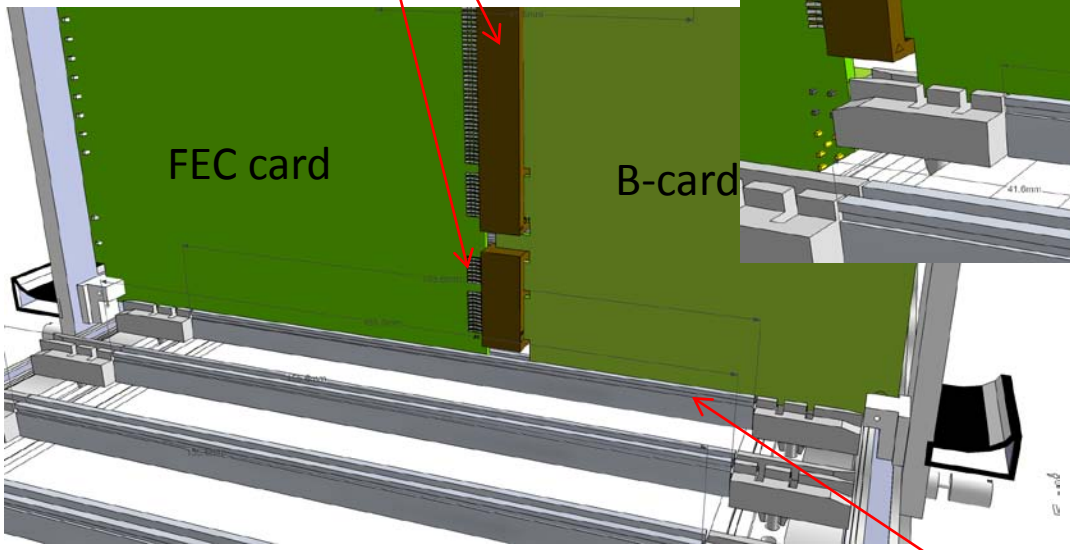
Extensions to be worked on:

- **Programmable HV for APD, SiPMs etc**
- **Programmable LED pulsers**
- **Adapters for subsystems like GBE or triggerless systems**

Card guides
Adapter card connectors

PCIe straddle-mount connectors
= off shelf from distributors
PCIe X16 connector
PCIe X8 connector
PCIe X1 connector

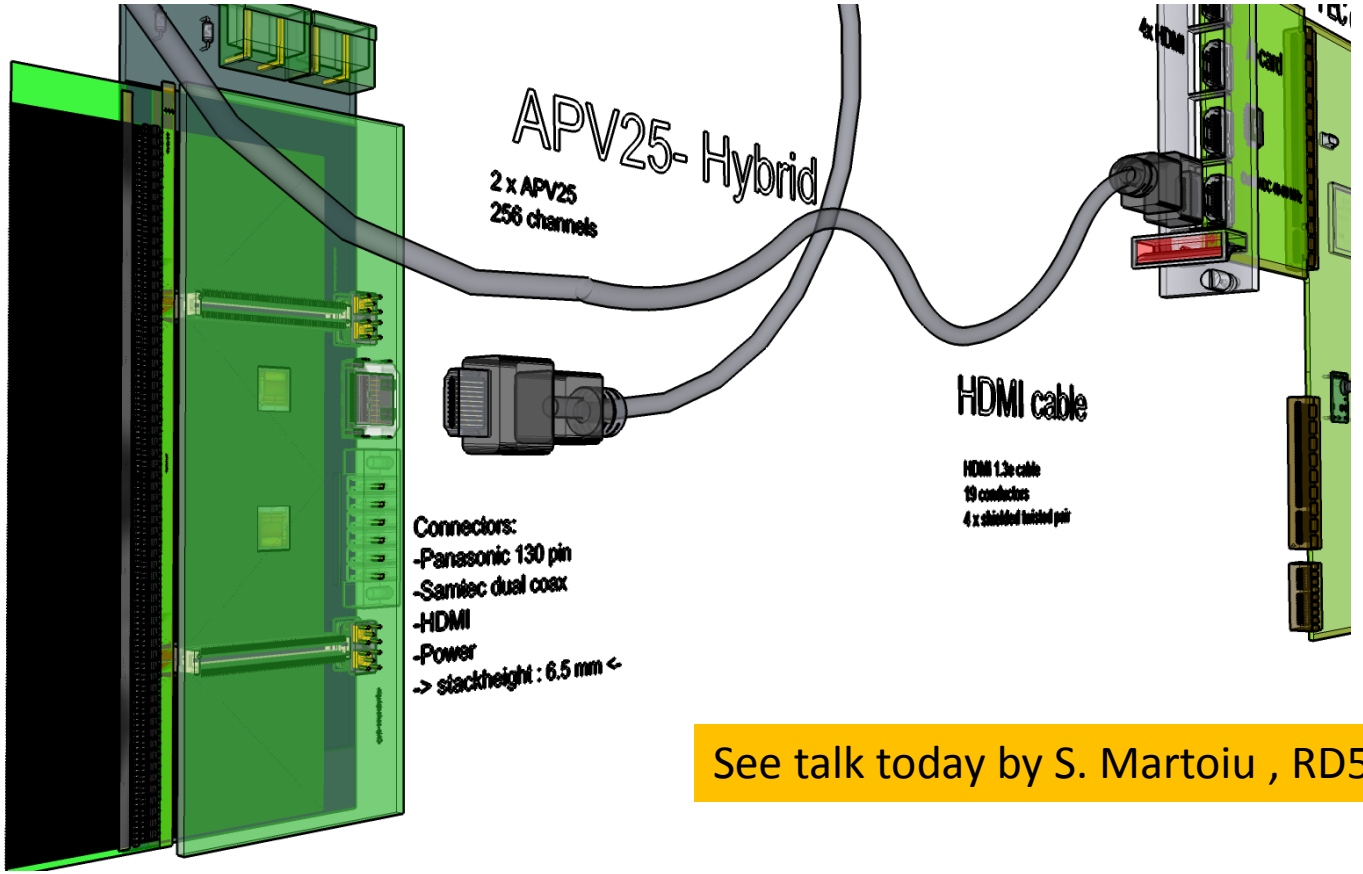




Adaptable-lenght ALU card guides: long 155.6 mm, short 41.6 mm
(will be ordered for RD51 by CERN store)

Detector Readout Cable (DRC)

DETECTOR
MM chamber



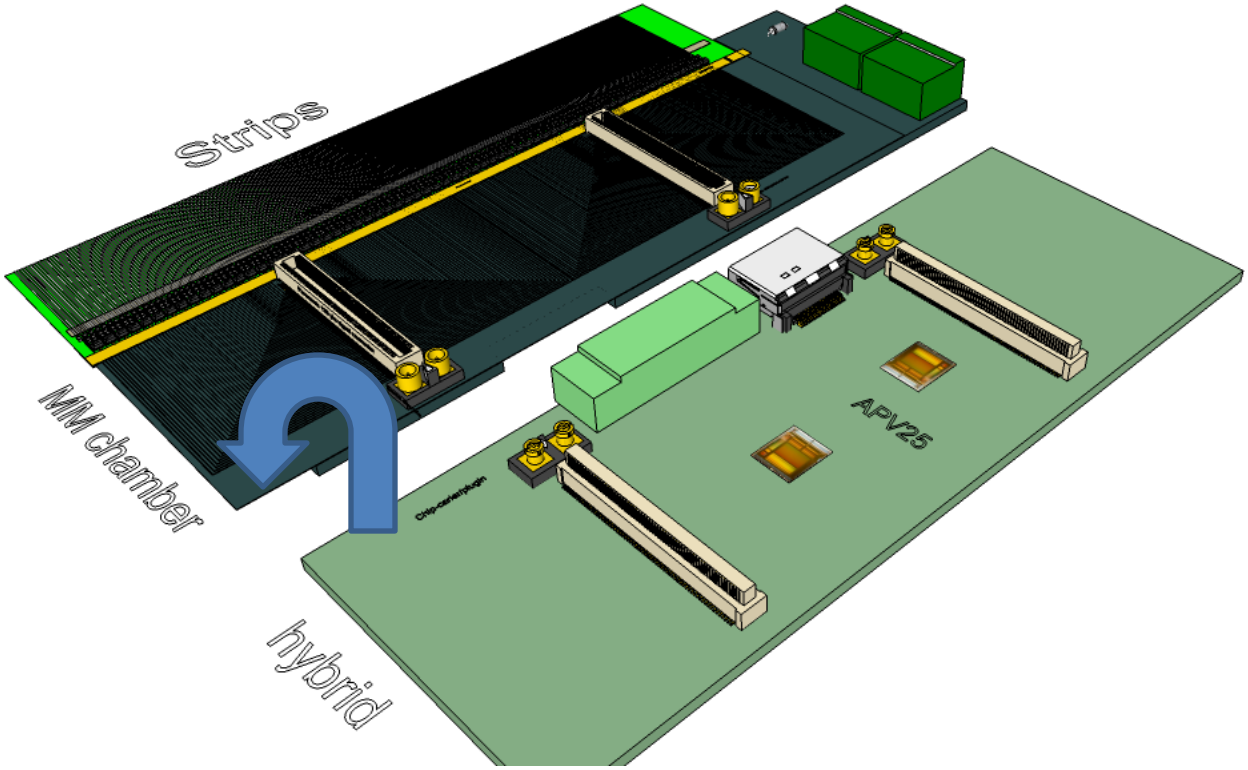
Adapter
card A

FEC card

See talk today by S. Martoiu , RD51 CERN

Chip carrier (hybrid for APV25)

Hybrid plugin concept



Chip hybrid plugs in to edge of MM chamber

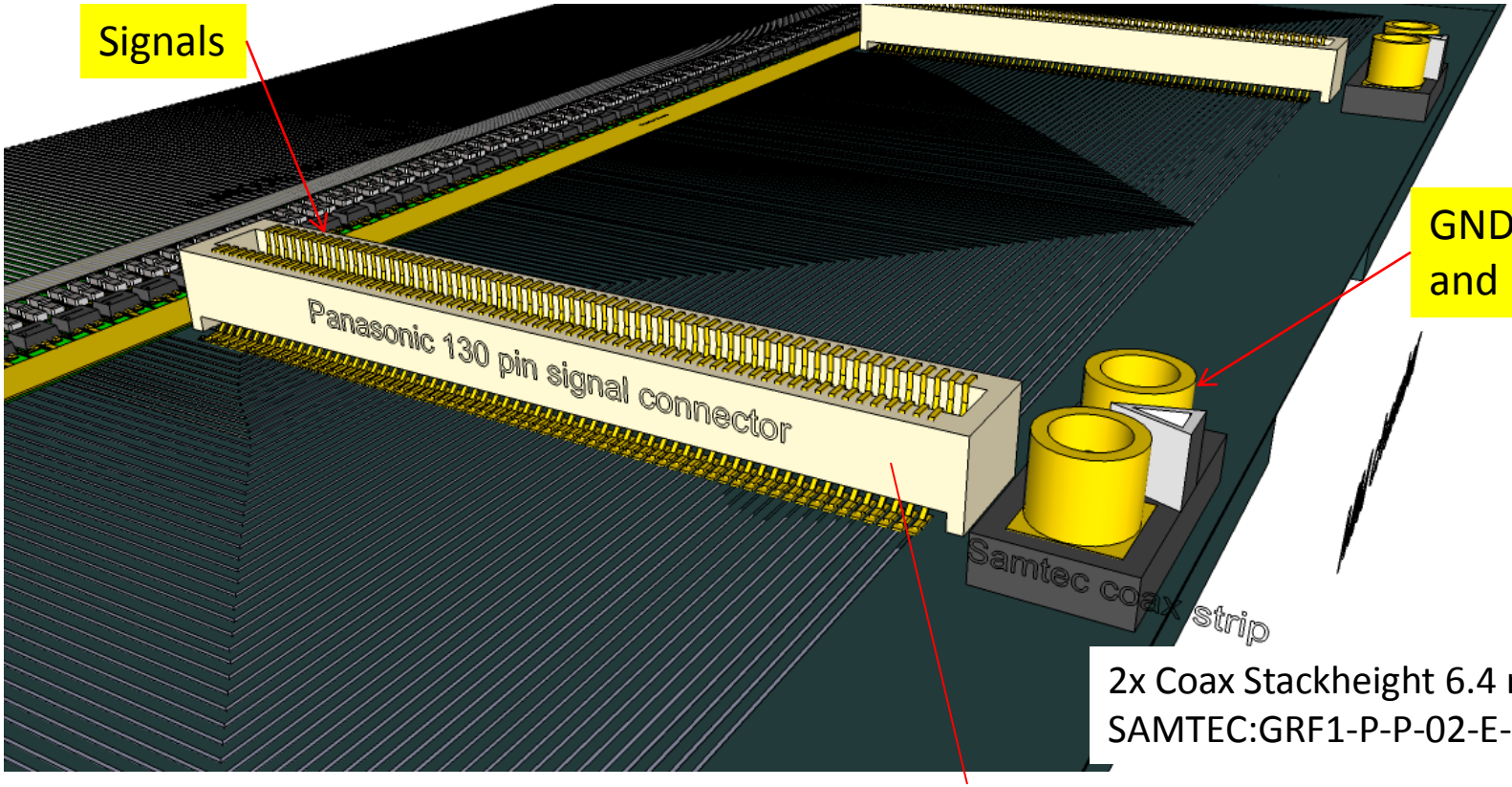
Chip hybrid defined by

- given surface/ channels
- LV connector
- Signal connector
-Readout connector
- GND and pickup connector

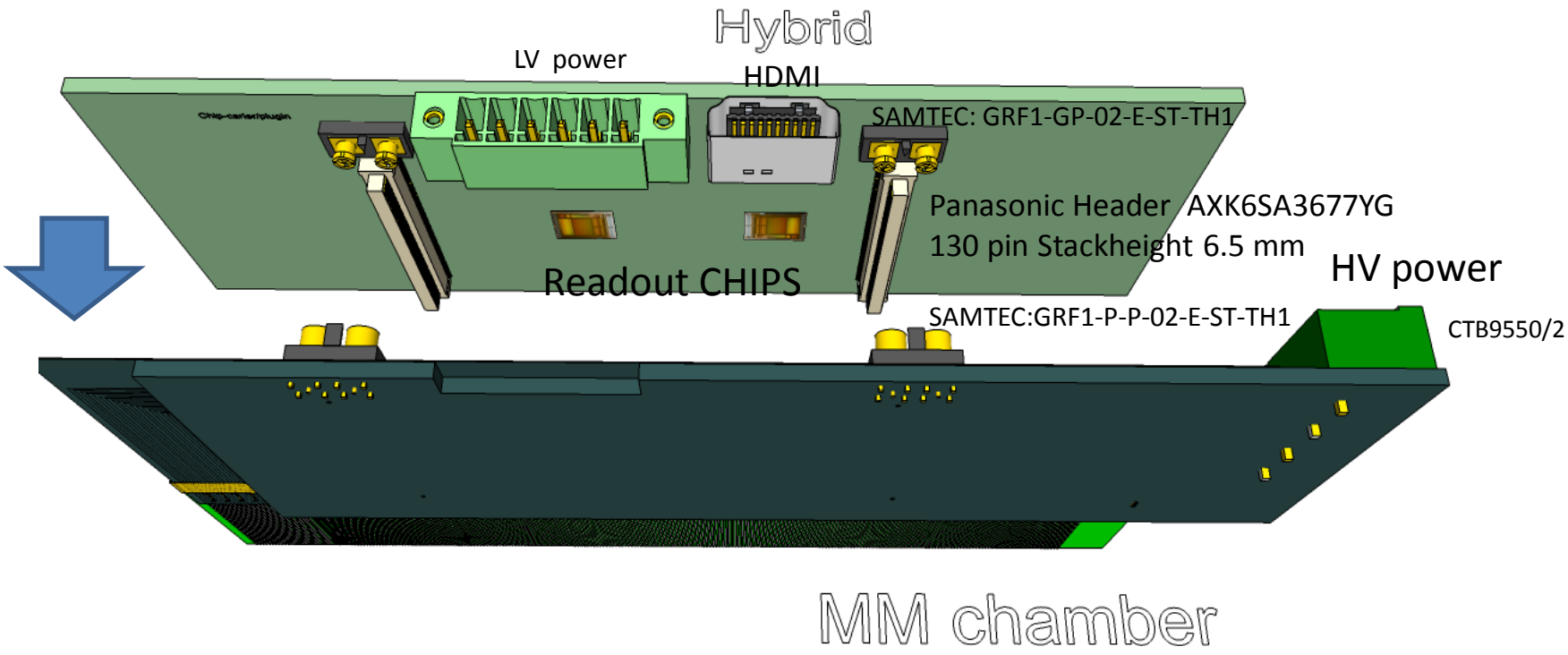
On chamber:

-HV connectors + filters
-ESD protection diodes
-Anode resistors
-Chamber ground

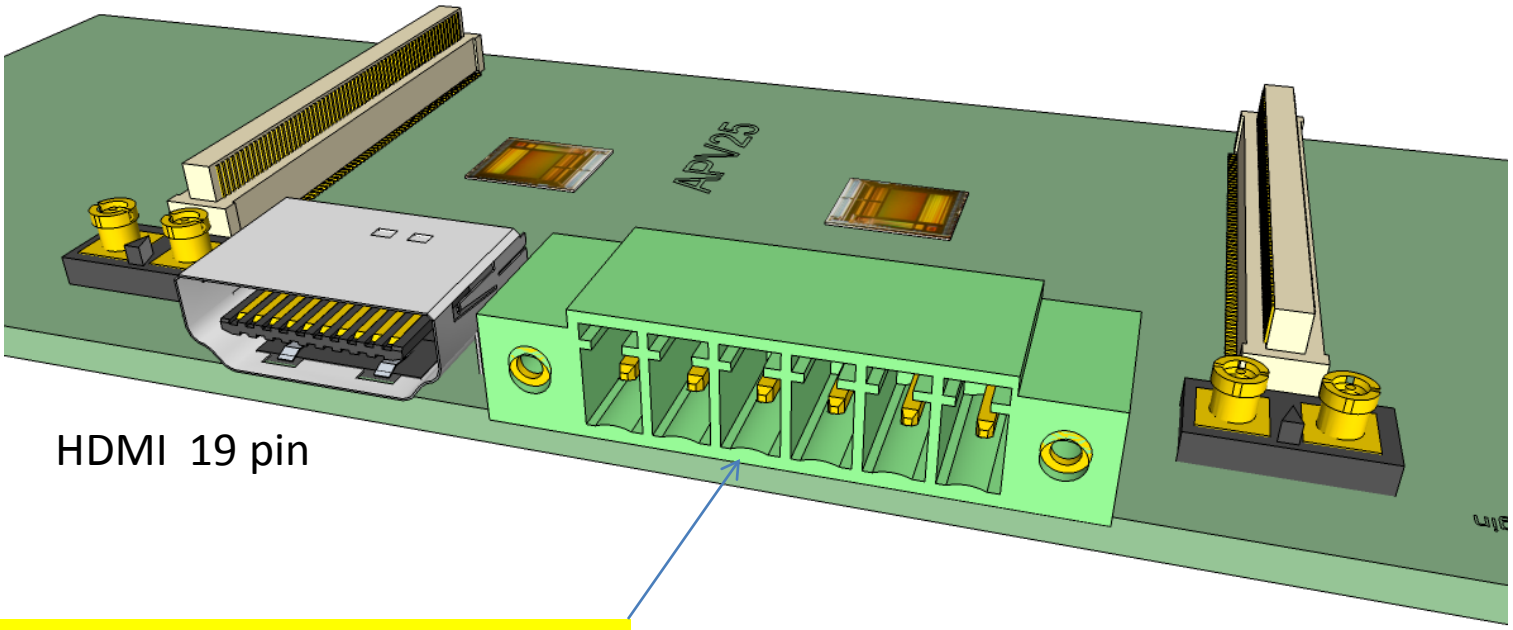
Connectors on chamber



Chip hybrid
plugs on 5cm chamber edge



Hybrid card Power connector



HDMI 19 pin

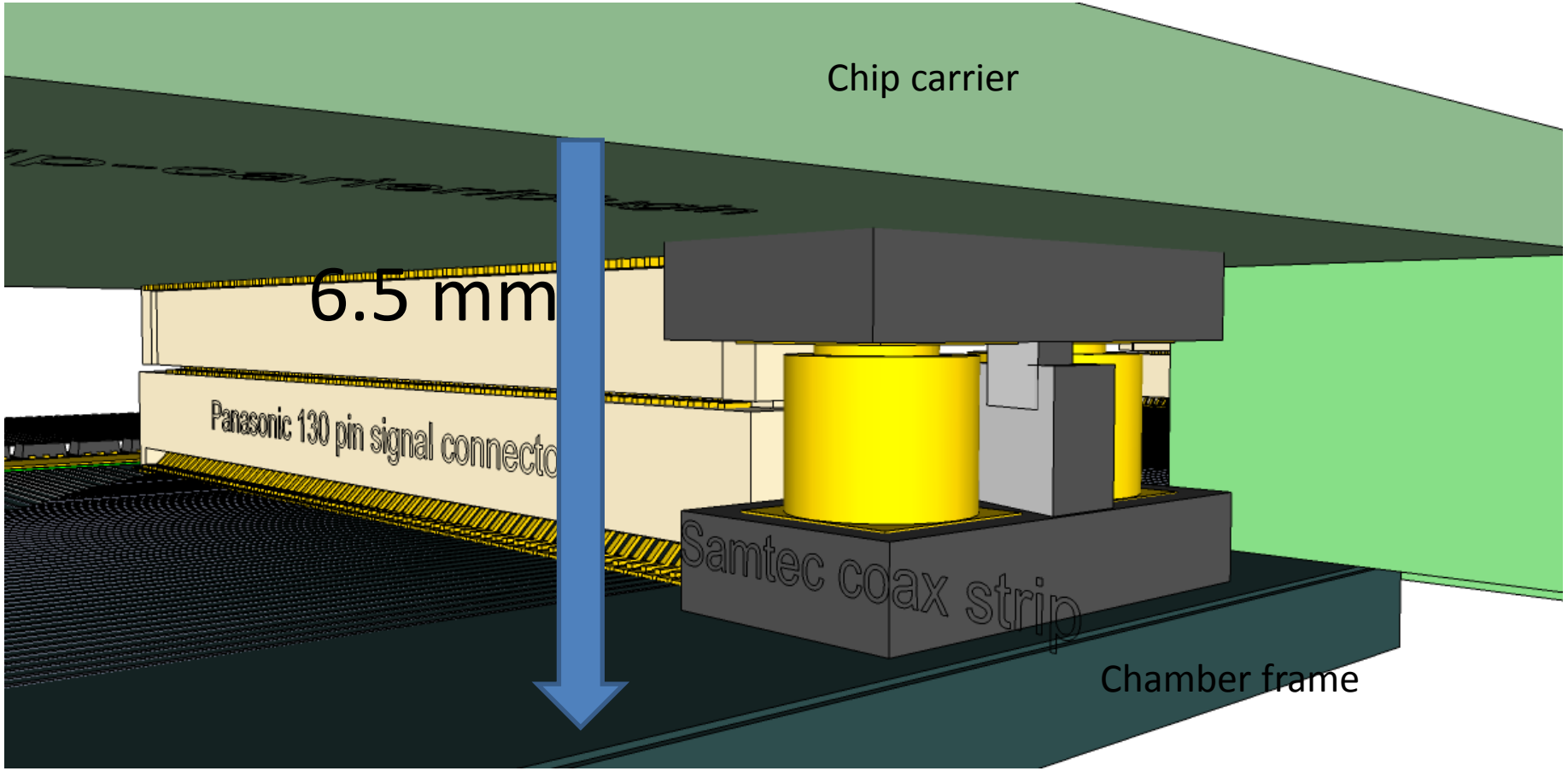
2x +- 2.5 V -- APD25 chip
2x +- 6.0 V -- pickup preamp
2x xx GND -- grounds

Phoenix MC 1,5/ 6-GF-3,5 THT

Stack height

Sandwich height = 6.5 mm + 2 x PCB thickness

All chosen connectors (signals, coax, hdmi, power) are compatible with 6.5 mm



Summary

Progress since September 09 Mini Week

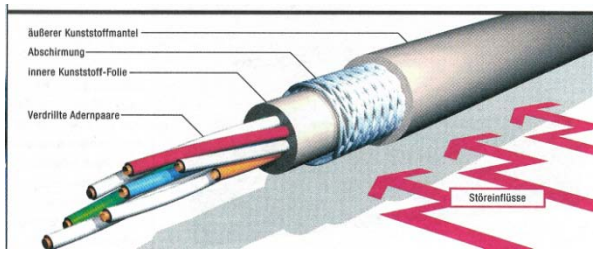
1. SRU PCB is in production by Eltos
2. DATE porting to Gigabit Ethernet progressing
3. DTC link firmware progressing at CCNU
4. Eurocrate mechanics finalized, off the shelf items
5. FEC final outlines released at CERN
6. 1st FEC card design started at UPV Valencia
7. Adapter card outlines A B and C all defined
8. 1st Adapter card A for analogue readout : concept finalized
9. New large C-card adapter for extensions
10. HDMI cable for analogue chip carrier readout under test
11. First chip carrier for APV25 (+ Beetle): concept finalized
12. Chip carrier connectivity for MM chamber edge defined

Approaching together the first SRS system

Backup material

DTC links: Data Trigger Control

a.) copper CAT -6 serial LVDS b.) MM fiber



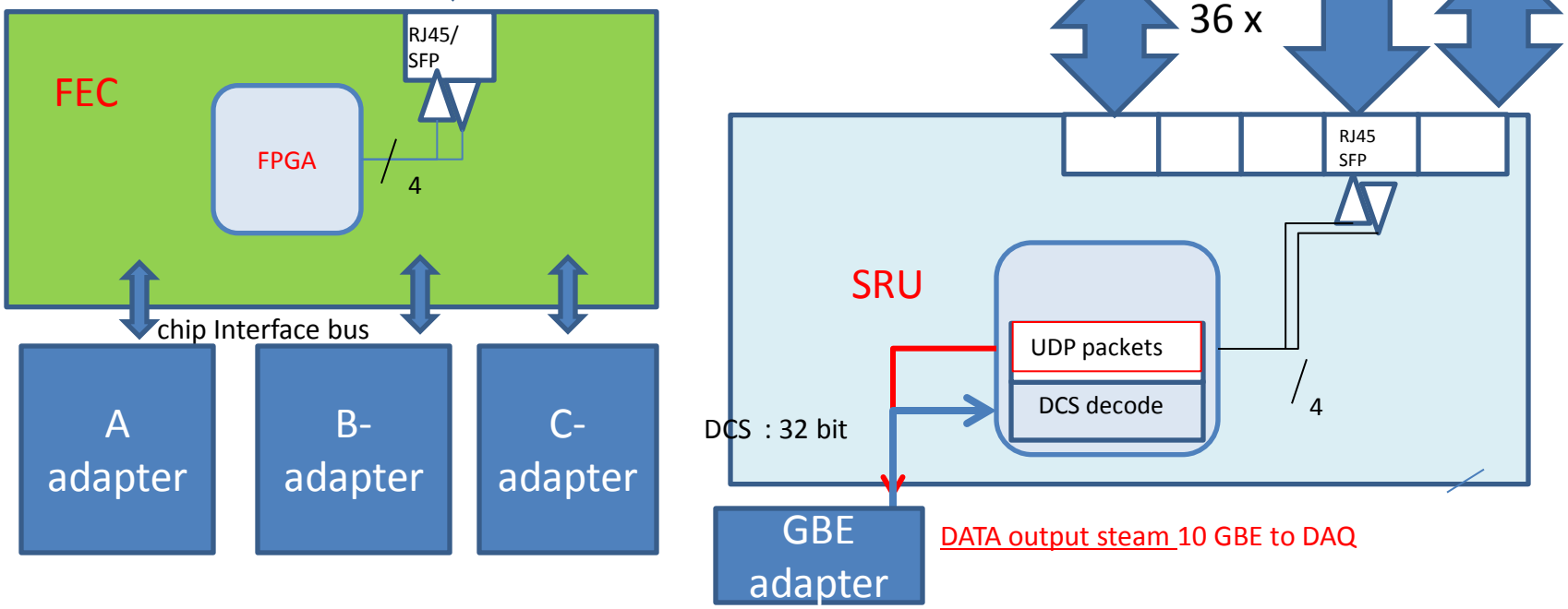
4 x twisted pairs
CAT6 cable

SFP RX/TX modules

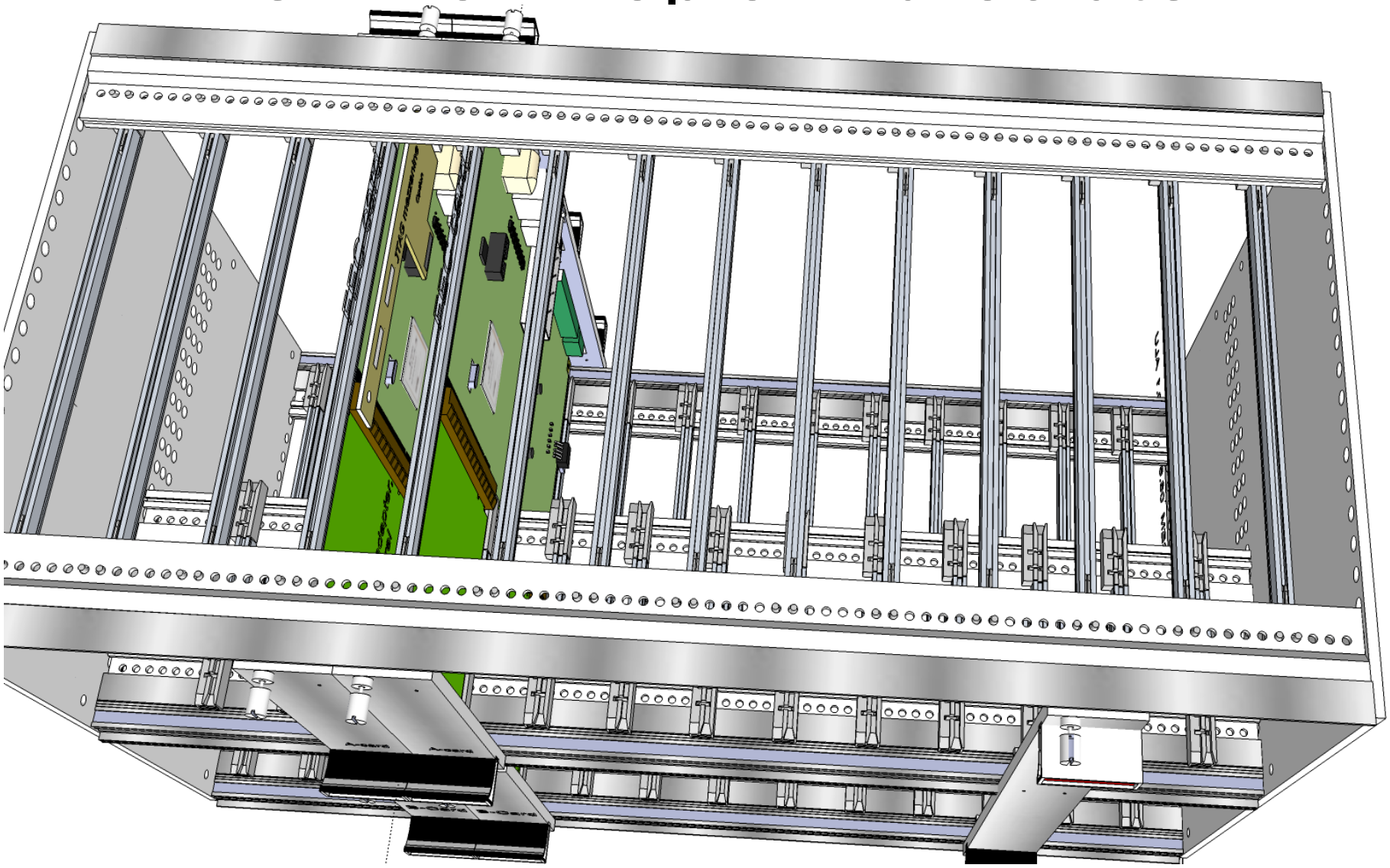
Note: 1st SRU has only copper

Clock ← 40MHz / 4 Mhz
Data → up 200 Mbps LVDS / 1Gbit optical
Select ← trigger or data
Return → trigger or status

Input stream from 36 FEC's @ 166 Mbit/s
= 5.976 Gbit/s



View from Top on Eurocrate



Detail of FEC <-> A-card matching