Status of DTC links and firmware for the scalable readout system

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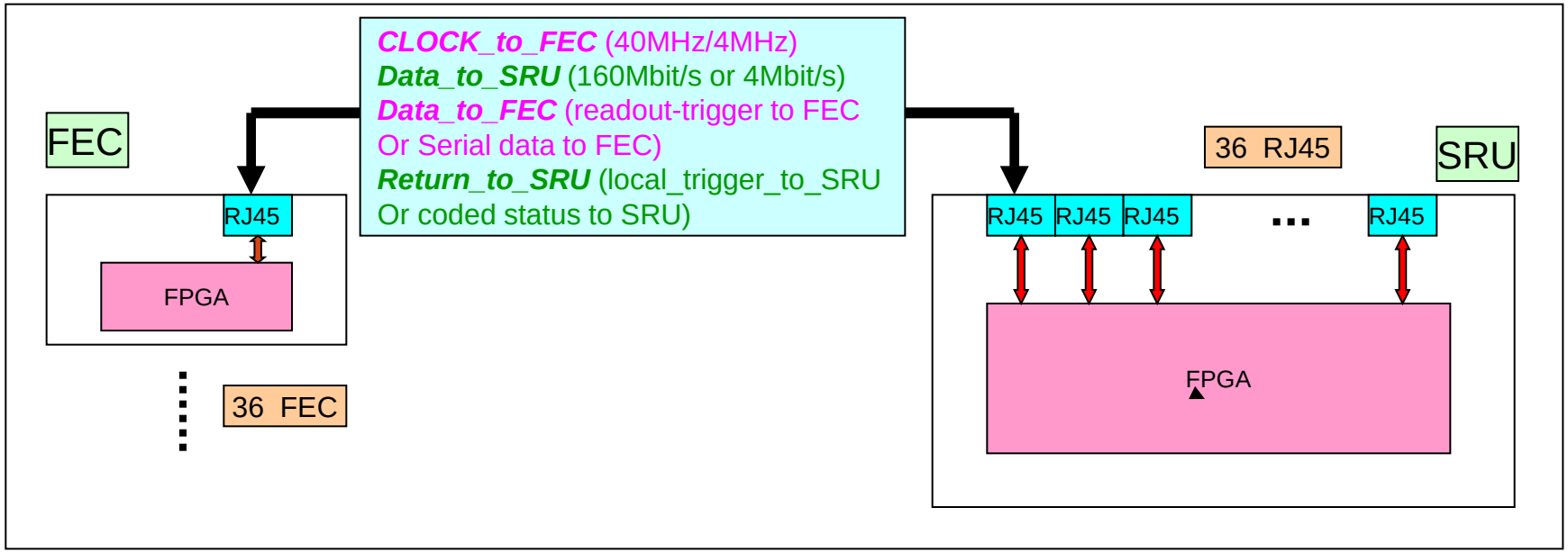
DTC(Data-Trigger-Control) link



- ***Readout mode***
  - **Clock = 40 MHz to FEC**
  - **Data = 160 Mbit/s to SRU**
  - **Trigger = select = readout-trigger to FEC**
  - **Trigger =return = local trigger to SRU**

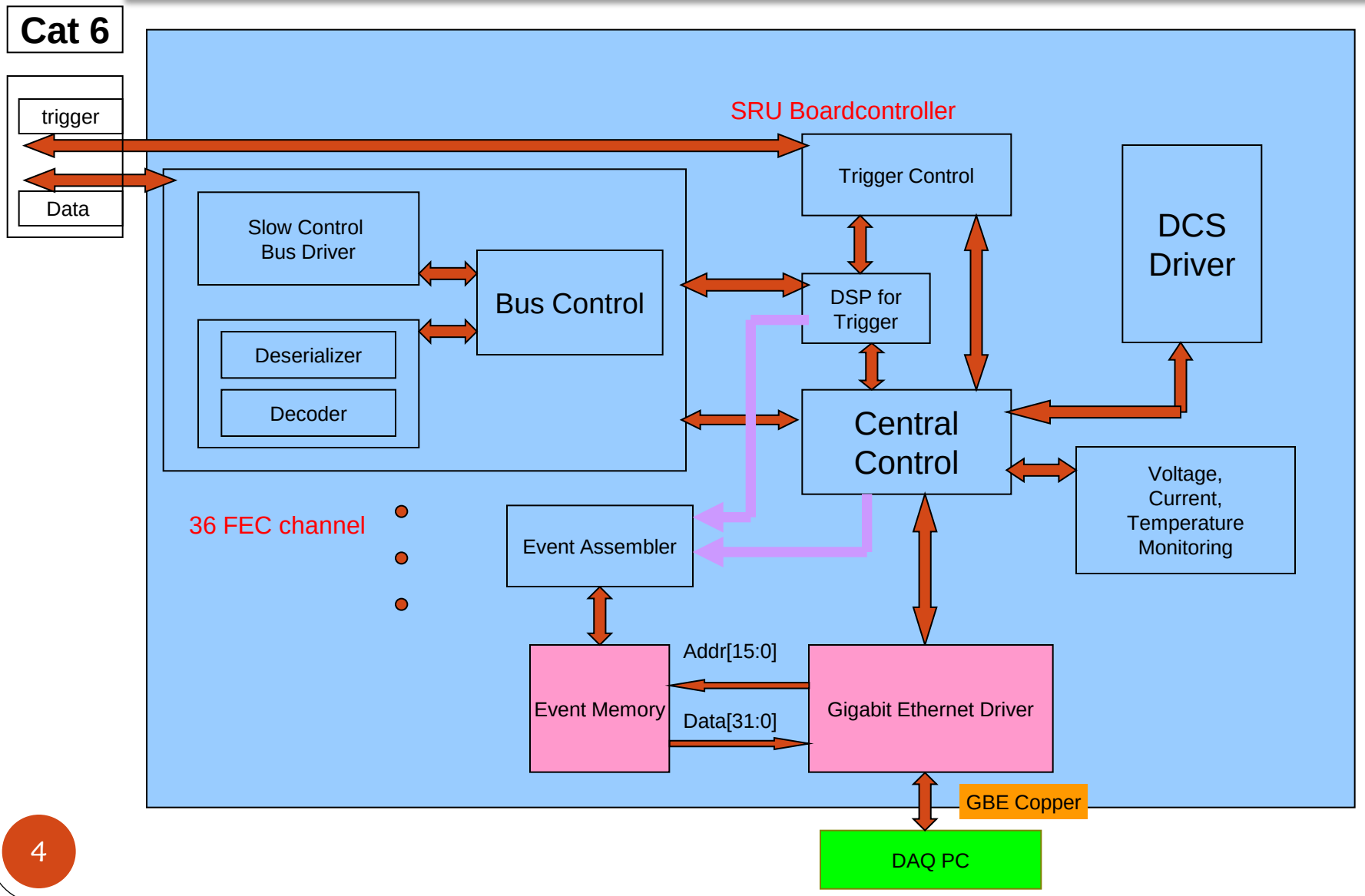
- ***Control mode***
  - **Clock = 4 MHz to FEC**
  - **Data_out = Serial data out to SRU**
  - **Data_in = Serial data in to FEC**
  - **Return = coded status to SRU (Error? Busy? ...)**

DTC Link Test Status

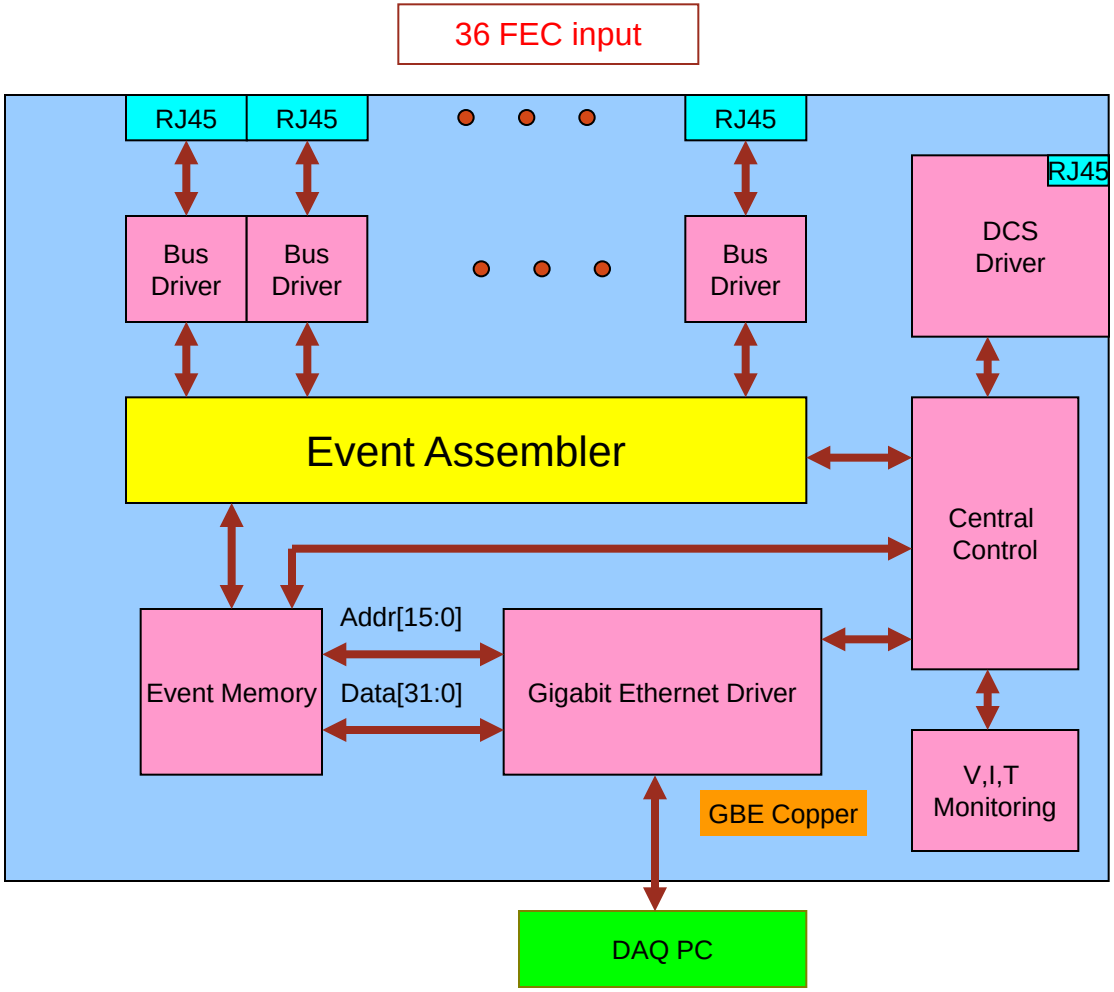
- **Firmware developing status**
  - The firmware for CAT6 data link testing has been developped.
  - The firmware for Frame encoding & decoding testing is under development and it is expected to be completed in 2-3 weeks.

- **Hardware preparation status**
  - Two CAT6 cables produced by different factories had been bought .
  - We have a good TRU board.
  - The Xilinx Virtex-5 evaluation board (ML505) had been ordered and will be in our lab one and half weeks later.
  - We are preparing to produce two LCU boards in China for DTC link and SRU firmware testing. It is expected to be finished in one and half months (Including PCB production, chips procurement and mounting).

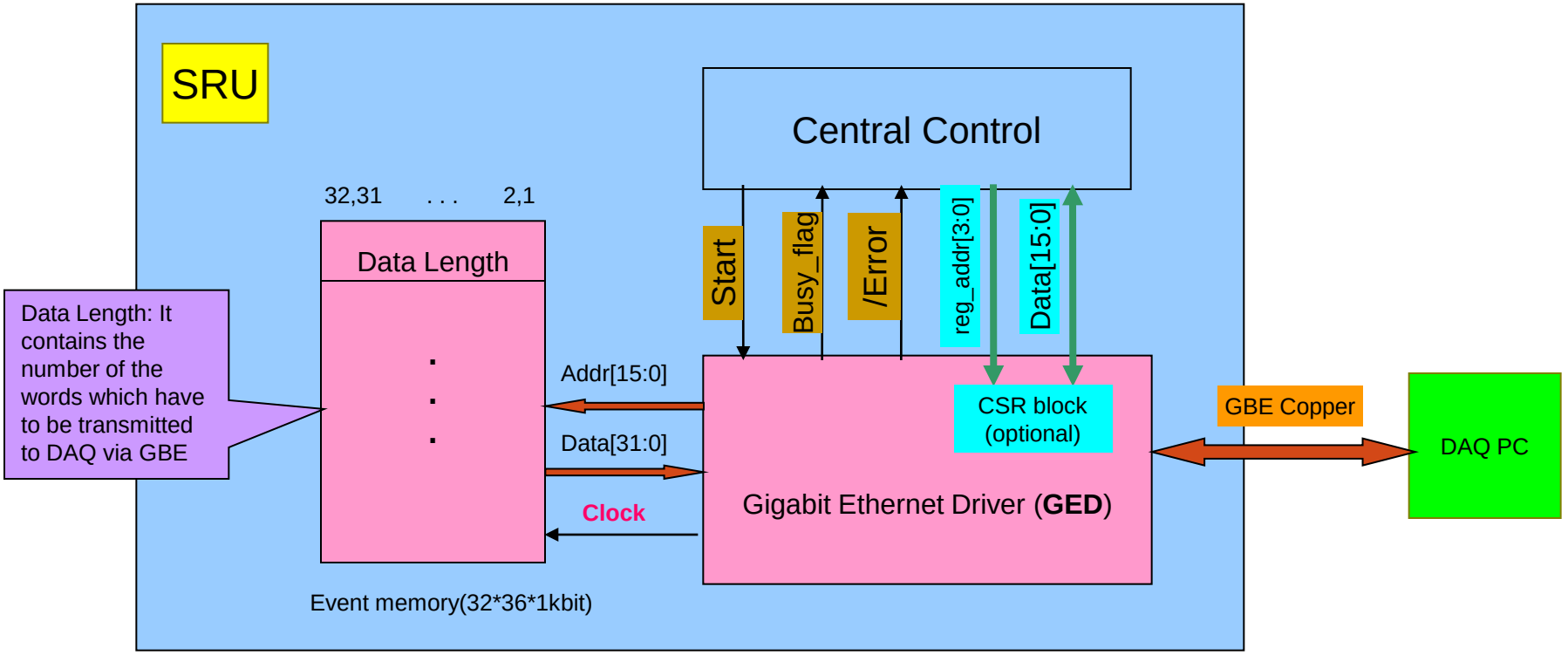
Firmware Architecture for SRU



First Target 2009: Firmware Architecture for Data Assembling and Transmission in SRU



Detailed Interface for GBE driver in SRU



Note:

- This interface definition had been discussed with Alfonso Tarazona Martinez.
- The signal definitions are presented in next slide.

Detailed Interface for GBE driver in SRU

The interface signals between GED(Gigabit Ethernet Driver) and other part of the SRU:

- ***Start*** : After received the command signal '***Start***', the GED will begin to transfer the data in Event memory block via GBE Copper link to DAQ PC.
- Busy_flag : The ***Busy_flag*** will be asserted to high when GED is transferring data to DAQ. It is low when GED transmitter is idle.
- ***Error*** : The error flag, low active, It will be asserted to low when there are some errors occured in GED.
- Reg_addr[3:0] and ***Data[15:0]*** : The address and data interface between the optional CSR block in GED and the Central Control block. The CSR block can include the configuration and status registers of GED, the DCS can configure and get the status of GED via these registers in CSR block.
- **Clock** : The frequency of the clock to read the Event memory is **200MHz**.

Note:

- The data format of Event_data has not been defined clearly yet, which needs further discussion with DAQ (DATE) developers.
- The data length of the event which stored in the Event memory is variable, and the event length is stored in the (Data Length) adress 0x0000 of the memory.
- The CSR block is optional, and the registers are defined by GED developer.

Thank you for your attention!