From Chip Matrix to the ‘Ideal Chip’ for MPGD

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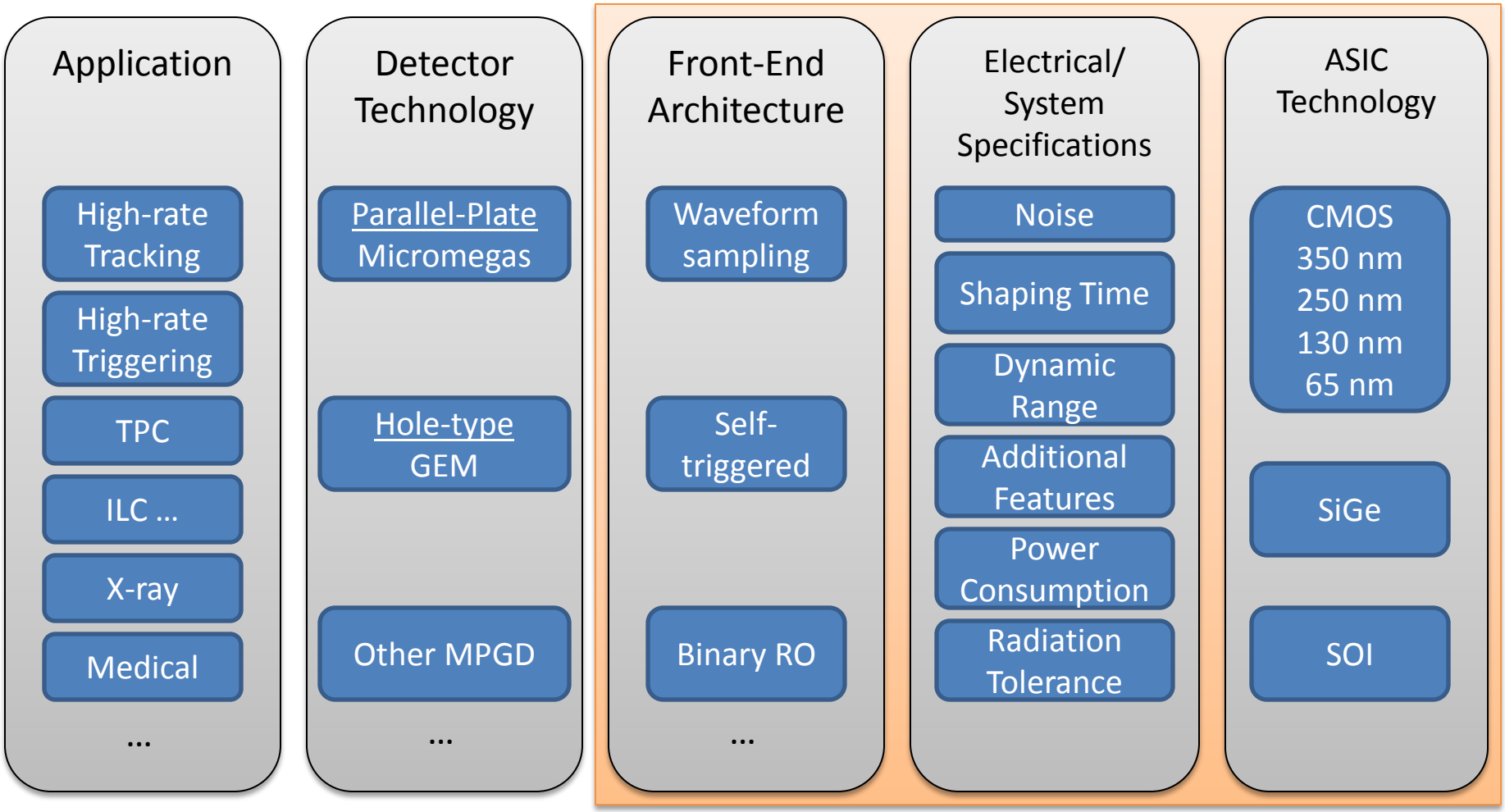
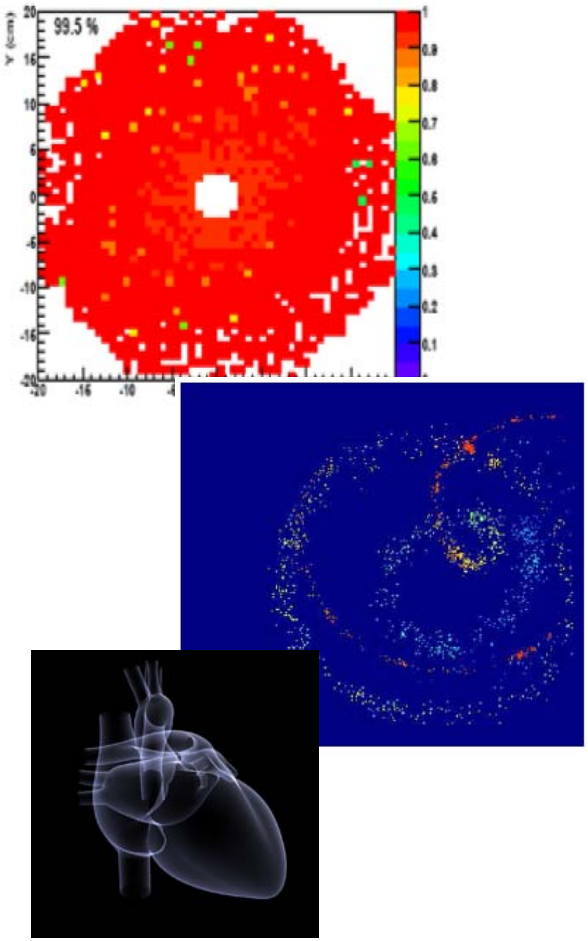
“Ideal Chip” Specification



Applications

Application

- High-rate Tracking
- High-rate Triggering
- TPC
- ILC …
- X-ray
- Medical
- …

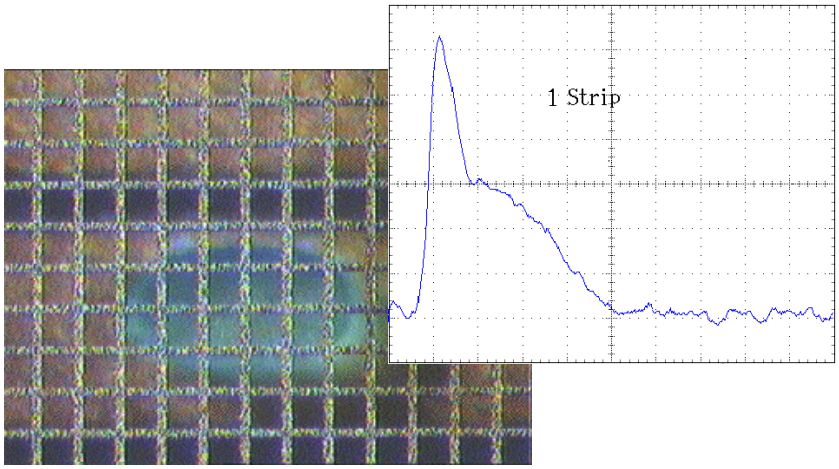


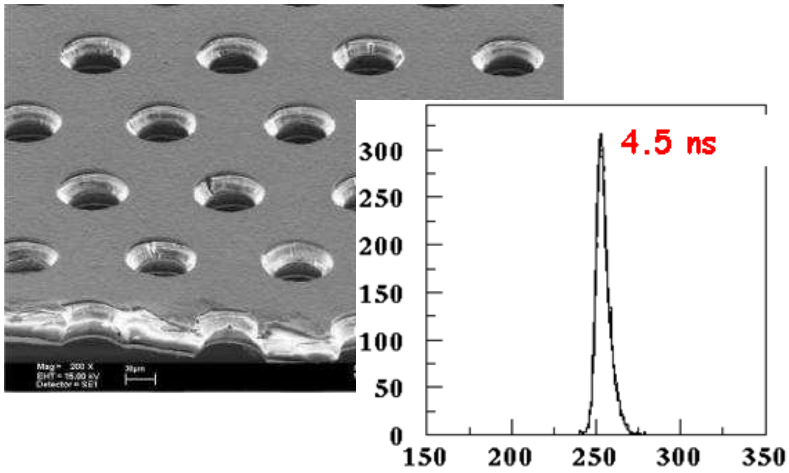
- total rate = … 25 kHz/mm^2
- rate/channel = ?
- spatial resolution = 10 … 100 um
- temporal resolution = 1 .. 25 ns
- energy resolution = ?
- efficiency = 95 … 99 %

Detectors

Detector Technology

- Parallel-Plate Micromegas
- Hole-type GEM
- Other MPGD
- ...

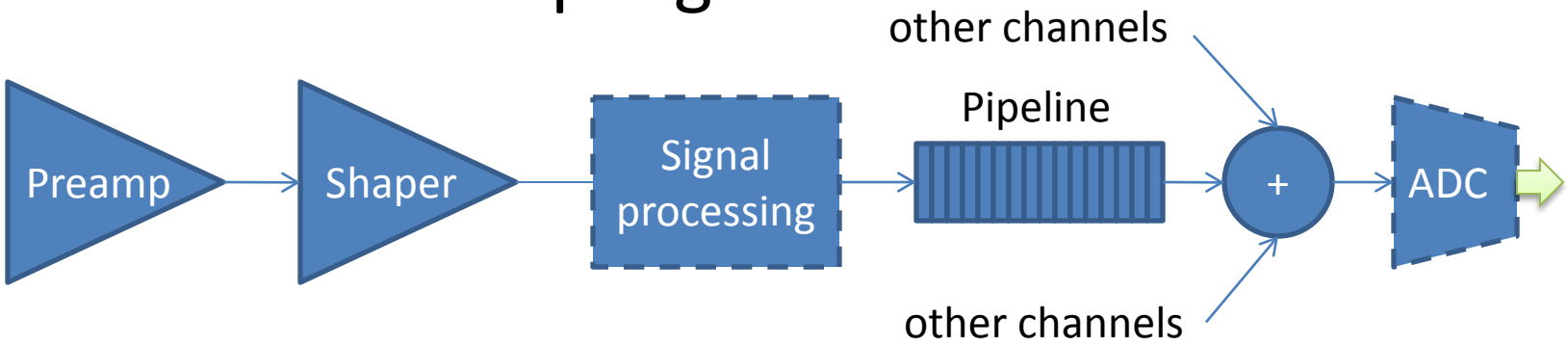




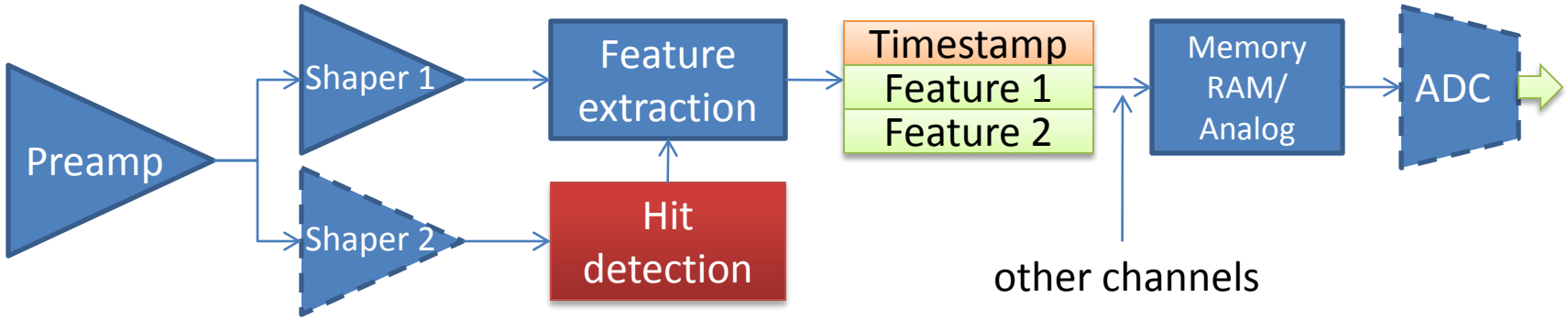
- gas gain = 10^3 .. 10^5
- signal range = 10 .. 1000 ke^-
- amplitude distribution
- signal width = 5 .. 20ns

Front-End Architecture

- Waveform sampling



- Self-triggered channel



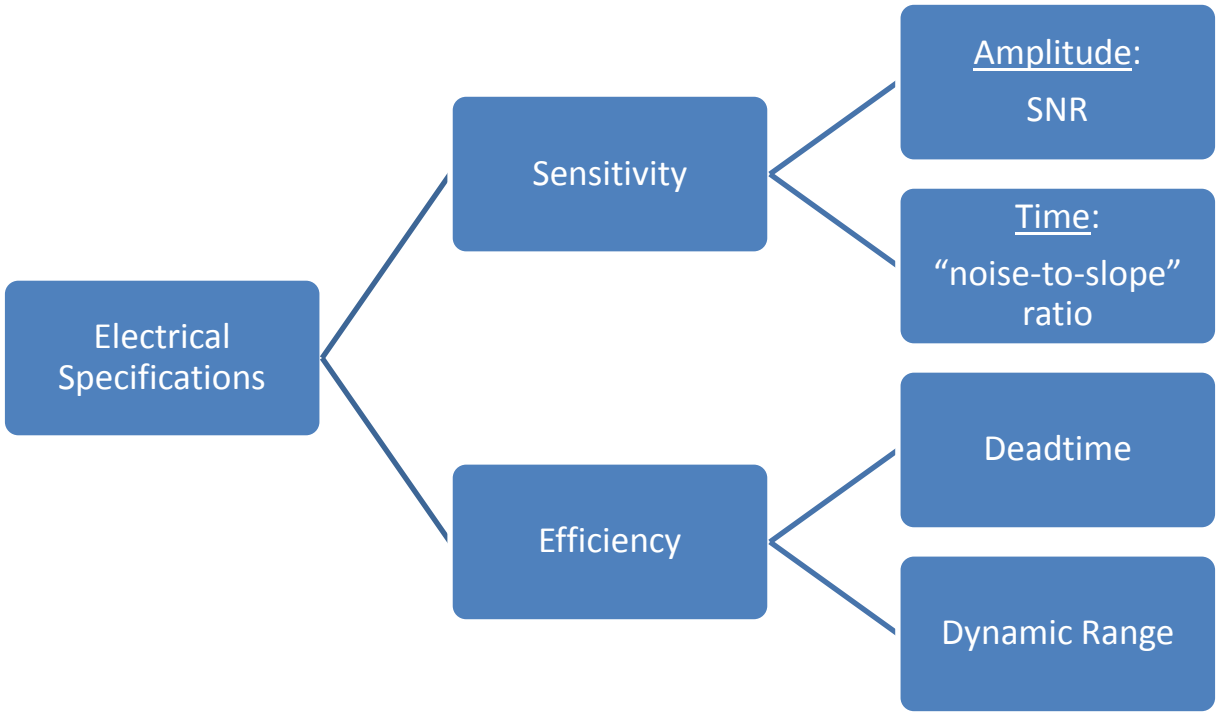
Front-End Architecture

	Pros	Cons

Waveform sampling
 	
•analog: *APV25, Beetle*
•binary: *VFAT*
•digital: *(S)ALTRO, SVX4*
	• simple (relatively)
	• versatile
	• off-line data processing
	  • pile-up rejection/detection
	  • systematic error correction
	  • advanced feature extraction
	• data rate ~ trigger rate
		• high data/event
		• readout time
		• needs external trigger
		• no zero-suppression

Self-triggered channel
Example: MSGCROC
	• zero-suppression
	• optimal data/event
		• less versatile
		  • pile-up rejection difficult
		  • limited off-line processing
		• data rate ~ event rate
		• high R/O bandwidth

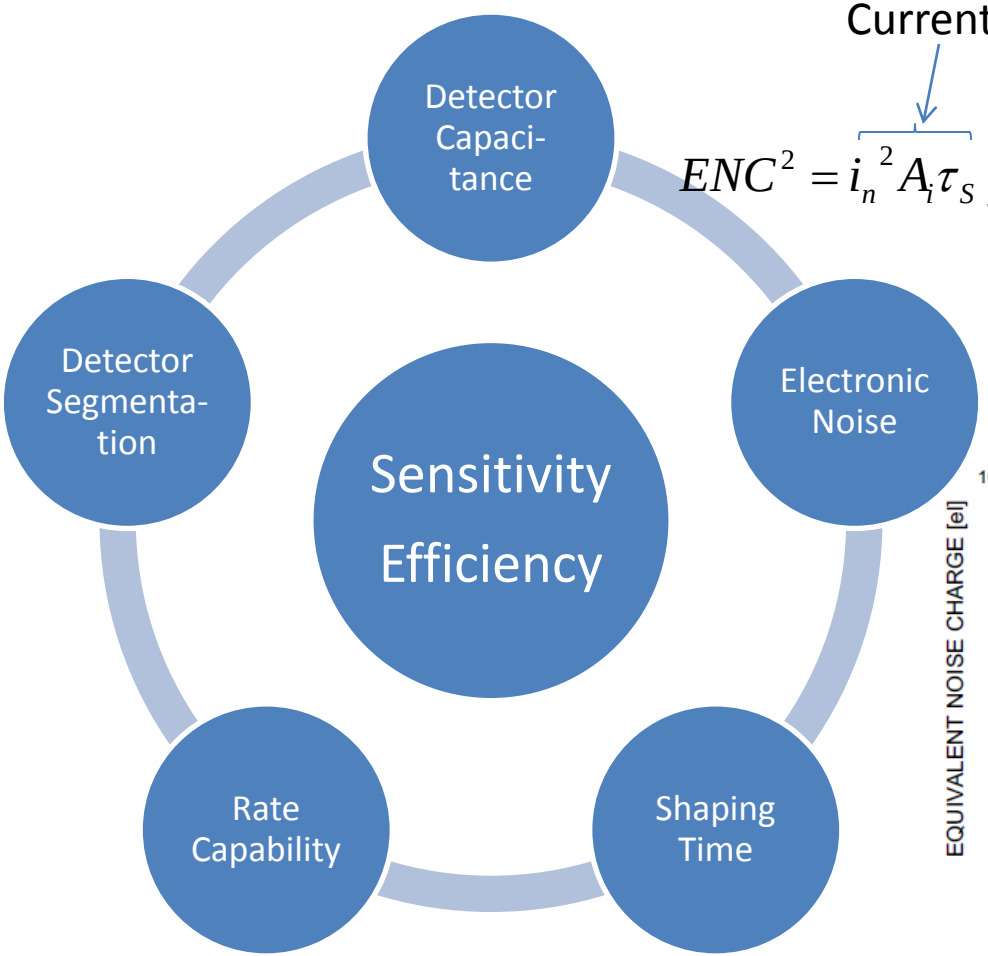
Electrical Specifications



$$\frac{\Delta E}{E} \propto SNR$$

$$\sigma_t = \frac{\sigma_v}{dV/dt}$$

Sensitivity vs. Efficiency



Current Noise

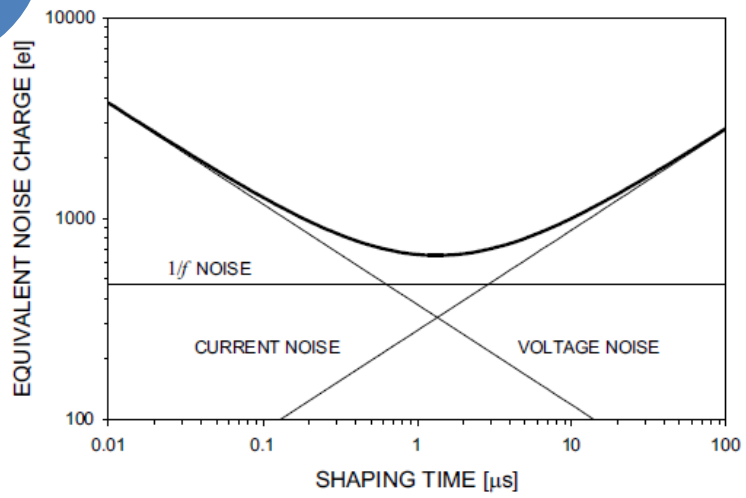
detector capacitance

$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

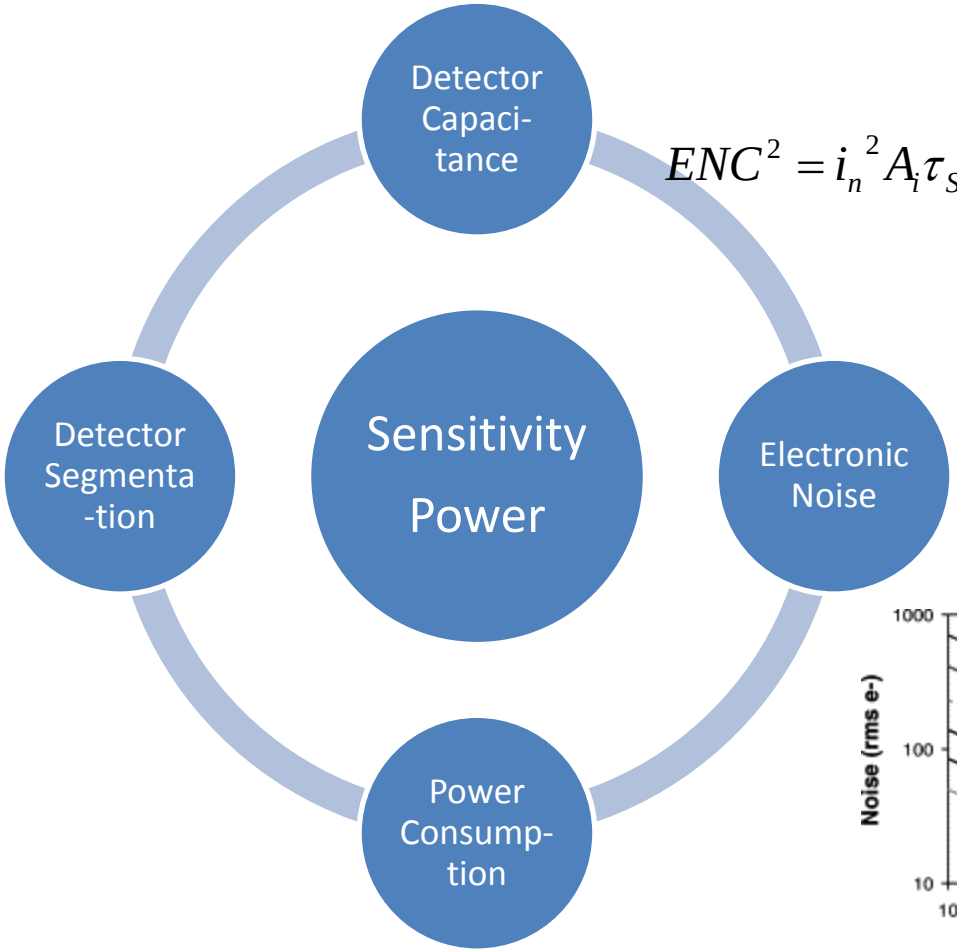
shaping time

White Noise

1/f Noise



Sensitivity vs. Power

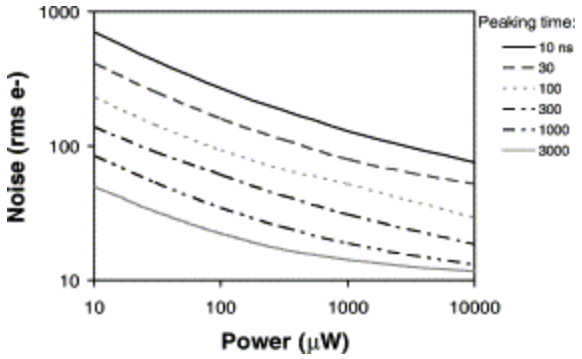


detector capacitance

$$ENC^2 = i_n^{\ 2} A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

$$S_w = \frac{8}{3}\frac{KT}{g_m}$$

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}$$



Capacitive Matching

- 1/f noise dominant

$$ENC_{1/f}{}^2 = A_f K_f \frac{(C_D + C_g)^2}{C_g{}^2} \quad \Rightarrow \quad C_g = C_D$$

- white noise dominant

$$ENC_w{}^2 = \frac{8}{3}\frac{KTA_w}{\tau_S}\sqrt{\frac{L^2}{2\mu}}\frac{(C_D + C_g)^2}{\sqrt{C_g}} \quad \Rightarrow \quad C_g = C_D/3$$

- No preamplifier can provide optimum noise performance for every detector

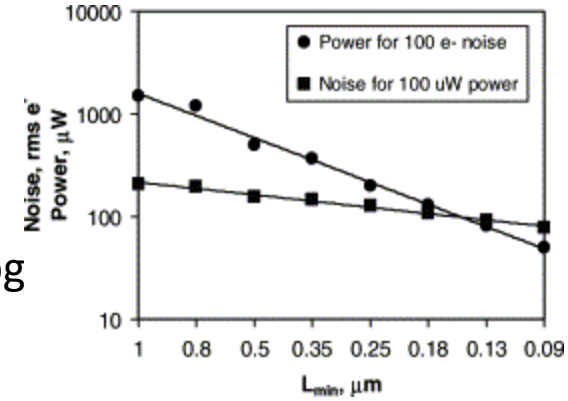
Technology

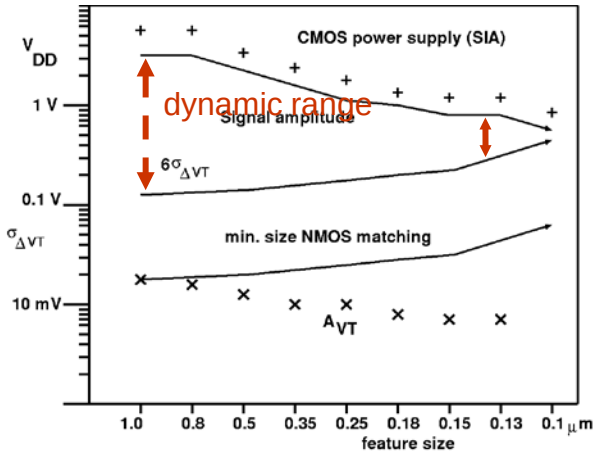
CMOS scaling

- better noise performance
- lower dynamic range
- optimum technology for analog design appears to be around the 0.25um node

Digital circuits clearly benefit from scaling

- Smaller ADCs
- More powerful digital signal processing
- (Auto)calibration and error correction digital circuits could compensate the analog performance deficit





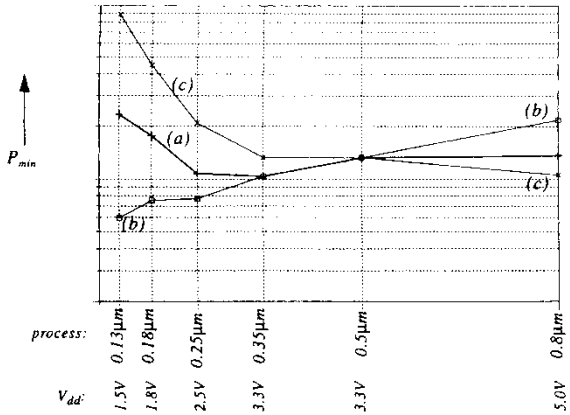


Fig. 8. Minimum power consumption for a voltage follower circuit (with constant topology, SINAD and maximum signal frequency). (a) Made in various processes, operated at their corresponding supply voltages. (b) Made in various processes, all operated at $V_{dd} = 3.3$ V. (c) All made in 0.5-μm CMOS, operated at various supply voltages.

Features

Chip matrix

Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
APV25	CMS	Si strip	128	50	270+38e/pF	20	both	A	40	2.7	PD, PR	0.25 CMOS	10
AFTER	T2K	TPC	72	100-2000 s-gauss	(350-1800) + (22-1.8)e/pF	19	both	A	1-50 (100)	7.5	VG,VS	0.35 CMOS	no
MSGCROC	DETNI	Gas strip	32	T: 25 E: 85	2000e @ 40pF	800	both	A,1	2ns TDC		VG, ZS	0.35 CMOS	no
Beetle	LHCb		128	25	500+50e/pF	17.5	both	A/1	40	5.2	F-OR	0.25 CMOS	40
VFAT	TOTEM		128	22	650+50e/pF	18.5 (cal)	both	1	40	4.47	F-OR	0.25 CMOS	50
NINO	ALICE	TPC	8	1	1900+165/pF	2000 th<100	both	1	async	30	BR	0.25 CMOS	no
CARIOCA	LHCb	MWPC	8	<15 @ 220pF	2000+40e/pF	250	both	1	async	46	BR	0.25 CMOS	20
PASA+ ALTRO	ALICE TPC	TPC	16	190_{fwhm} s-gauss	570e @20 pF	160	both	10	20	< 40	BC, TC, ZS	0.35,0.25 CMOS	
SVX4	CDF, D0	Si strip	128	100-360	410+45e/pF	60fC	neg	8	106 (212)	2	ZS	0.25 CMOS	20
SPIROC	ILC, T2K	SiPM	36	A:25-175 T: 10	A: 1/11pe; T:1/24pe	2000 pe	neg	8-12	100ps TDC	0.025 *pulse*	dual-gain	0.35 SiGe	no

Legend: PD = peak detection, PR = pile-up rejection, VG = variable gain, VS = variable shaping, F-OR = fast-OR, BR = baseline restorer, BC = baseline correction, TC = tail correction, DC = data compression, ZS = zero suppression

- ✓ fast-OR,
- ✓ variable gain,
- ✓ variable shaping,
- ✓ peak detection
- ✓ pile-up rejection,
- ✓ baseline restorer,
- ✓ baseline correction,
- ✓ tail correction,
- ✓ data compression,
- ✓ zero suppression

From Chip Matrix to the Ideal Chip

Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
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- shaping time: 5ns .. 1us
- dynamic range: <100fC
- power: < 10 mW/ch (?)
- ADC accuracy: 10 bits (?)
- TDC accuracy: 1ns

…

*We need an **APV25** chip with variable gain and shaping time like the **AFTER** chip, dynamic range like **MSGCROC,** integrated fast-OR like **Beetle**, integrated ADC like **SVX4,** digital signal processor like **ALTRO***