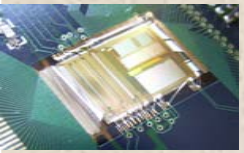
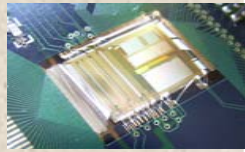
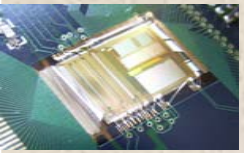


VFAT

A 128 channel chip for charge sensitive readout of multi-channel silicon & gas particle detectors.



P. Aspell *CERN*



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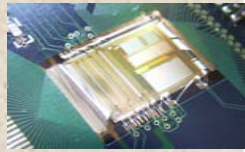
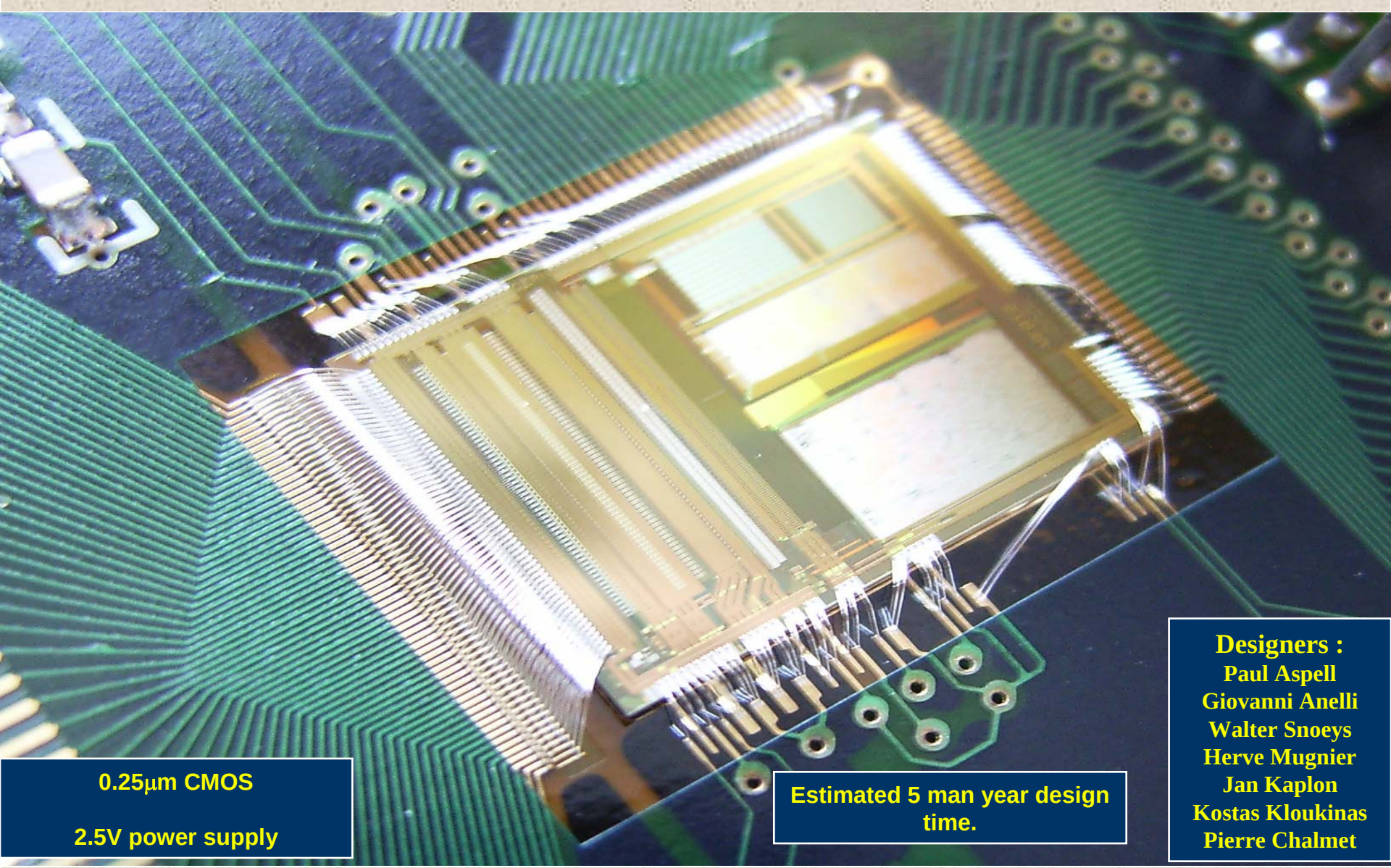




0.25μm CMOS

2.5V power supply

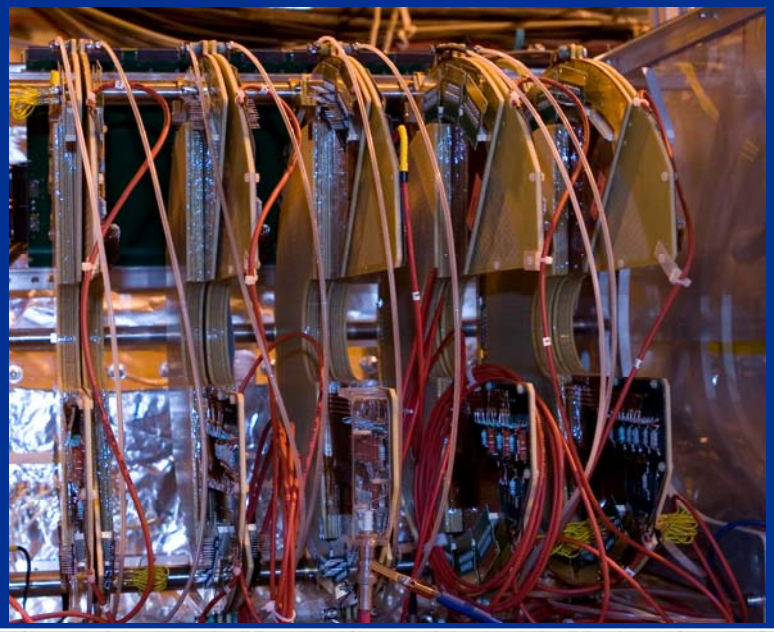
Estimated 5 man year design time.

Designers :
Paul Aspell
Giovanni Anelli
Walter Snoeys
Herve Mugnier
Jan Kaplon
Kostas Kloukinas
Pierre Chalmet

TOTEM's 3 different detector technologies

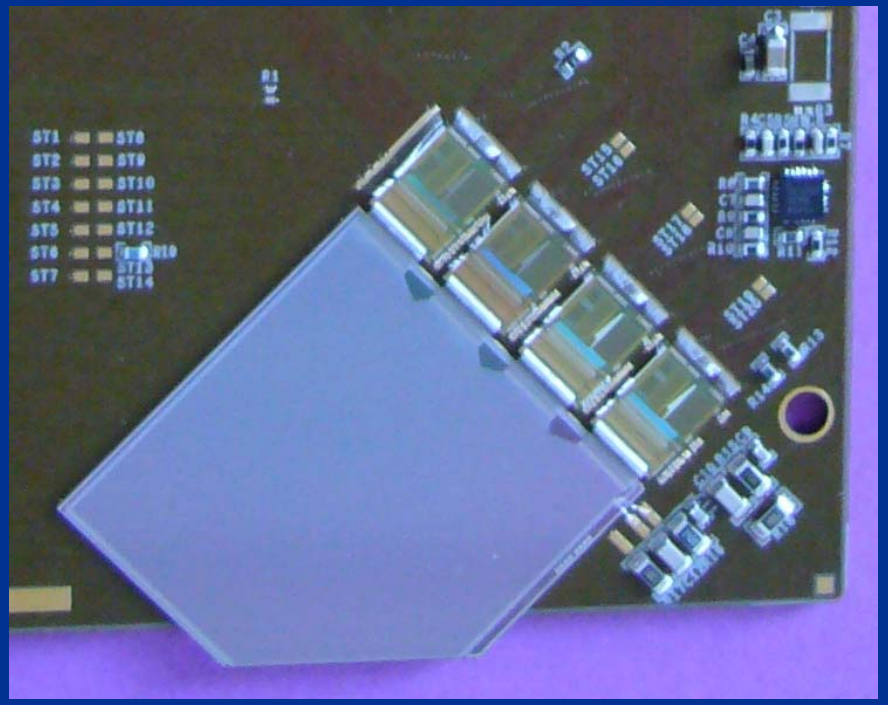
T1
CSCs

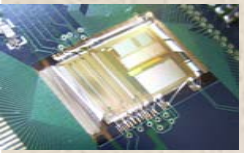
T2
GEMs



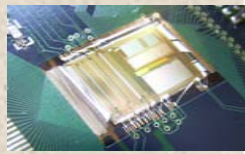
VFAT2 is used with all 3 detector technologies

Roman Pot – Silicon strips





VFAT2 Functions

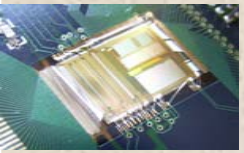


- **Trigger ……..**
  - Provide intelligent “FAST OR” information for the creation of a trigger.
- **Tracking …….**
  - Binary “hit” information for each of the 128 channels as triggered by the LV1A.

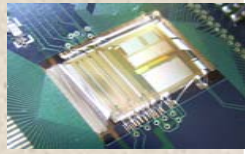
Reference for VFAT2:

“VFAT2: A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors.”

Proceedings of TWEPP Prague, Czech Republic, 3-7 September 2007, ISBN 978-92-9083-304-8, p.292 .



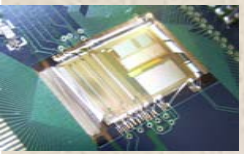
VFAT2 Key Features

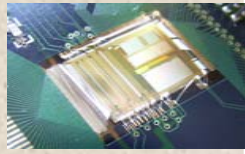


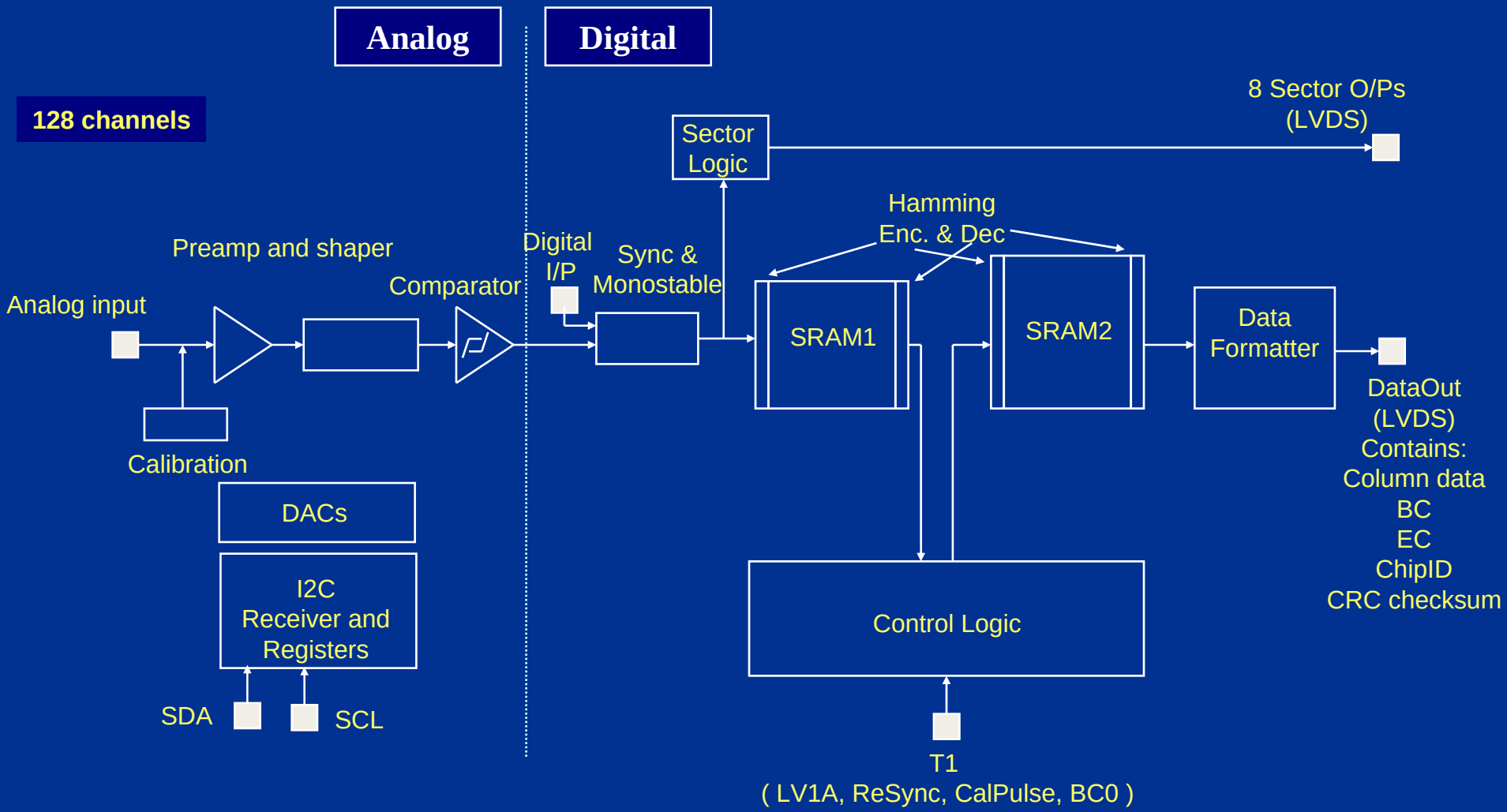
Trigger and Tracking Functions

- **128 channel** low noise front-end chip for binary readout of capacitive sensors.
- **40MHz signal sampling** (dead time free)
- **Digital memory** Programmable LV1A latency up to 256 clock periods. Simultaneously storage of up to 128 triggered events.
- **Trigger building** Programmable "fast-OR" trigger building outputs
- **Internal calibration** via internal test pulses with programmable amplitude
- **Fully programmable** through an I^2C interface.
- **Data packet output** includes headers, counters, flags and CRC check
- **Radiation tolerant** design – suitable for use in demanding radiation environments both with respect to ionising radiation and Single Event Upset.

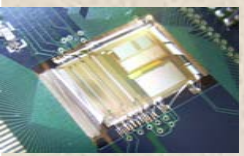
VFAT2 Signal Flow

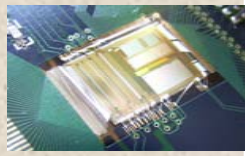


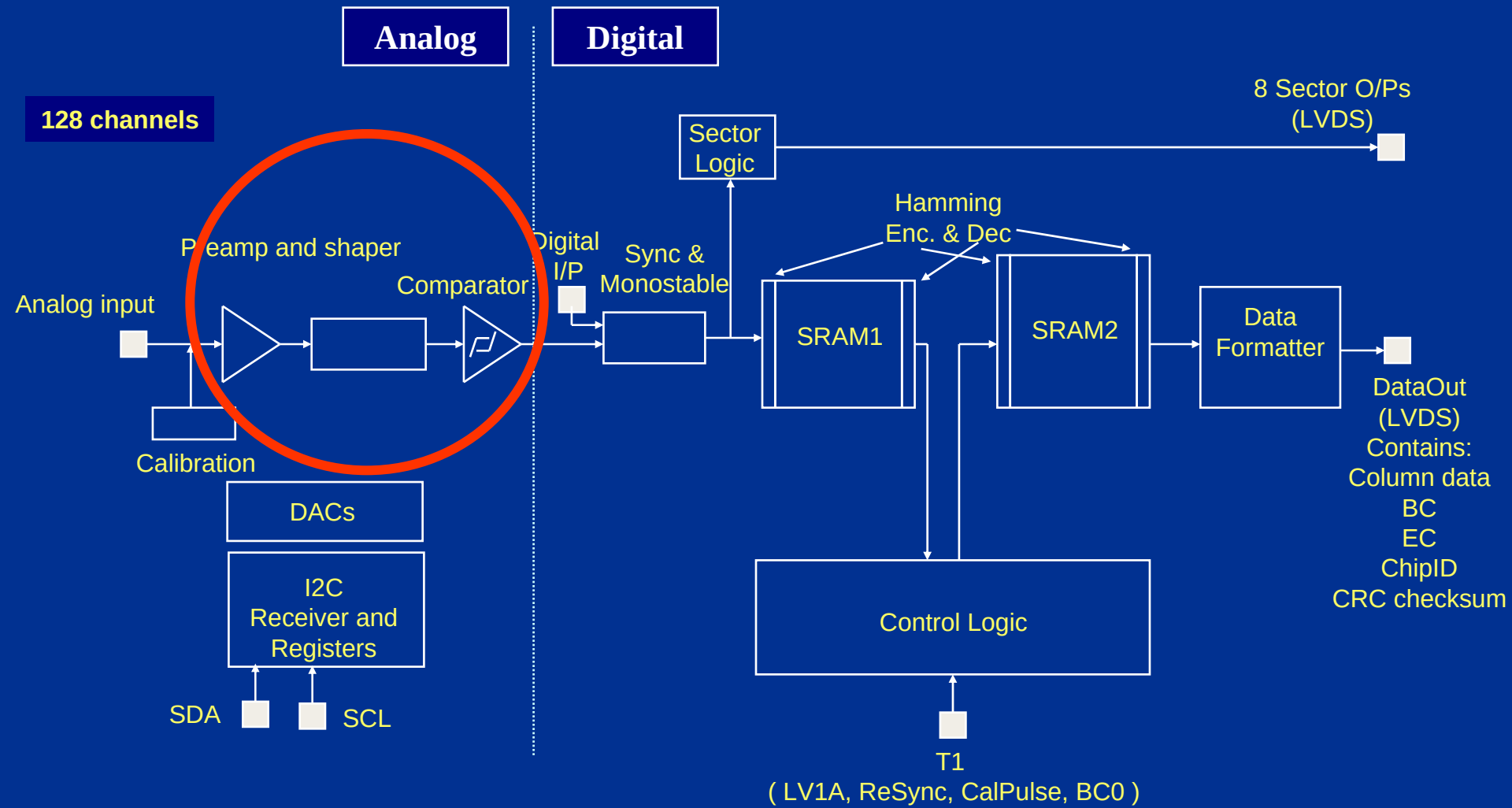




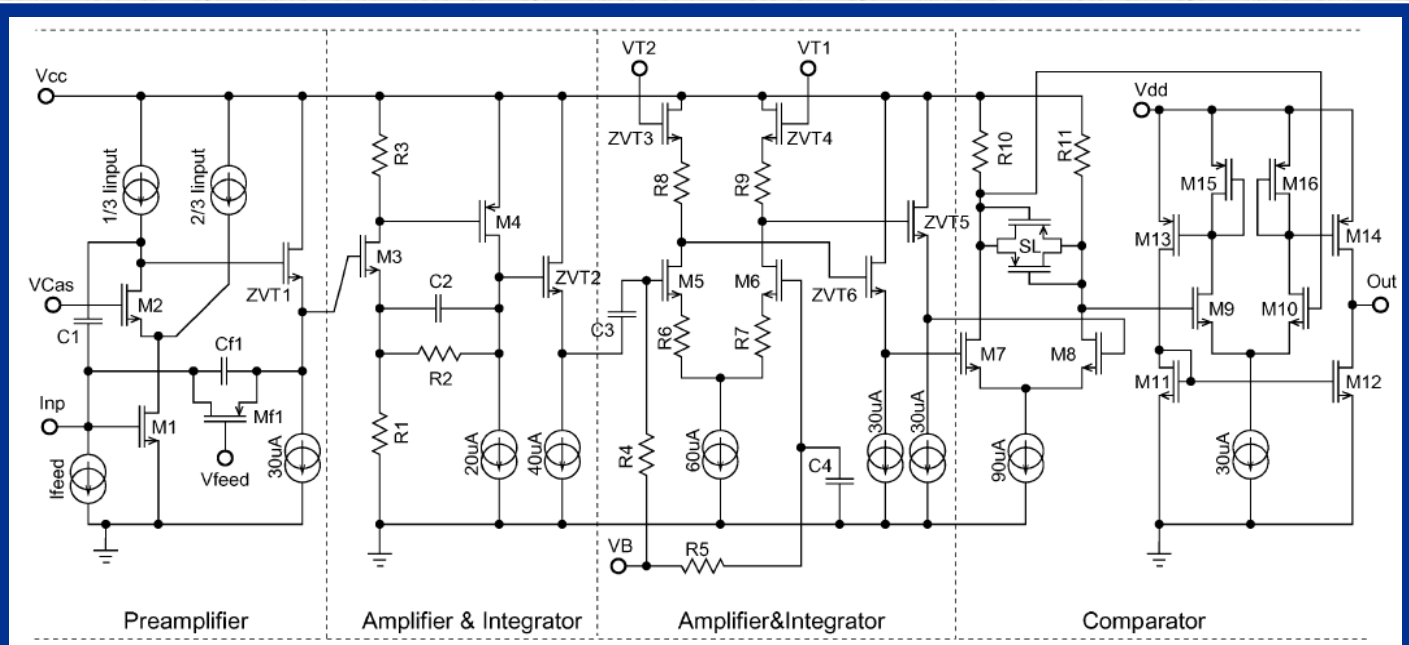
The Front-end







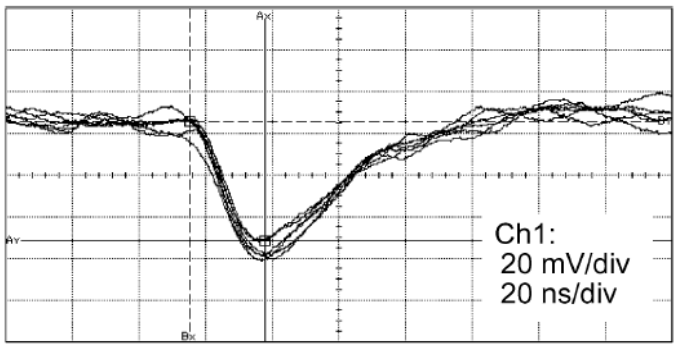
VFAT2 front-end

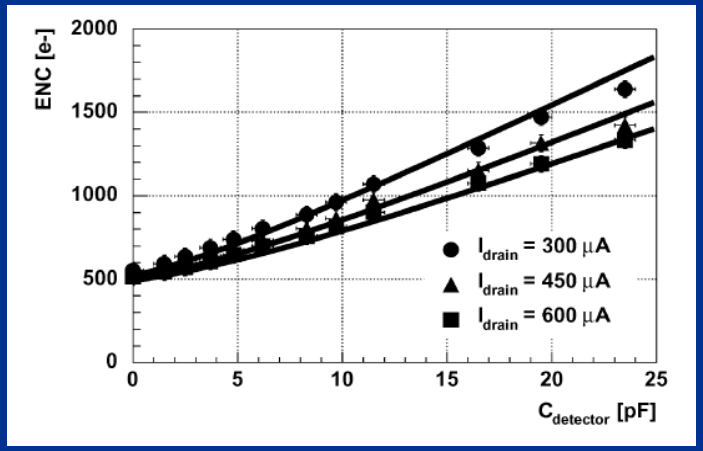


Also includes a 5 bit trim-DAC on each channel

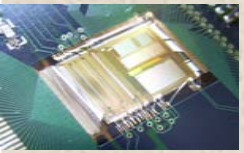
Gain	60mV/fC
Shaping Time	22ns
Power consumption	1.5 mW/channel
Linearity	± 12 fC
Time walk (for 1.2 to 10fC with 1fC threshold)	12ns
ENC (at 20pF)	<1500 e
Parallel noise	400e
Noise slope	40 – 60 e/pF
Radiation resistance	< 10 Mrads

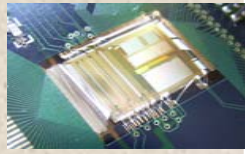
J.Kaplon, W.Dabrowski "*Fast CMOS Binary Front End for Silicon Strip Detectors at LHC Experiments* ,"
IEEE Transactions On Nuclear Science,
Vol. 52, No. 6, December 2005

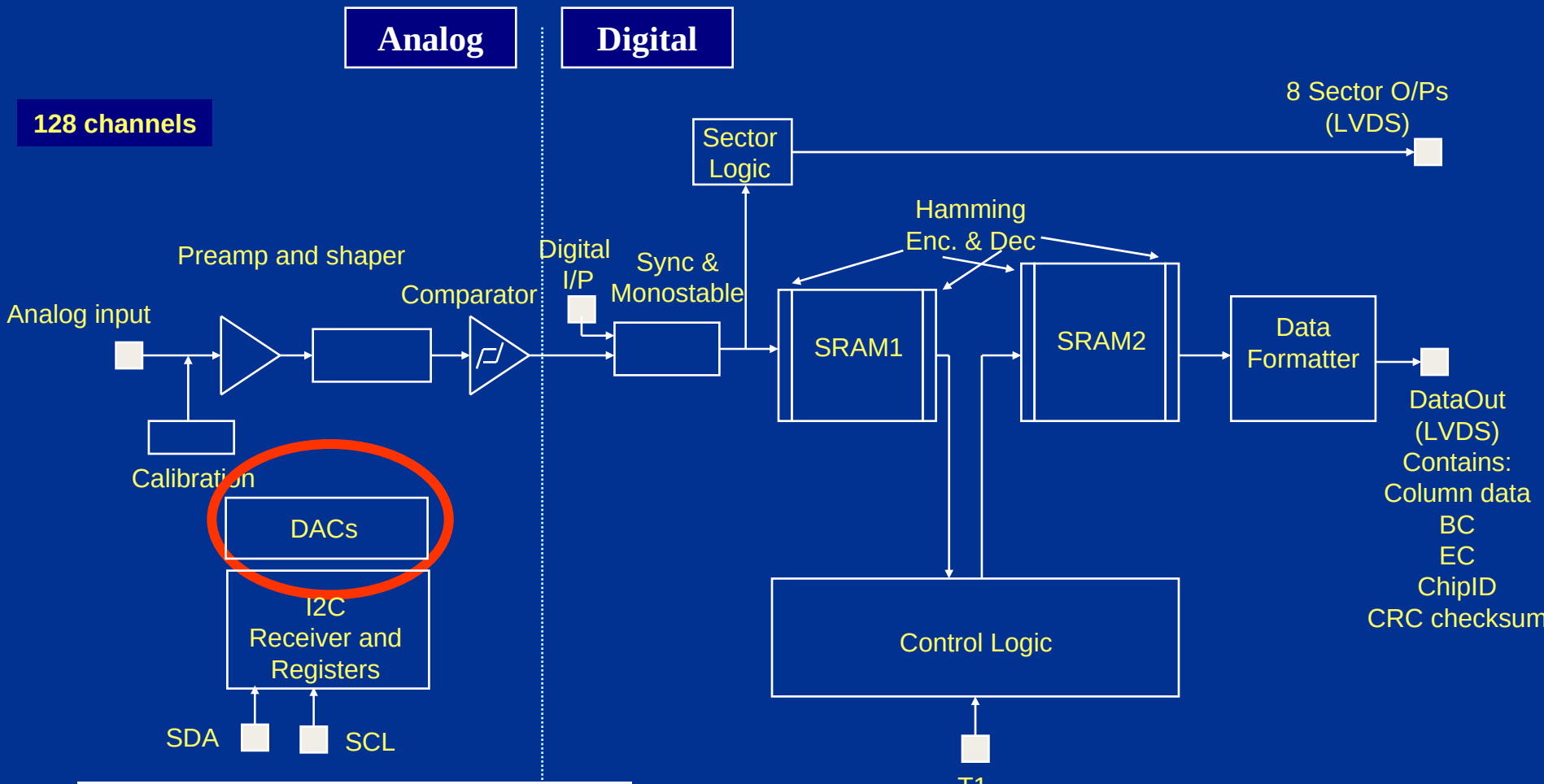




DACs



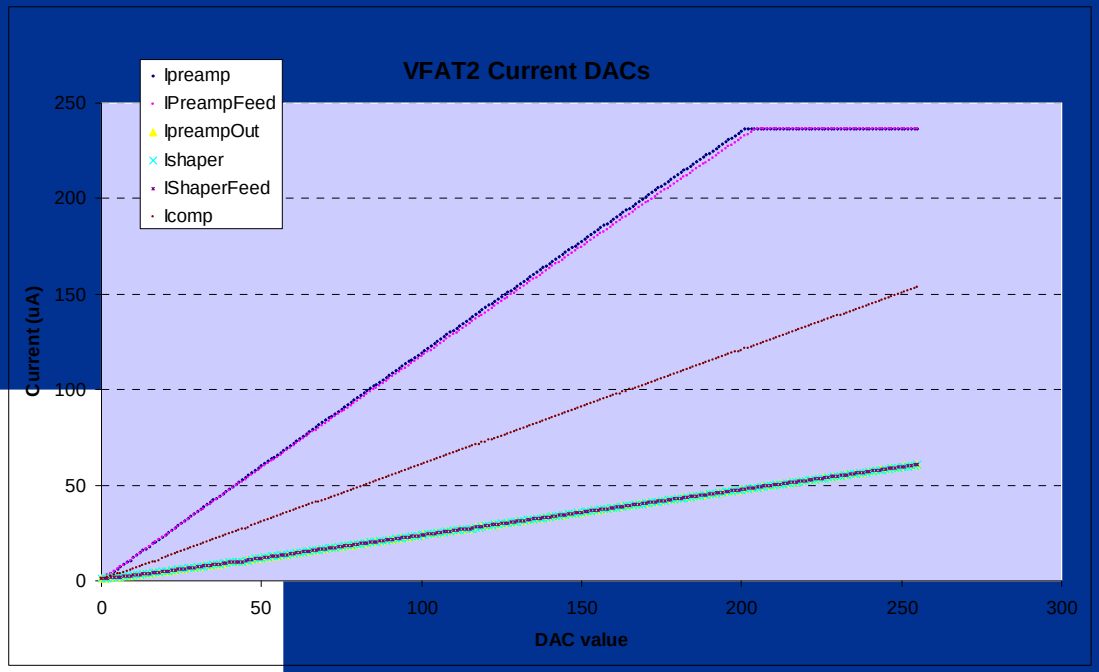


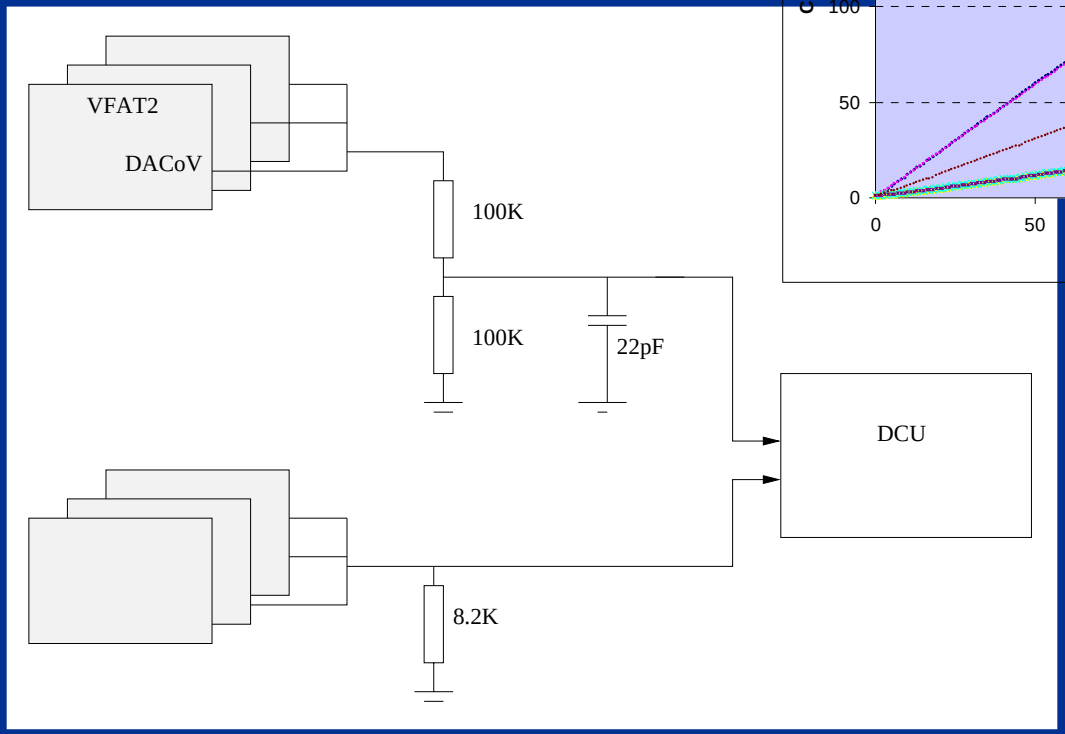


Global threshold adjustment &
Individual channel trimDACs

Characterisation of DACs

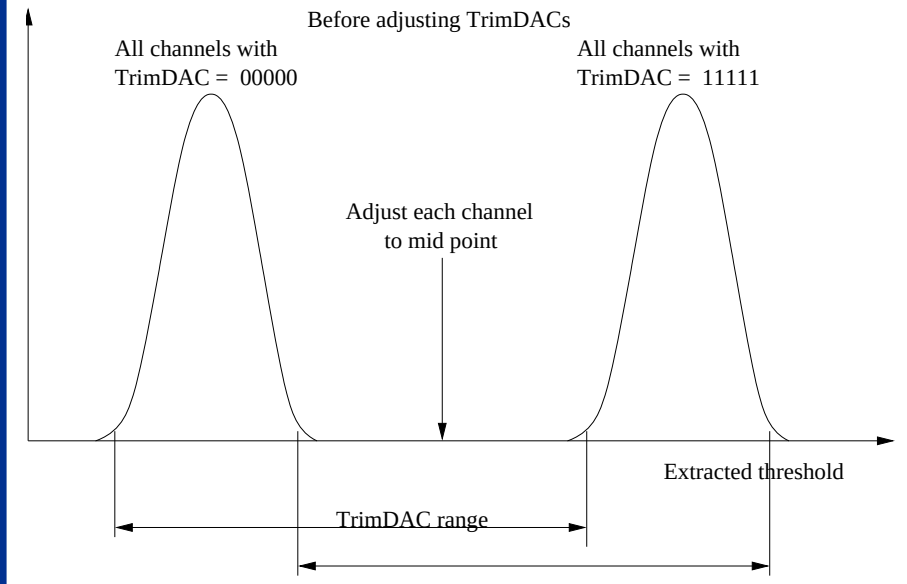
Each VFAT2 DAC response can be characterised.

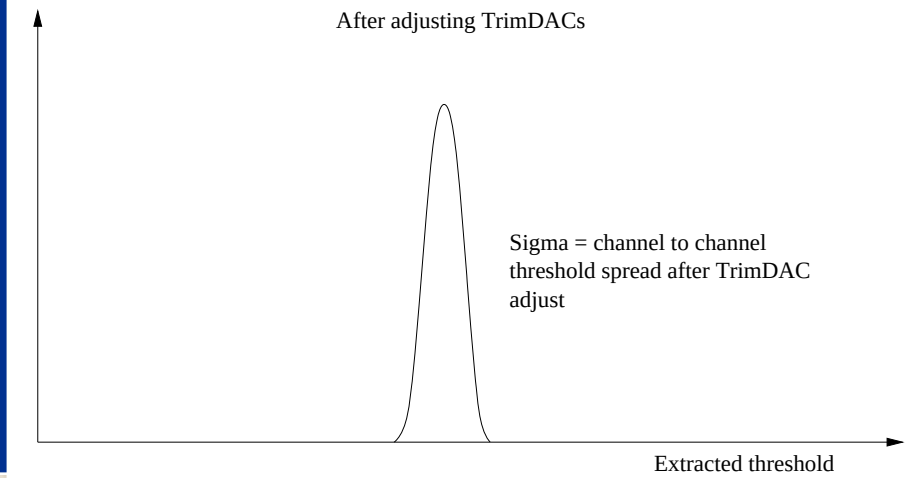




I2C commands route one by one each DAC V or I signal outside of the chip for measurement by the DCU. Also read by I2C.

TrimDAC functionality





5 bit TrimDAC for each channel

3 bits for TrimDAC range settings

Constant threshold :

1, Measure thresholds for all channels with TrimDACs = 00000 & 11111

2, Select TrimDAC range to have the smallest gap possible between the two histograms.

3, For each channel, adjust TrimDAC to central point.

OR

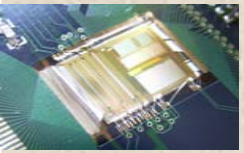
Constant clarity :

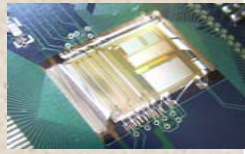
1, Adjust TrimDAC for each channel to achieve constant

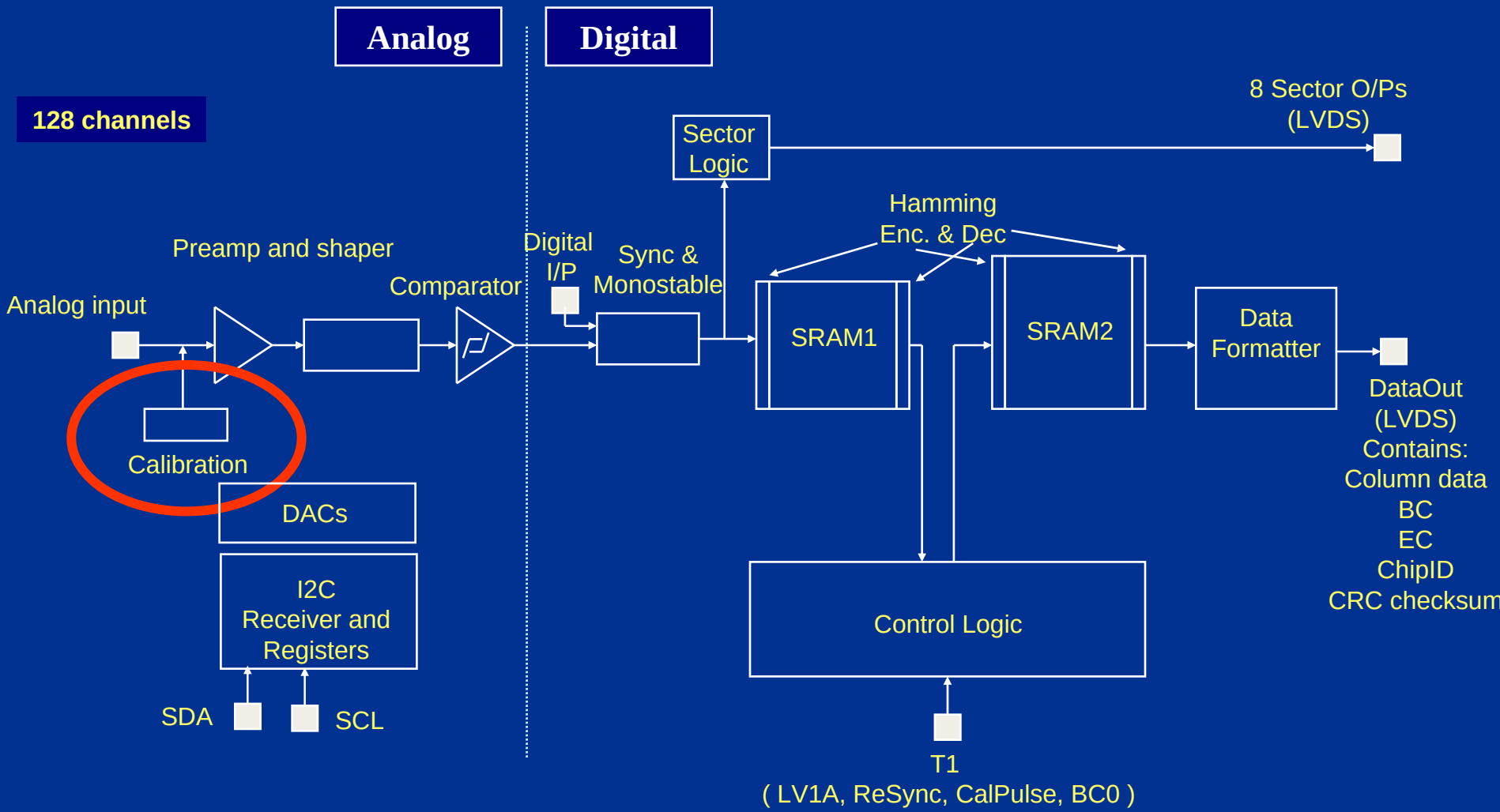
Threshold / (S/N)

Within limits, depends on the S/N variations of the detector.

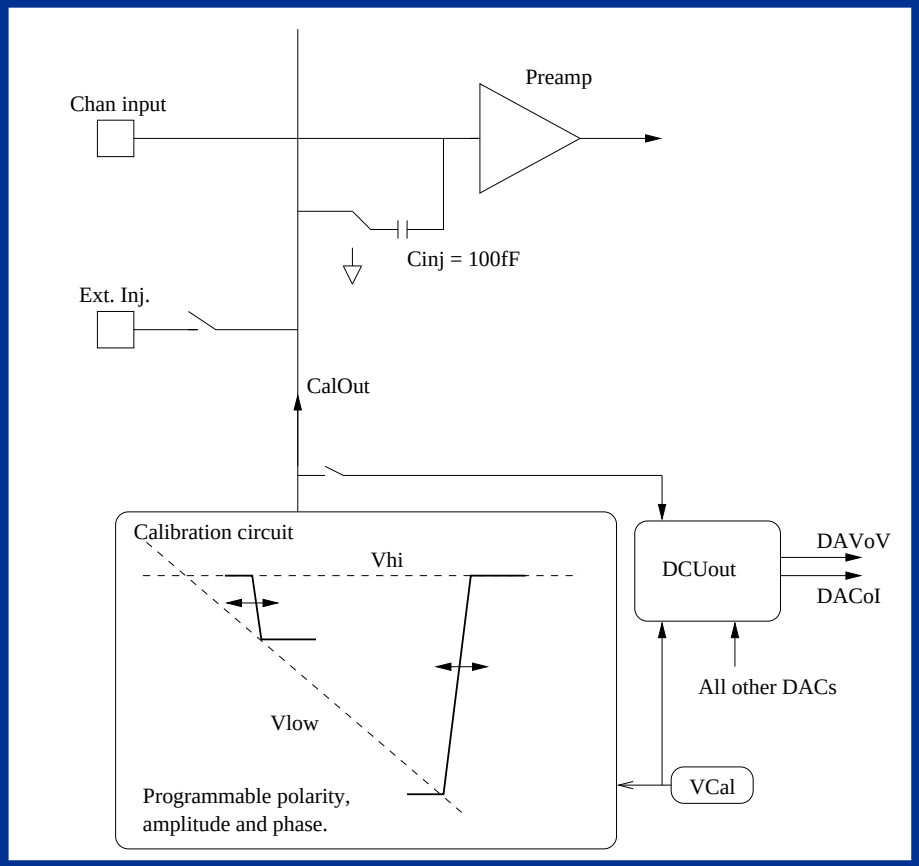
Calibration







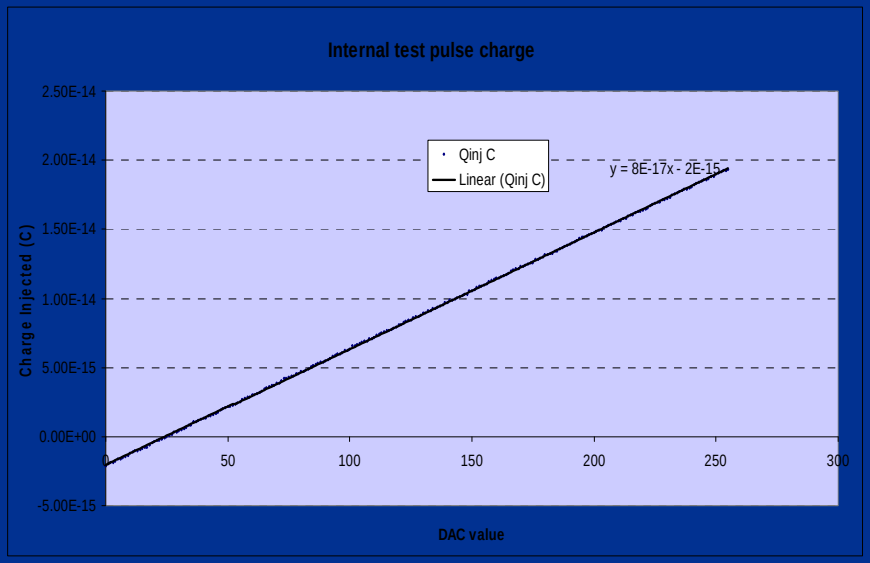
Internal Calibration Circuit



Injects a charge pulse to any one channel or group of channels selected by I^2C.

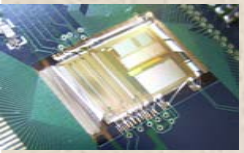
8 bit range

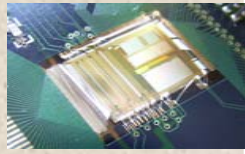
Linear fit Q-inj = $8^{-17}x - 2^{-15}$

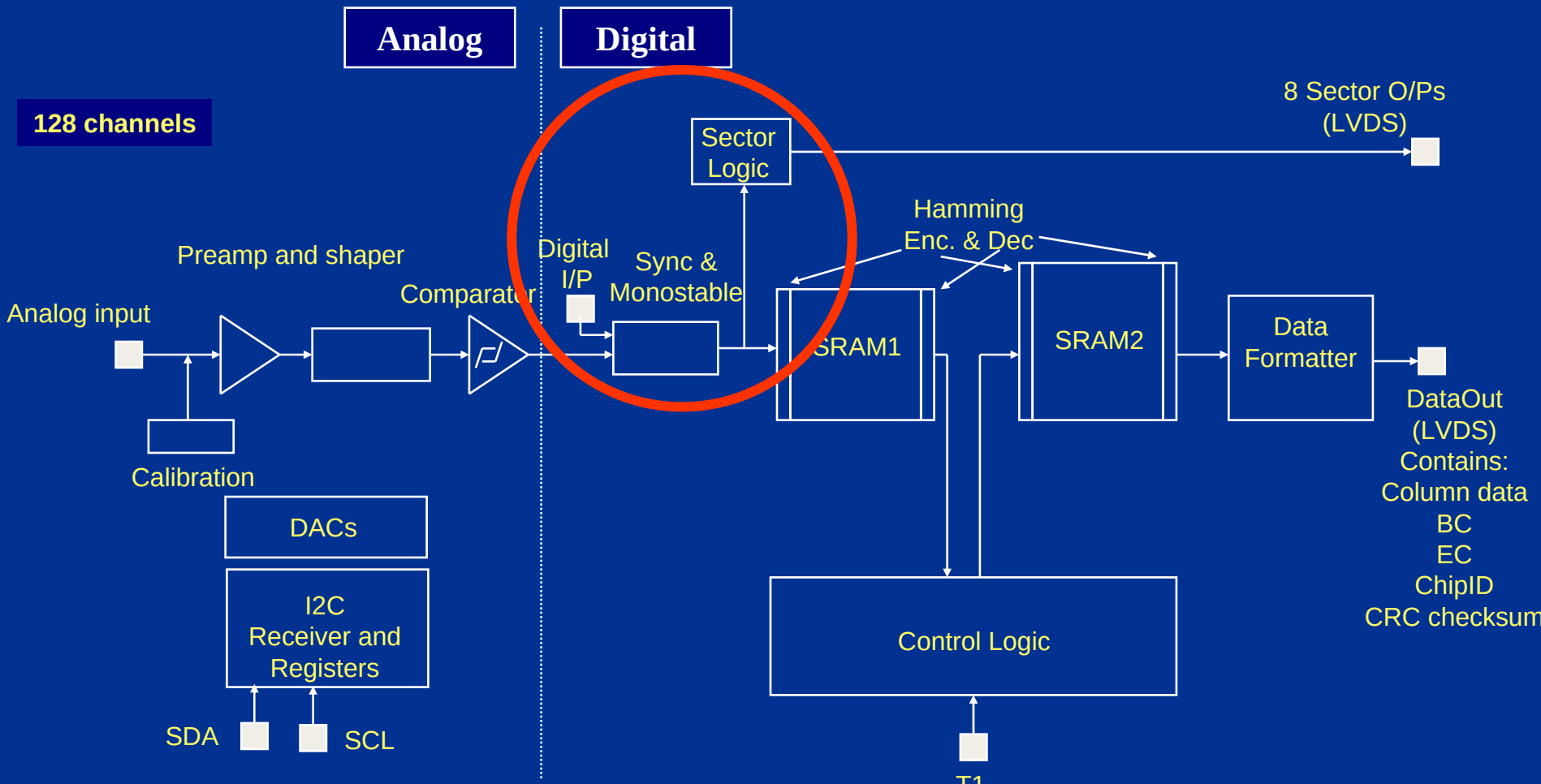


	Injection Range	LSB	σ (LSB)
Q	-2 fC to 18.5 fC	0.08 fC	0.3 fC

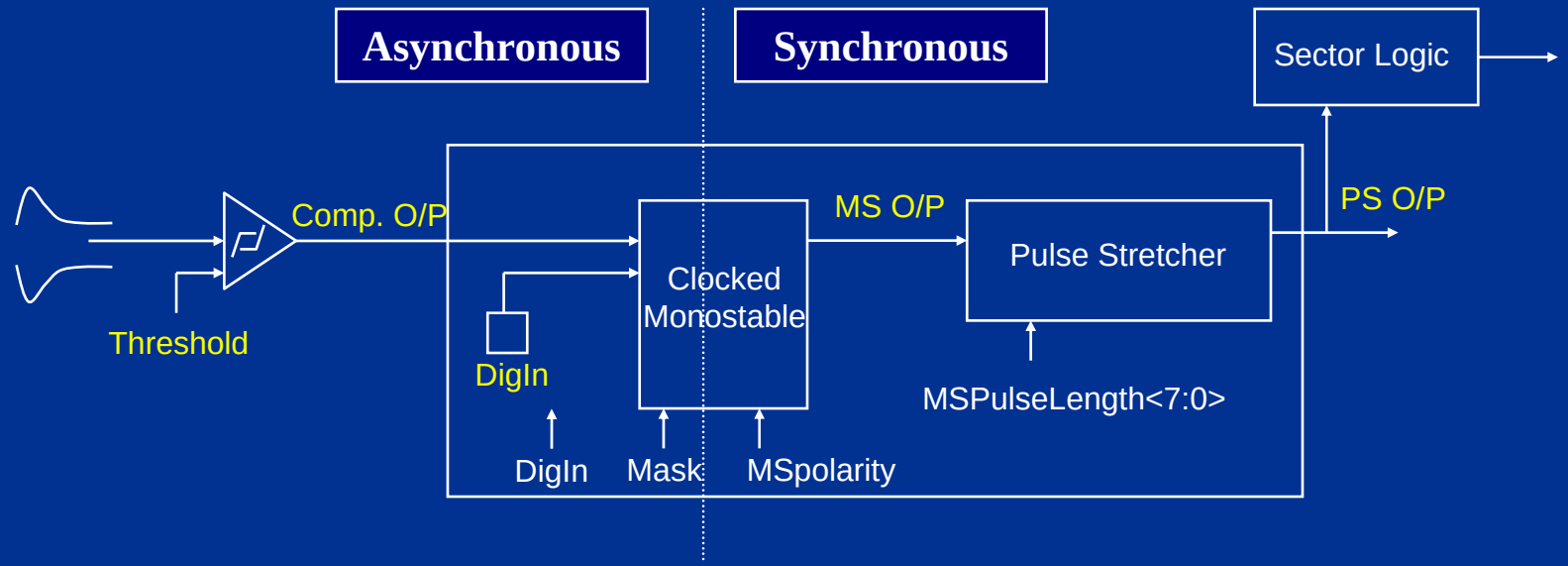
Synchronisation, Pulse Stretching & Sector Logic

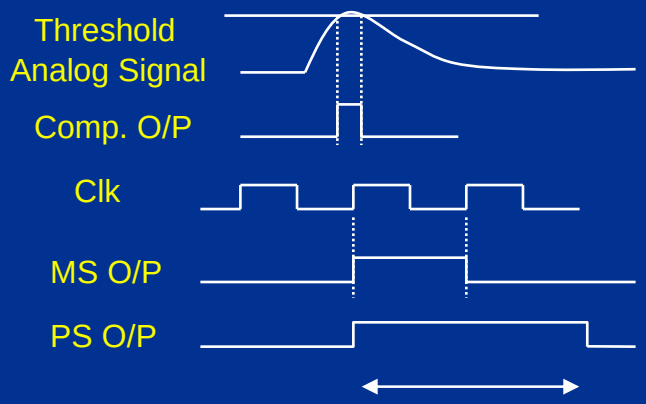


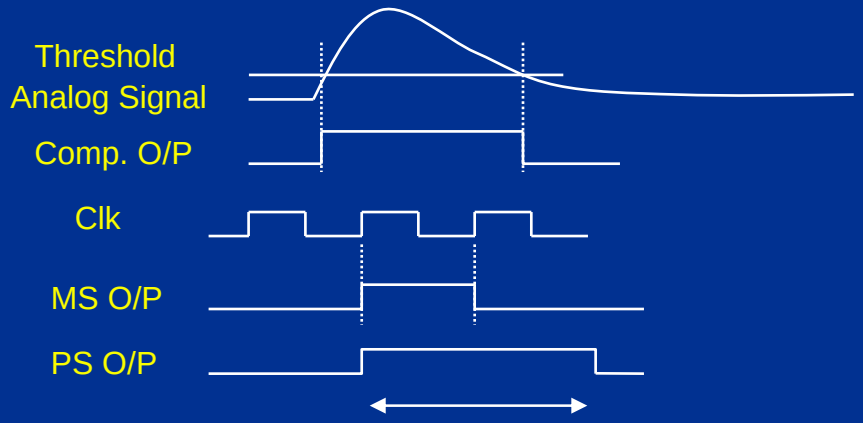




Synchronisation & Pulse stretching

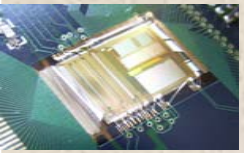


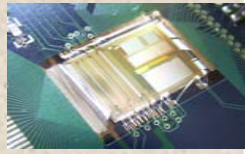


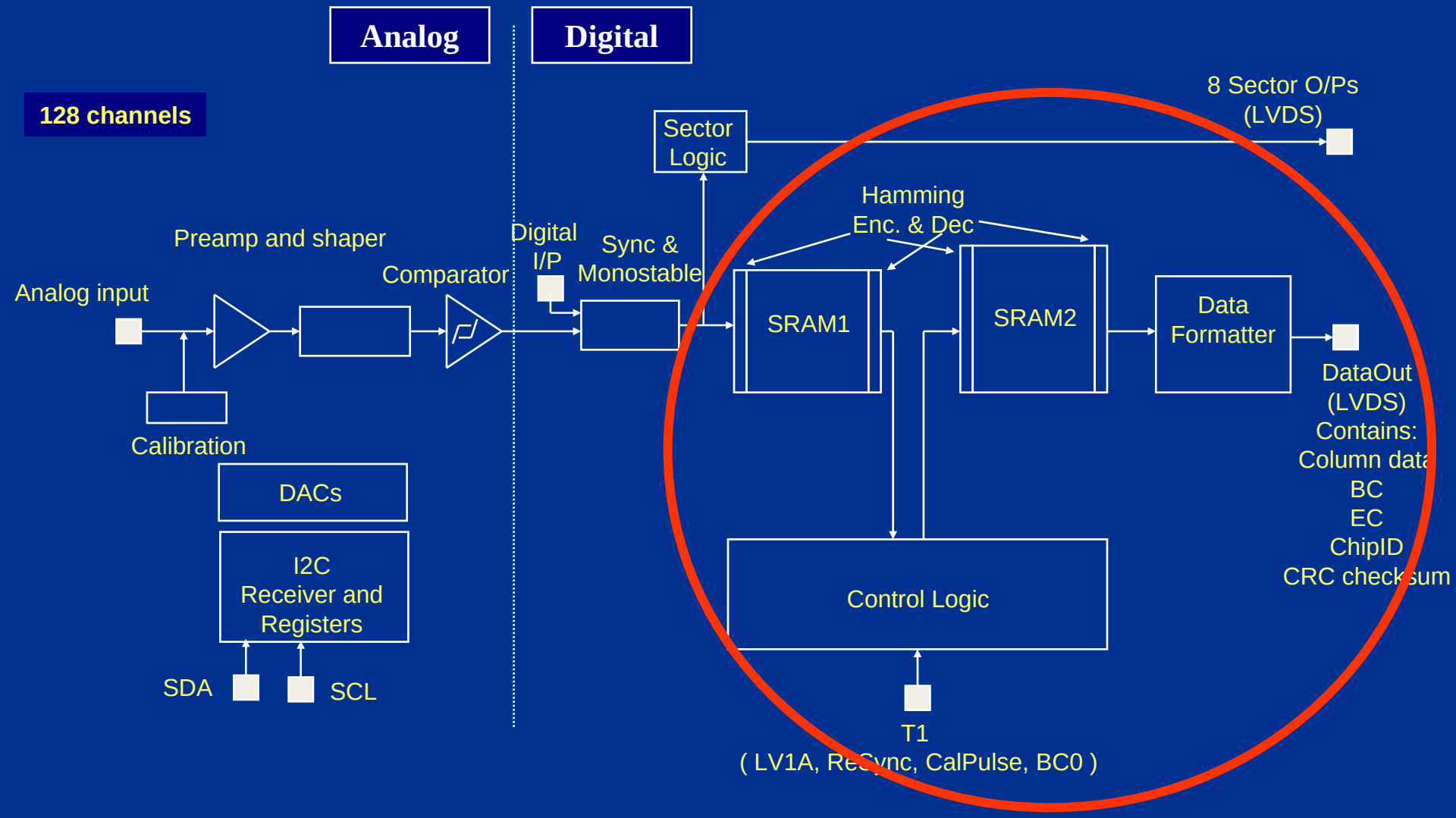


Pulse Stretcher O/P pulse length programmable from 1 to 8 clock periods

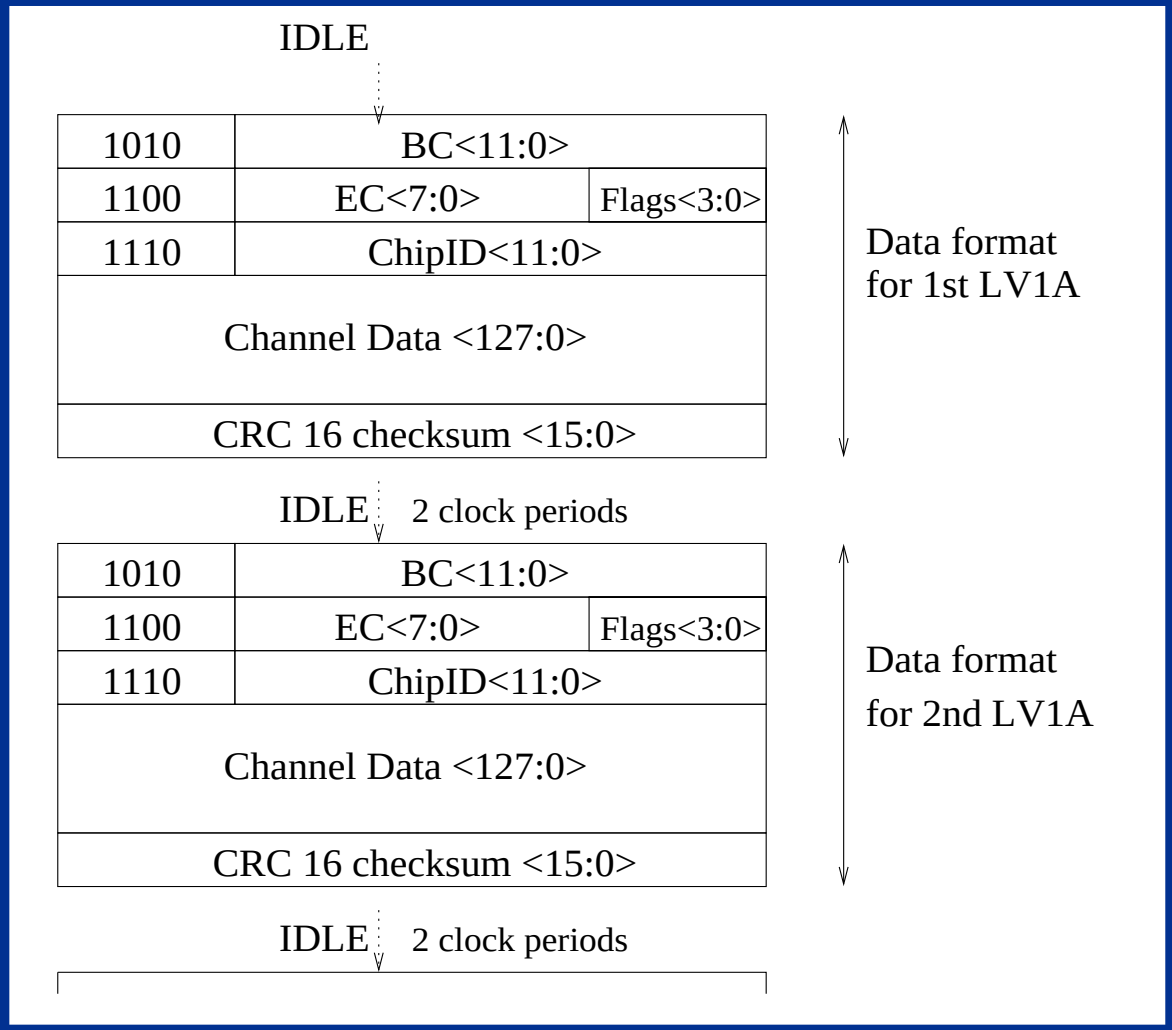
SRAMs, Control Logic and Data Formatter



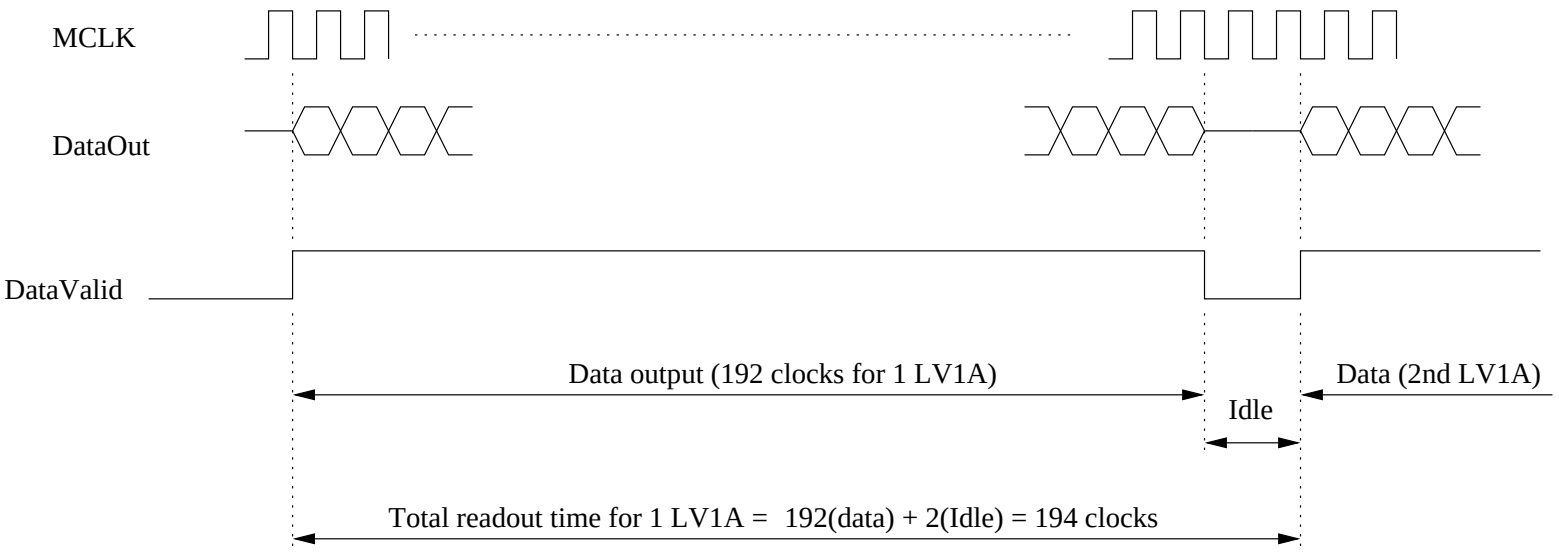




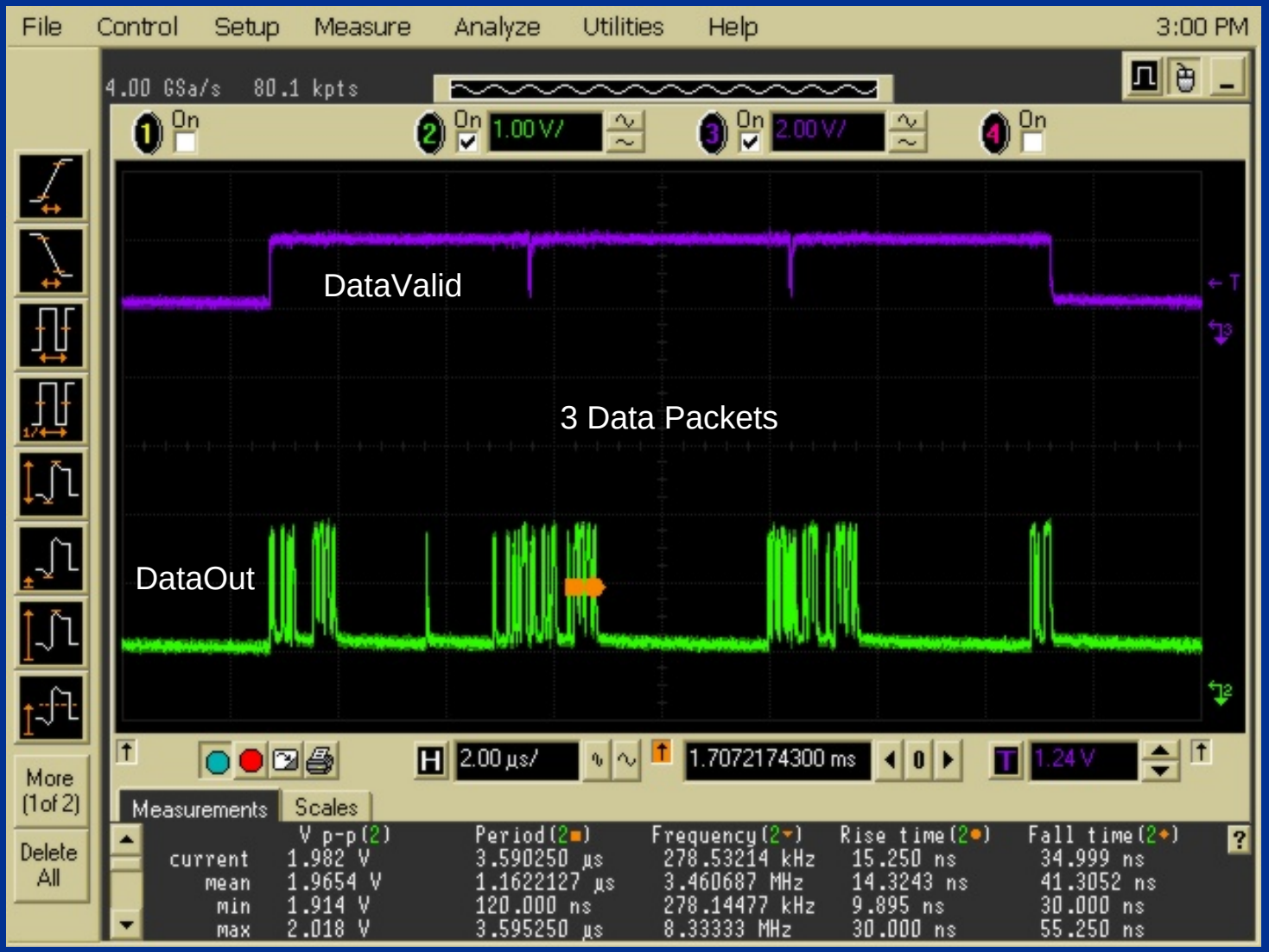
VFAT2 Data Format



VFAT2 Data Format



VFAT2 Data Packet on the output



VFAT2 noise results with &without detector

Noise Results without detector

Noise over all 128 channels ……. <ENC> = 589 electrons rms, ENC spread (σ) = 14.26%

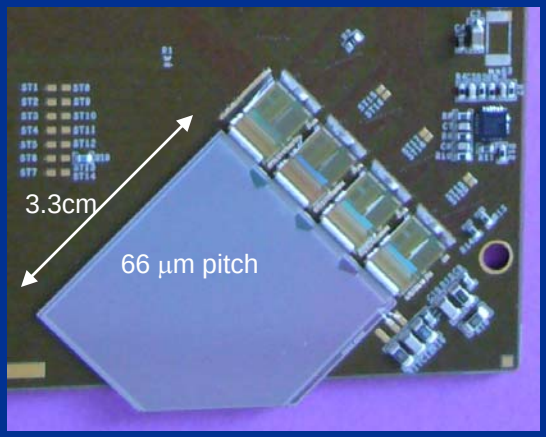
Threshold chosen = 5909 electrons (0.945 fC)

Threshold spread over 128 channels = 1.8% (without trimming DACs)

Min. Threshold = 0.7 fC (4375 e)

Max. Threshold = 18.7 fC (116875 e)

Noise Results with a silicon detector

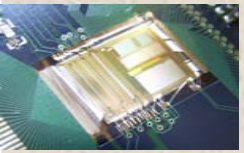


Noise over all 128 channels ….. <ENC> = 933 electrons rms, ENC spread (σ) = 9%

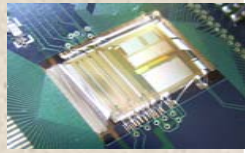
Threshold spread over 128 channels = 1.7% (without trimming DACs)

Noise increase of 344e

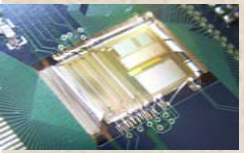
For 50 e/pF indicating additional capacitance < 7pF



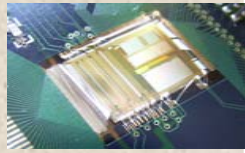
VFAT2 characteristics



Number of channels	128	
Front-end shaping time	22 ns	
ENC	~ 400 e + 50 e/pF	
Internal Calibration test pulse	-2 fC to 18.5 fC, LSB = 0.08 fC with σ(LSB) = 0.3fC	
Sampling frequency	40 MHz	
LV1A Latency	Up to 6.4 us	
Trigger rates	Up to 200kHz continuous trigger rate.	
Storage capacity	128 triggered events	
Slow Control interface	I^2C	
Testability features	Scan Chain, BIST, Probe pads, Auto test patterns, Auto Data Packet,	
Power Consumption	168 mW (Sleep Mode)	572 mW (Run Mode)
	Properties for 300um silicon detectors	Properties for TOTEM GEM detectors
Dynamic range	± 18 fC	35 fC to 45 fC
Threshold range	18 fC	30 fC
Trim-DAC range	40% of threshold range	
Recovery time after large signals	1us after 100 fC (delta pulse)	



Specific VFAT features for operation with gas detectors



- **Enhanced input protection on all 128 channel inputs.** Each channel has input protection diodes to protect the chip from detector discharge.

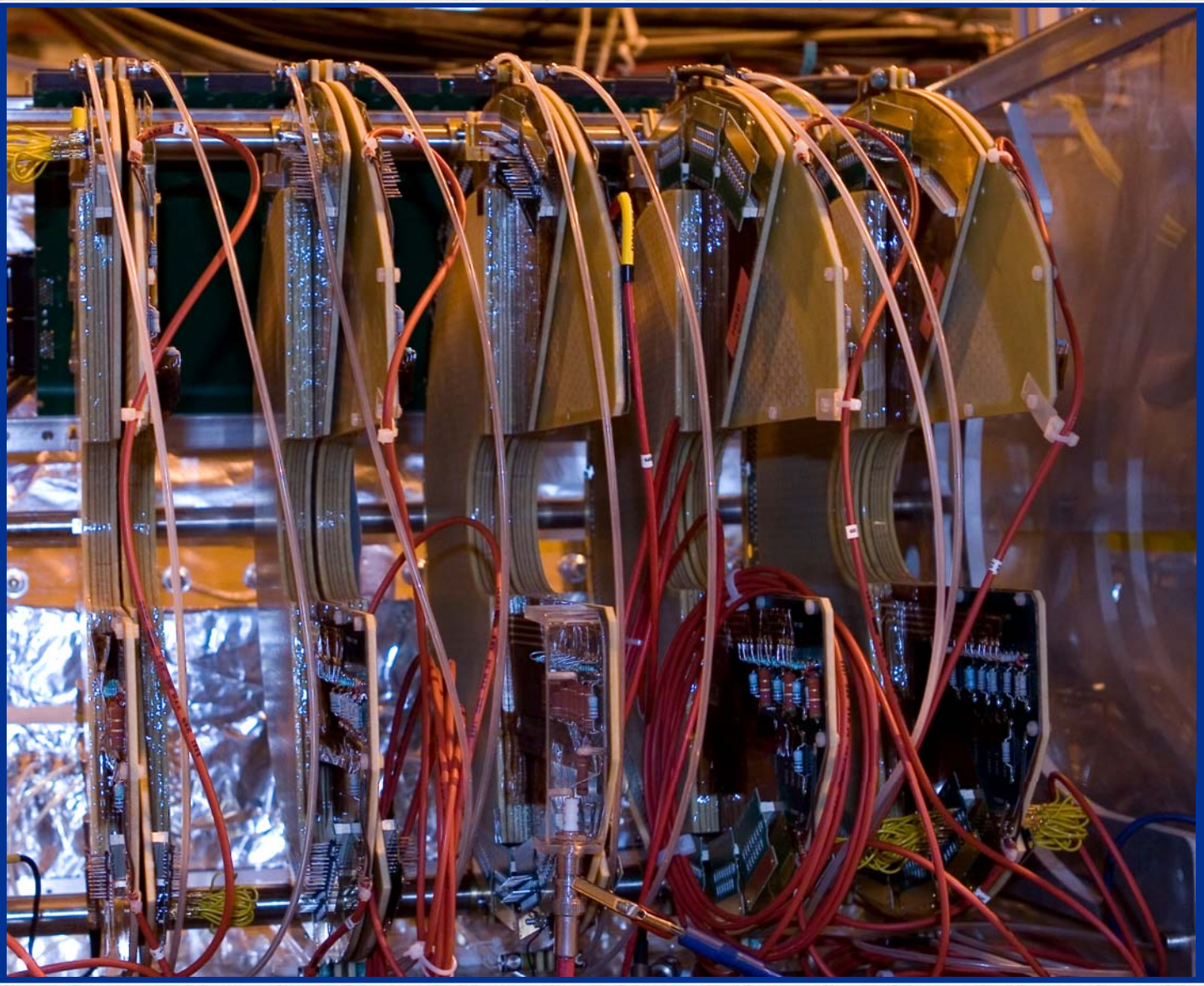
- **Positive or negative input charge.** Preamplifier and shaper operation with both positive and negative input charge.

- **Calibration with positive and negative charge.** The polarity of the calibration pulse is programmable.

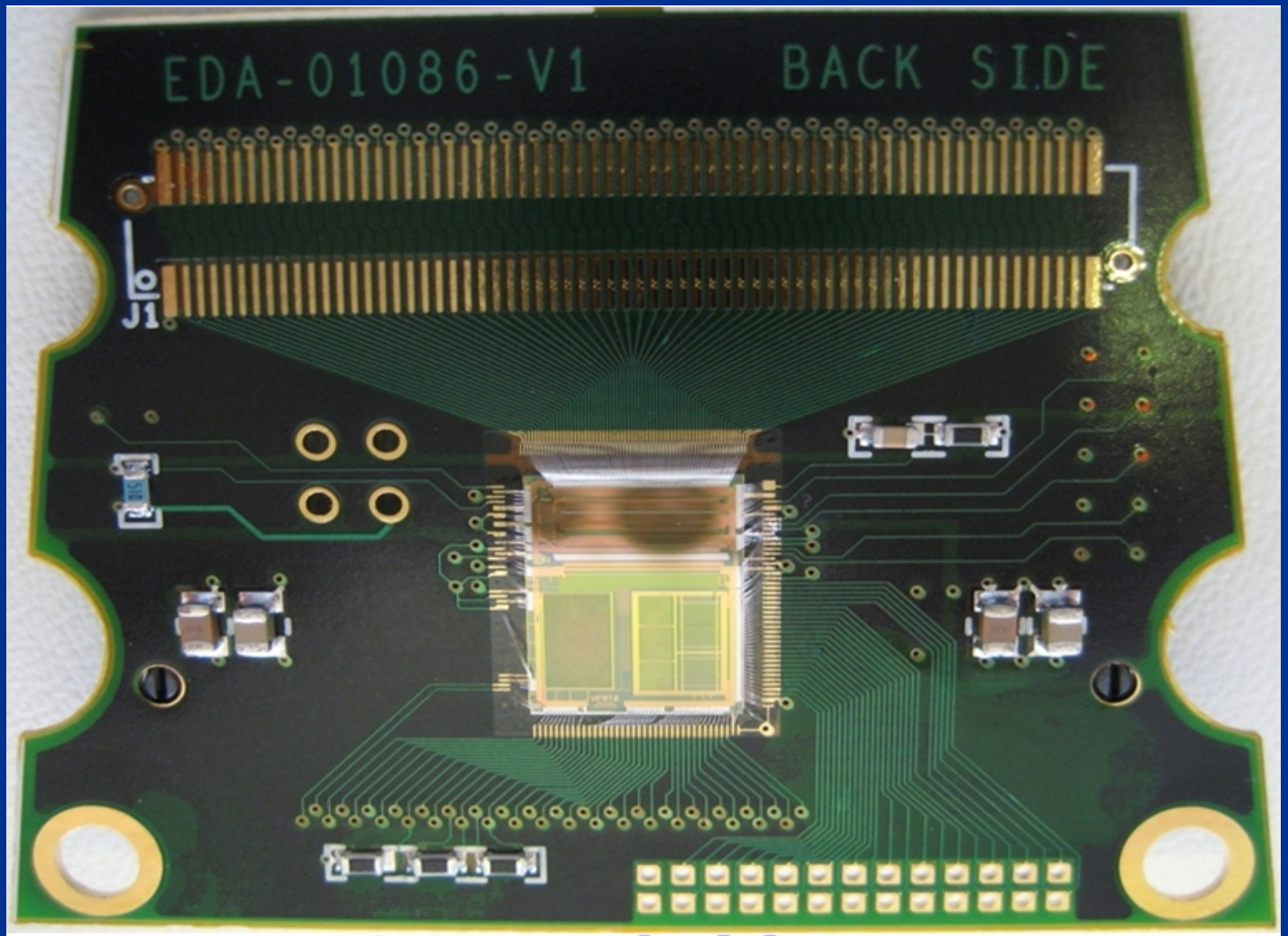
- **Direct "digital" input possibility** In the case that an alternative front-end is used there is the possibility to bond directly to the input of the digital part and hence by-pass the analog front-end.

- **Monostable length** Gas detectors have a larger time walk on both rising and falling edges of the signal compared to silicon. In synchronous systems this can lead to ambiguity on which time slot the event belongs to for a given level 1 latency. In VFAT the duration of the monostable pulse can be adjusted from 1 to 8 clock periods. This spreads the result of the hit over multiple time slots enabling 100% capture of the signal.

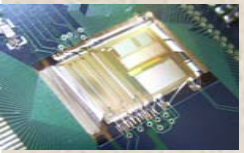
The T2 GEM detector



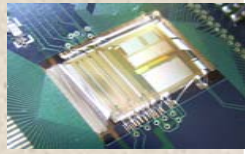
VFAT GEM hybrid



GEM Hybrid - V1



The TTP



A stand-alone, USB controlled VFAT Test Platform

Paschalis Vichoudis……. Hardware & firmware

Wojciech Bialas…….. Software consultant

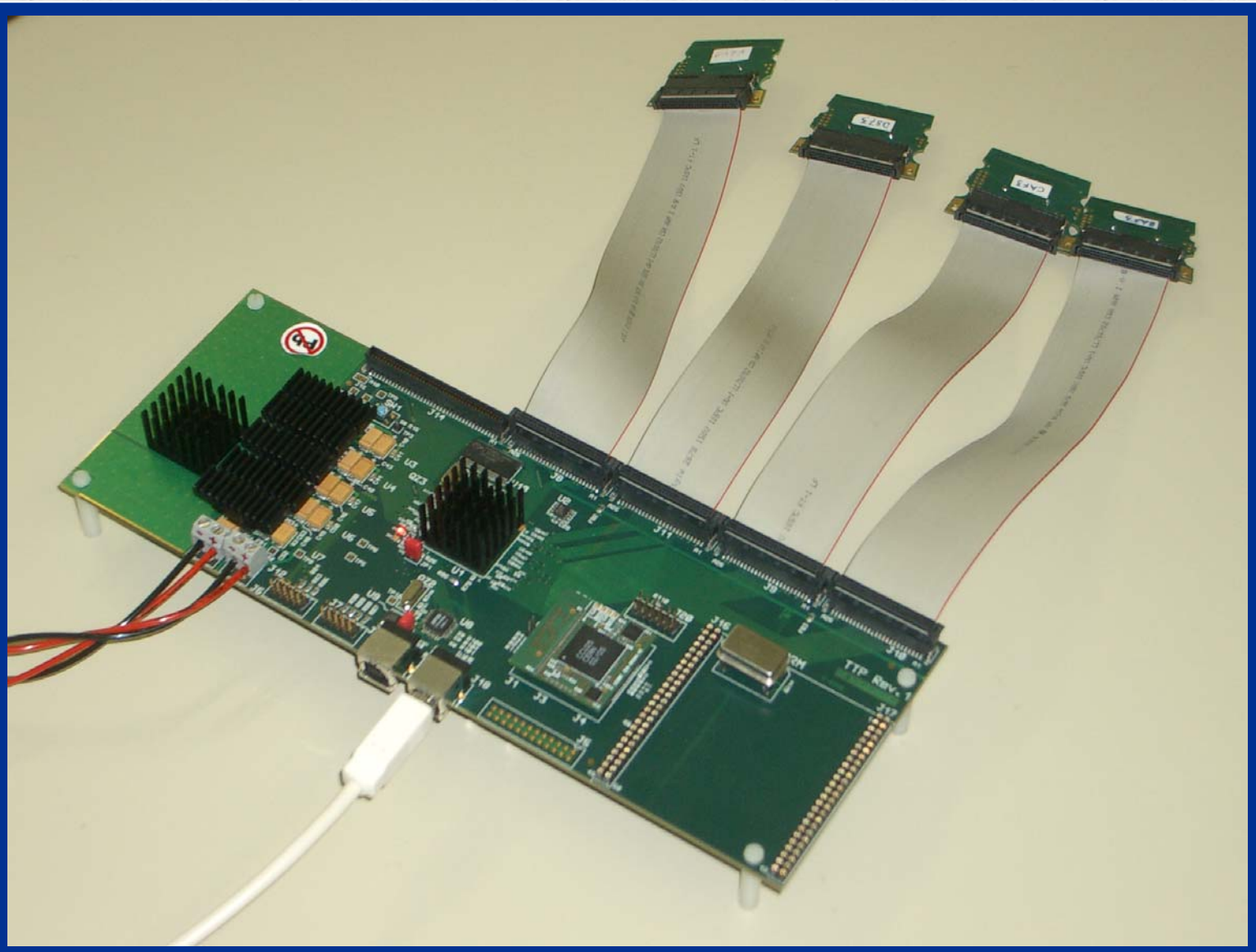
Juha Petaejaejaervi …….. Software

The TTP firmware & software development is largely based on a existing system, the **C**ontrol & **R**eadout **E**mulator for the **P**reshower **E**lectronics (CREPE).

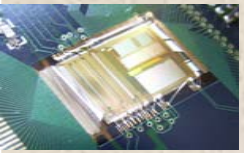
"A flexible stand-alone test bench for facilitating system tests of the CMS Preshower", Proceedings of the 10th Workshop on electronics for LHC and future experiments, Boston (2004), CERN-LHCC-2004-030 (2004), 127.

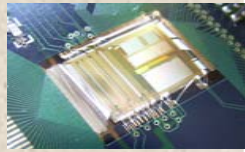
"The control & readout emulator for the Preshower electronics (CREPE): user's guide", CMS IN 2005/049.

The TTP with 4 GEM hybrids



VFAT2 I²C Control Panel





VFATDebugger - Beta Version

Control | Tests

Chip ID: 0xee73

Position

FEC: 0,0 | CCU: 0x7F | I²C Channel: 0x10 | Device: 0x10

Control Registers

	CalMode	CalPol	MSPol	TrigMode	Run
CR0 :	Normal	+ve	+ve	No Trig	Run
	ReHitCT	LVDSPowerSave	ProbeMode	DACsel	
CR1 :	6,4 µs	OFF	OFF	OFF	
	DigInSel	MSPulseLength	HitCountSel		
CR2 :	An I/P	1 clock	Fast OR		
	DFTestPattern	PbBG	TrimDAC-range		
CR3 :	OFF	OFF	0		

Biasing

IPreampIn	0	Latency	0
IPreampFeed	0	VCal	0
IPreampOut	0	VThreshold 1	0
IShaper	0	VThreshold 2	0
IShaperFeed	0	CalPhase	135 °
IComp	0		

Counters

Upset	0
HitCount 0	0
HitCount 1	0
HitCount 2	0

Read Counters

Channel Register #1

Cal 0 | Cal 1 | Mask | TrimDAC: 0

Other Channel Registers

CH #: 2 | Cal | Mask | TrimDAC: 0

Change this one | Change to all

Commands

Scan for FECs and CCUs

Initialize VFAT access

Chip

Read | Write

Compare written values

Select all registers

Select none

XML

File :

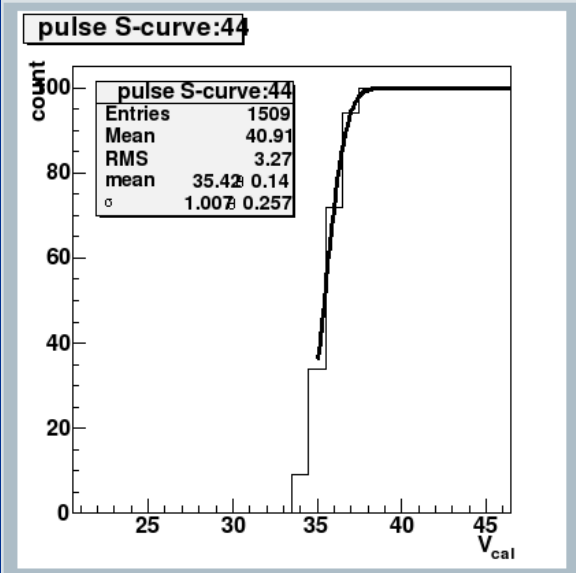
Load | Save

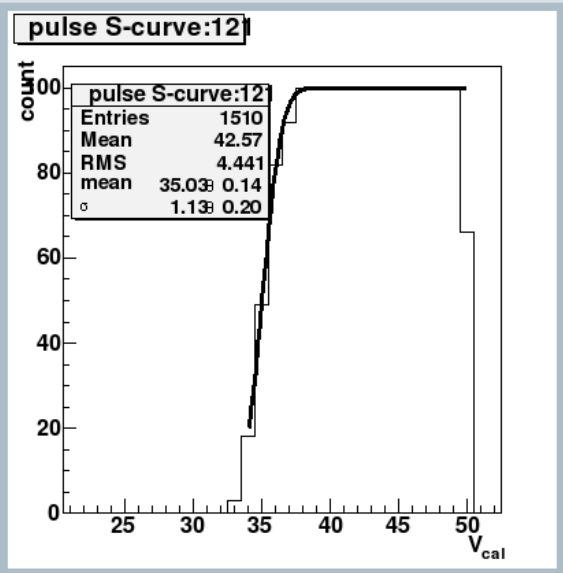
Show Array in Console

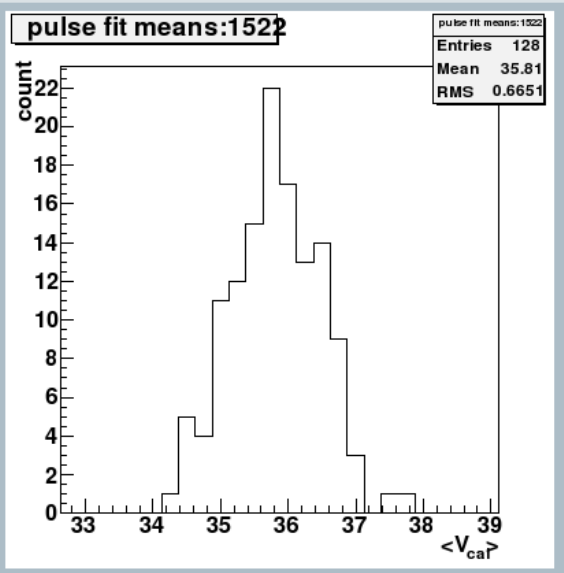
About | Quit

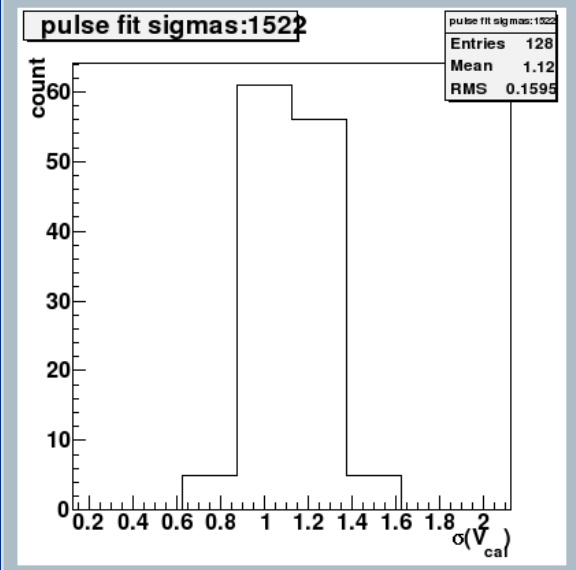
Software written by Juha Petaejaejaervi

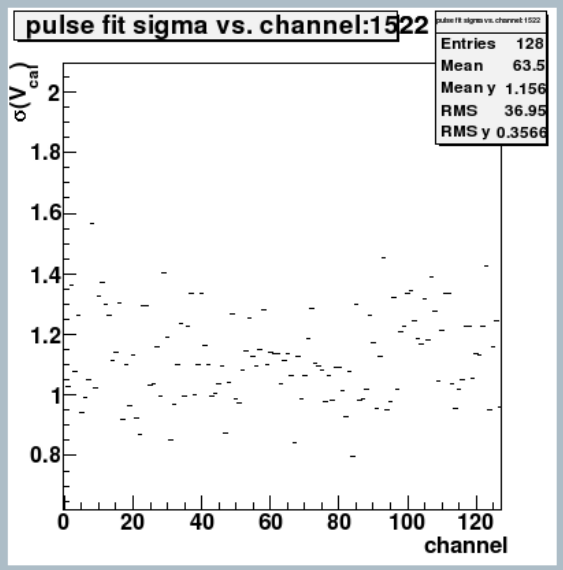
S-Curve on all channels

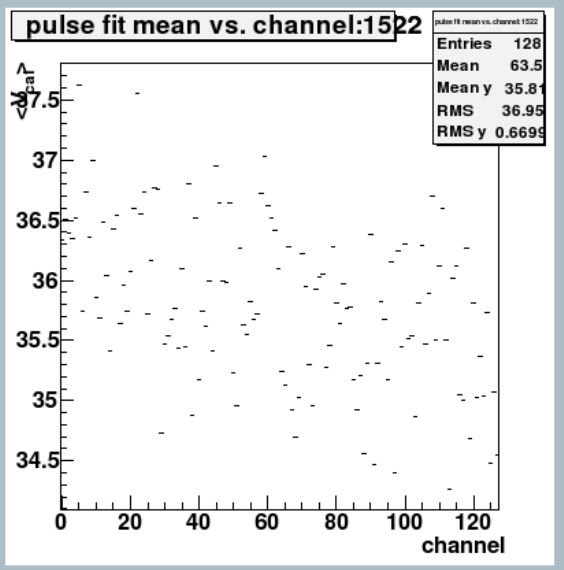




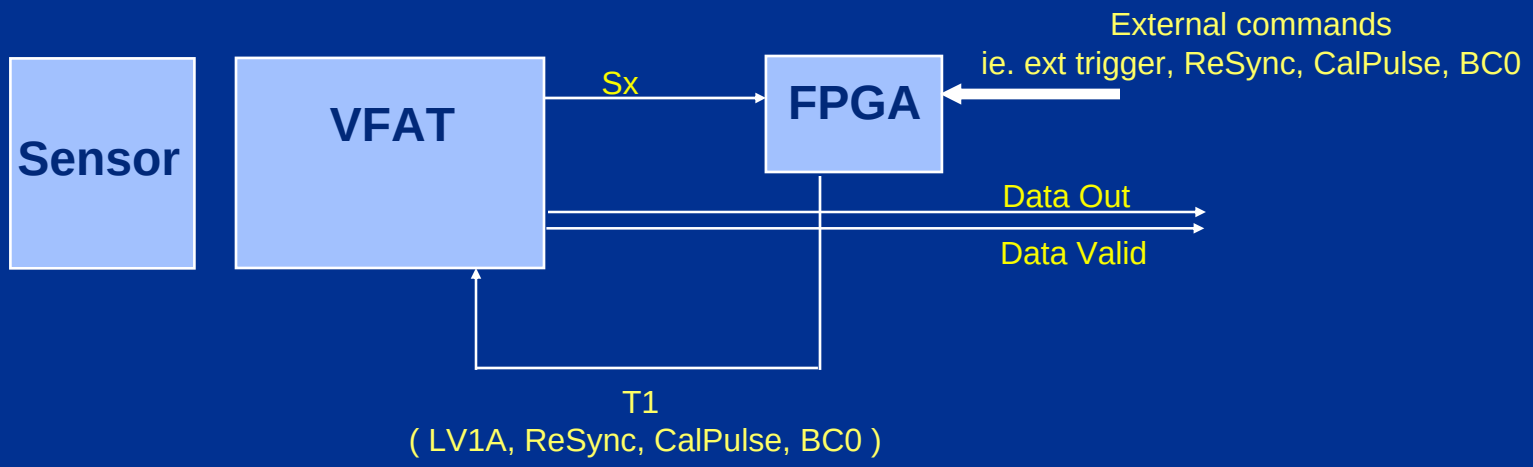




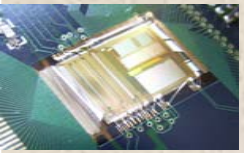




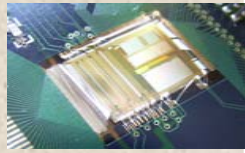
Stand Alone (self triggered) system



VFAT can operate as a stand alone (self triggered) system. The “sector” outputs (Sx) will signal hits seen by VFAT. An FPGA then constructs the T1 signal (100) to send back to VFAT as a trigger. The latency for a self triggered system can be as short as 4 clock cycles.



Projects expressing interest in using VFAT

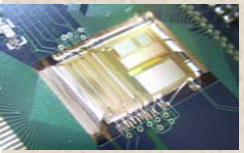


TOTEM : Currently using VFAT for the readout of silicon and GEM detectors.

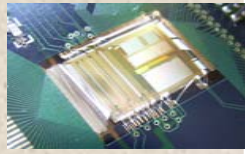
HEP:
Trigger detector for Alice. Potentially thousands of chips needed.
CMS MPGD Track and trigger : Potentially thousands of chips needed.
Tracking of a CSR (cooling storage ring).
Qweak experiment for GEM readout. 100 chips needed.
4 plane silicon telescope, ~ 40 chips

Non HEP:
X-ray imaging using GEMs.
X-ray diffraction studies using GEMs, up to 200 chips.
Imaging for proton therapy, ~ 50 chips needed ?

All groups require a few samples to start with for initial tests.



Summary



The VFAT chip provides charge sensitive readout for silicon and gas particle detectors.

The chip design alone represents more than 5 man years of design effort.

VFAT is highly programmable and versatile.

It is rare that a chip design reaches the sophistication of VFAT and we believe that it could be of use in many applications other than it's initial design application.