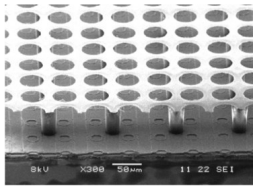
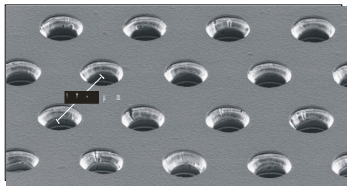
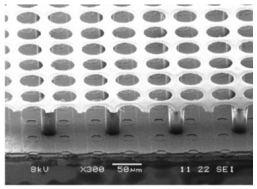




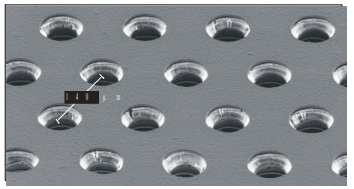
Summary WG5

J. Kaminski

RD51 Collaboration Meeting, 23rd – 25th November 2009
CERN

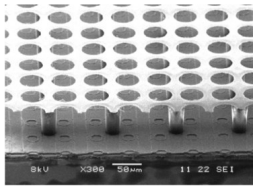


5 tasks of WG5

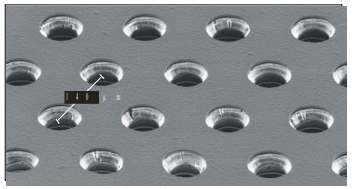


(1) Definition of front end electronics requirements for MPGDs;
(2) Development of general purpose pixel chip for active anode readout;
(3) Development of large area detectors with pixel readout;
(4) Development of portable multichannel data acquisition systems for detector studies;
(5) Discharge protection strategies

During the parallel session:
11 talks addressing 4 of the tasks



Task 4



Development of portable multichannel data acquisition systems for detector studies;

The 'Scalable Readout System' is designed by several members of the working group

4 contributions

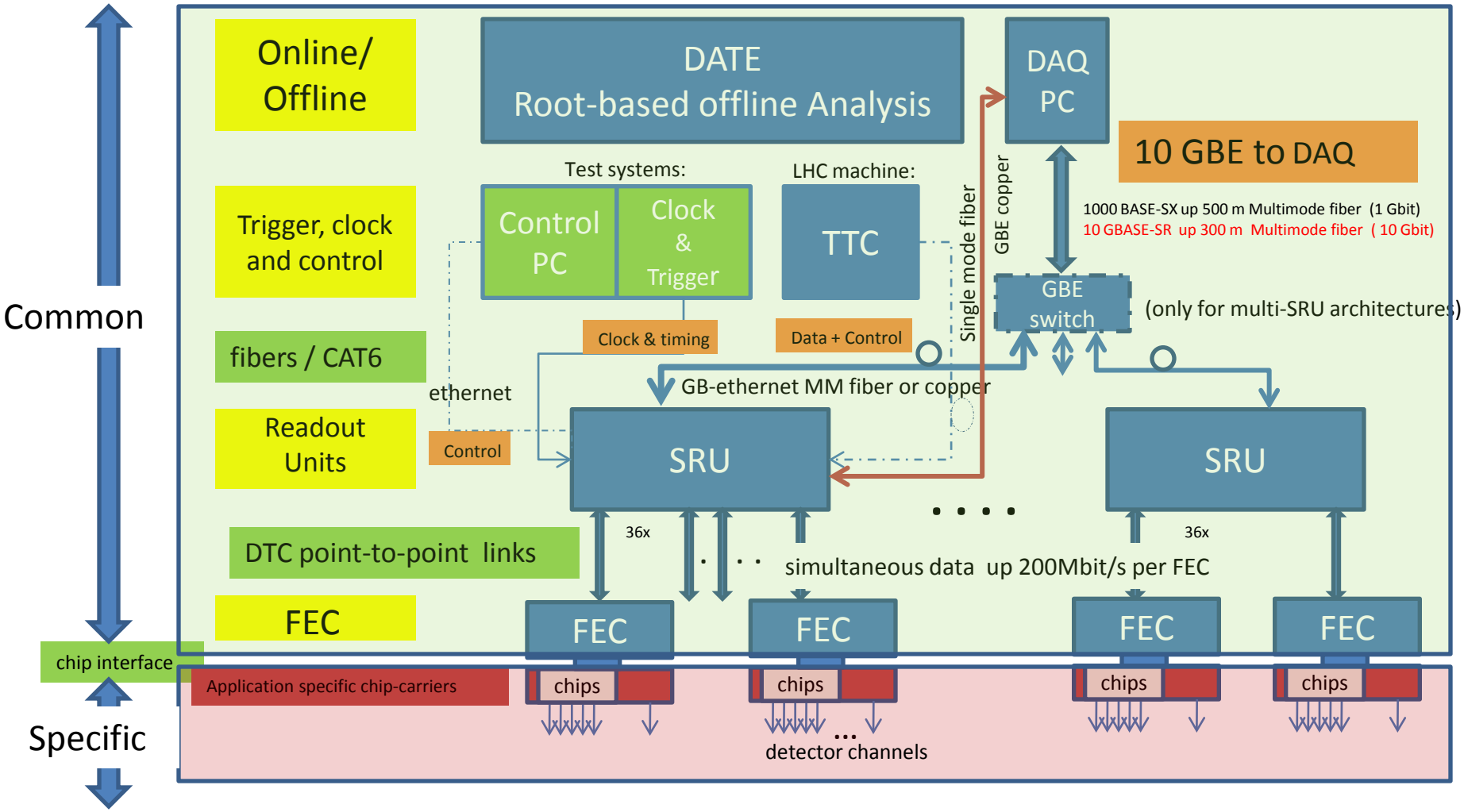
+ 1 contribution presenting a readout system for GEM detectors.

Sofar development driven by '2 main users':

ATLAS-upgrade Micromegas detector

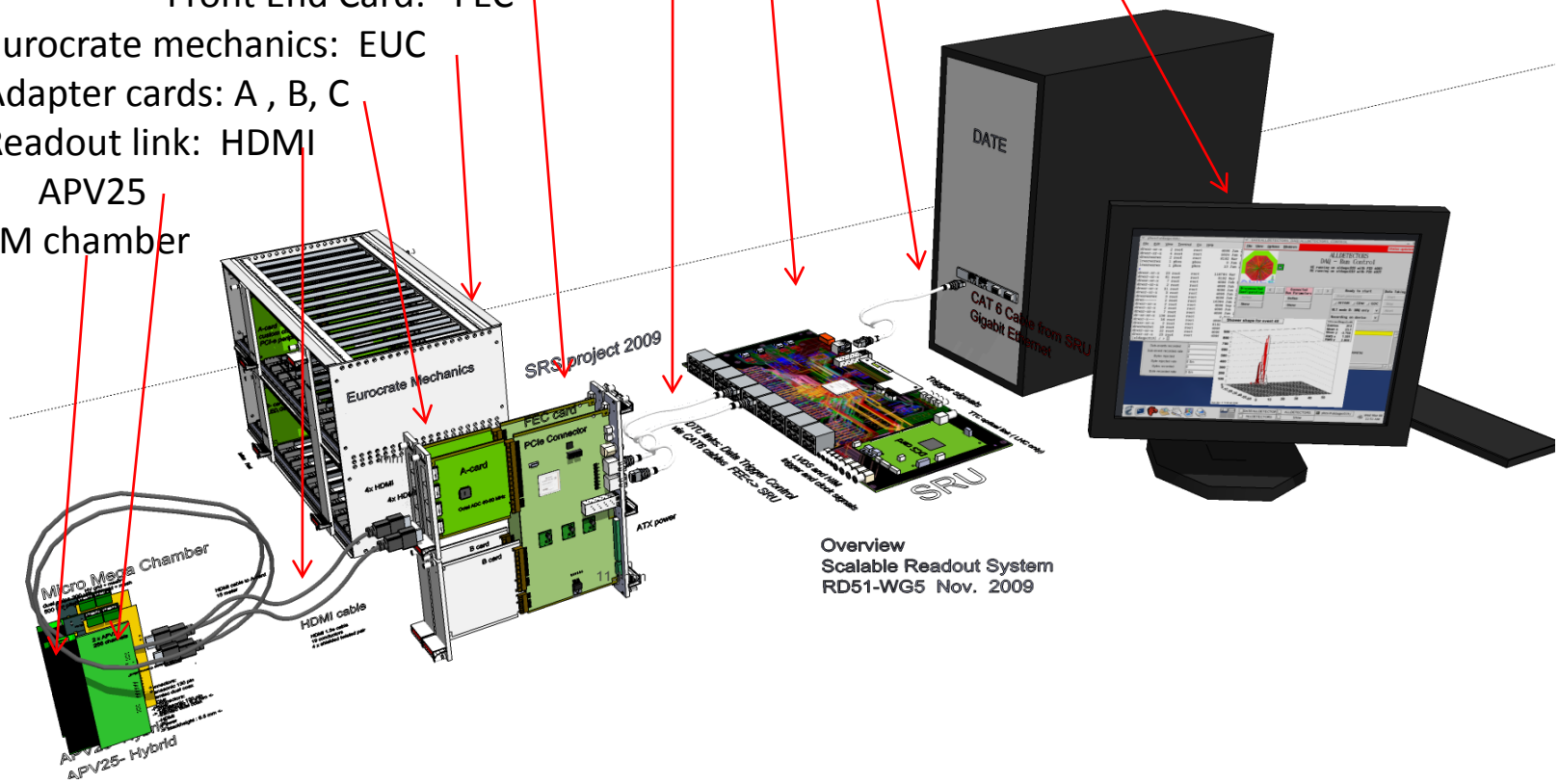
NEXT experiment

SRS proposal revisited

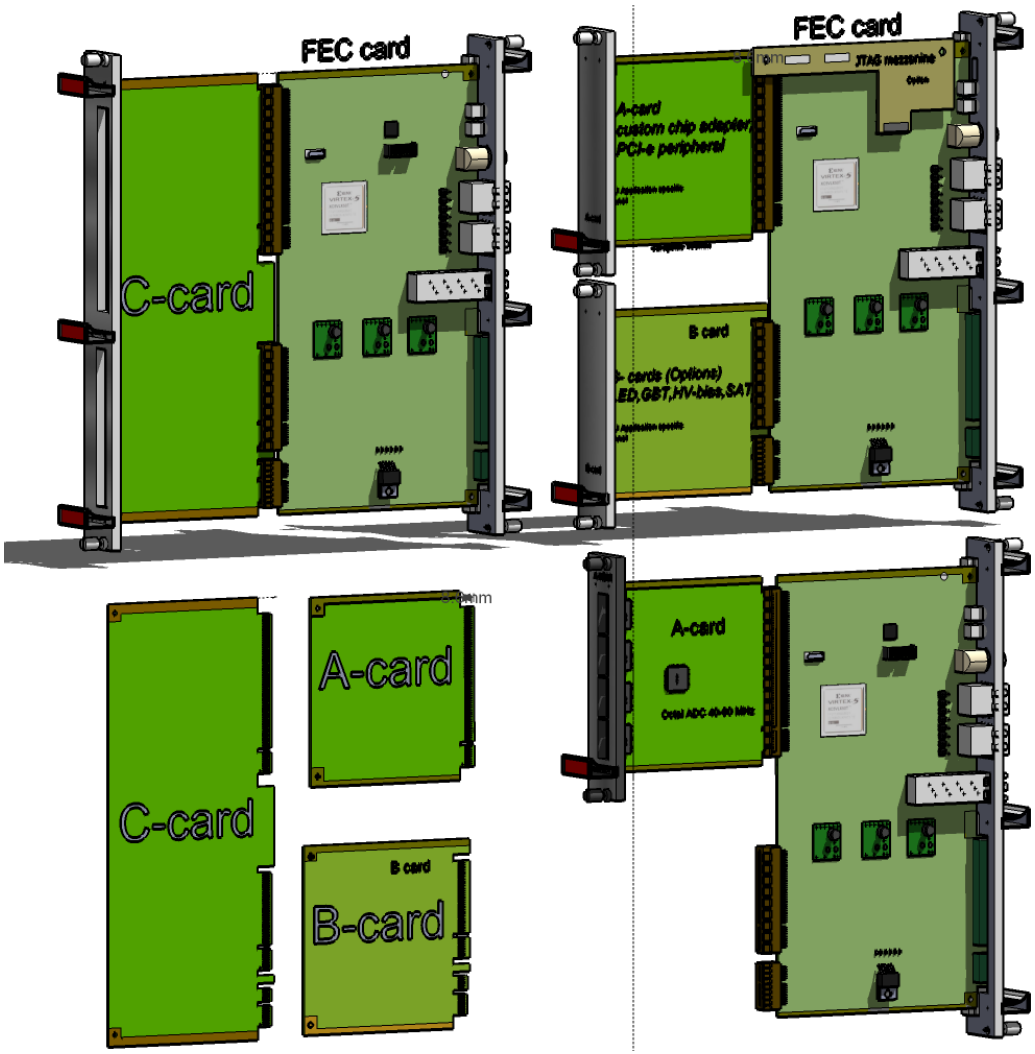


SRS 2009 Overview

Readout DAQ System: DATE
Readout links: Gigabit Ethernet
Large systems link concentrator: SRU
Data Trigger Control links: DTC
Front End Card: FEC
Eurocrate mechanics: EUC
Adapter cards: A , B, C
Readout link: HDMI
Chip carrier: APV25
Detector: MM chamber



SRS adapter card “Lego”



All dimensions and system-connector are defined now

A cards: chip readout adapter

B cards: small size Extensions

C cards: large size extensions

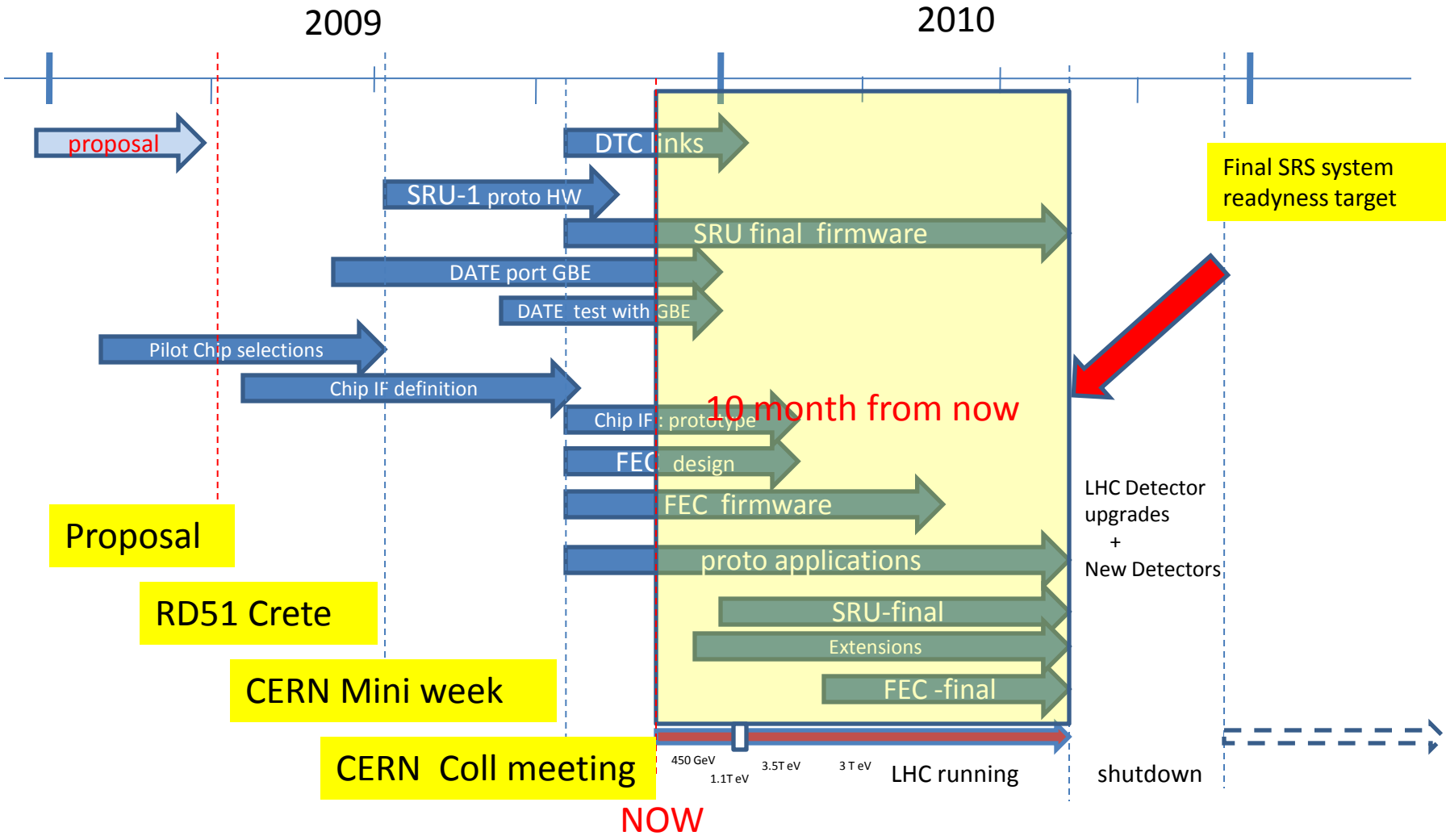
1st card will be A card for APV25

All can in principle be mixed in one EU crate

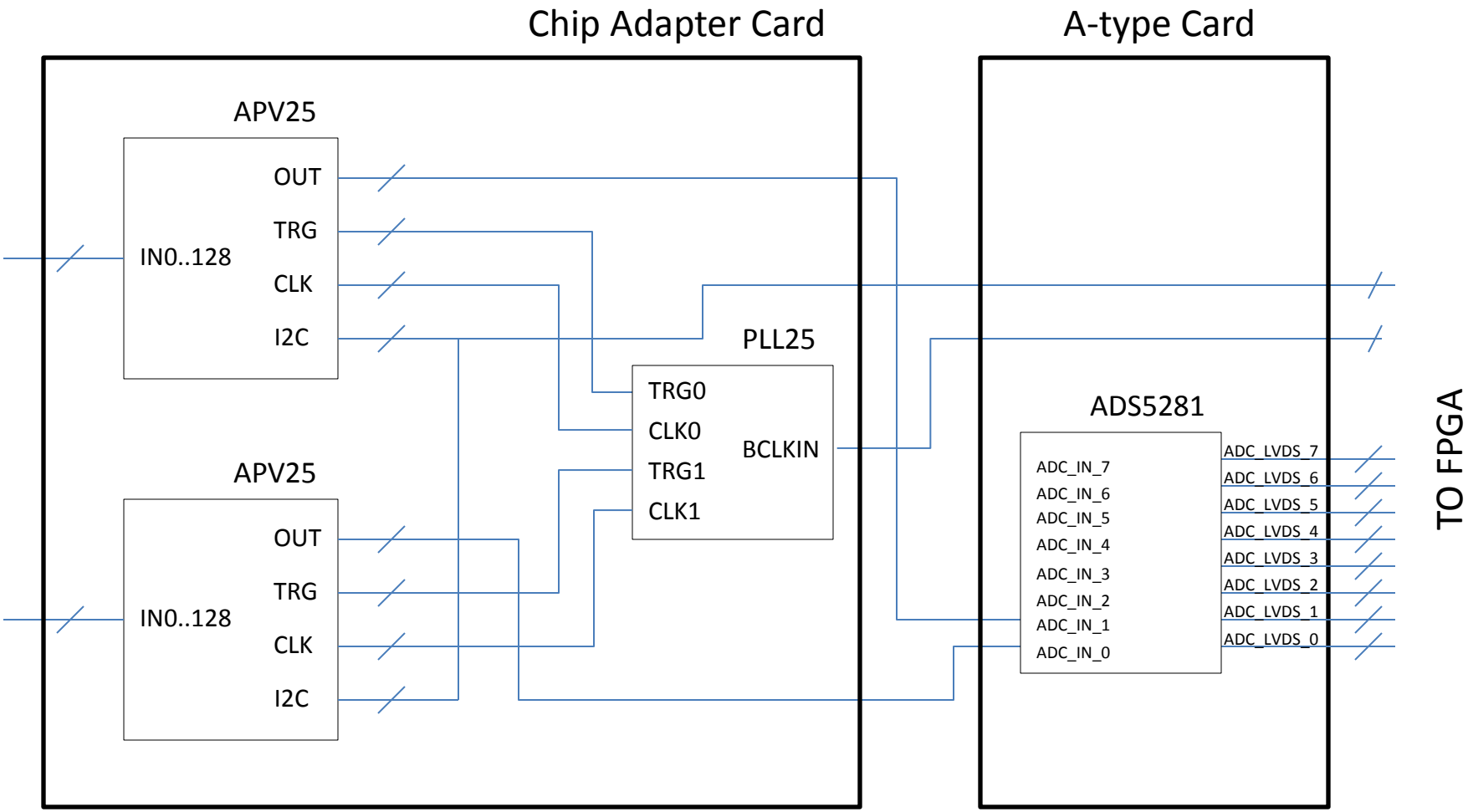
Extensions to be worked on

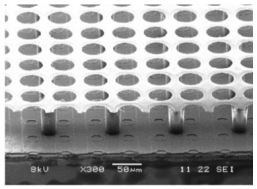
-Programmable HV for APD, SiPMs etc
- Programmable LED pulsers
- Adapters for subsystems like GBE or triggerless systems

updated SRS project timing
Nov. 23 2009 - @startup of LHC

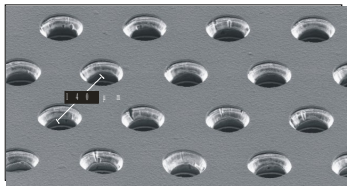


APV25 Chip Adapter

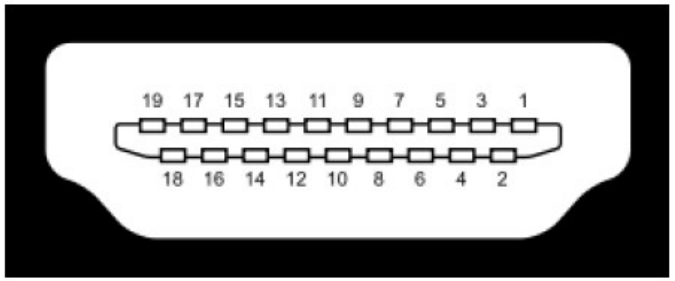




HDMI connection



Layout and specification



HDMI version	1.0–1.2a	1.3	1.4
Year	2002	2006	2008
Maximum signal bandwidth (MHz)	165 MHz	340 MHz	340 MHz
Maximum TMDS bandwidth (Gbit/s)	4.95 Gbit/s	10.2 Gbit/s	10.2 Gbit/s
Cable length	< 5m	< 15m	< 15m
Attenuation 300kHz - 825MHz 825MHz - 2.475GHz 2.475GHz - 4.125GHz 4.125GHz – 5.1GHz	 < 8dB < 21dB < 30dB - -	 < 5dB < 5dB...< 12dB < 12dB...< 20dB < 20dB...< 25dB	 < 5dB < 5dB...< 12dB < 12dB...< 20dB < 20dB...< 25dB
Differential Impedance	100 ohm ± 10%	100 ohm ± 10%	100 ohm ± 10%

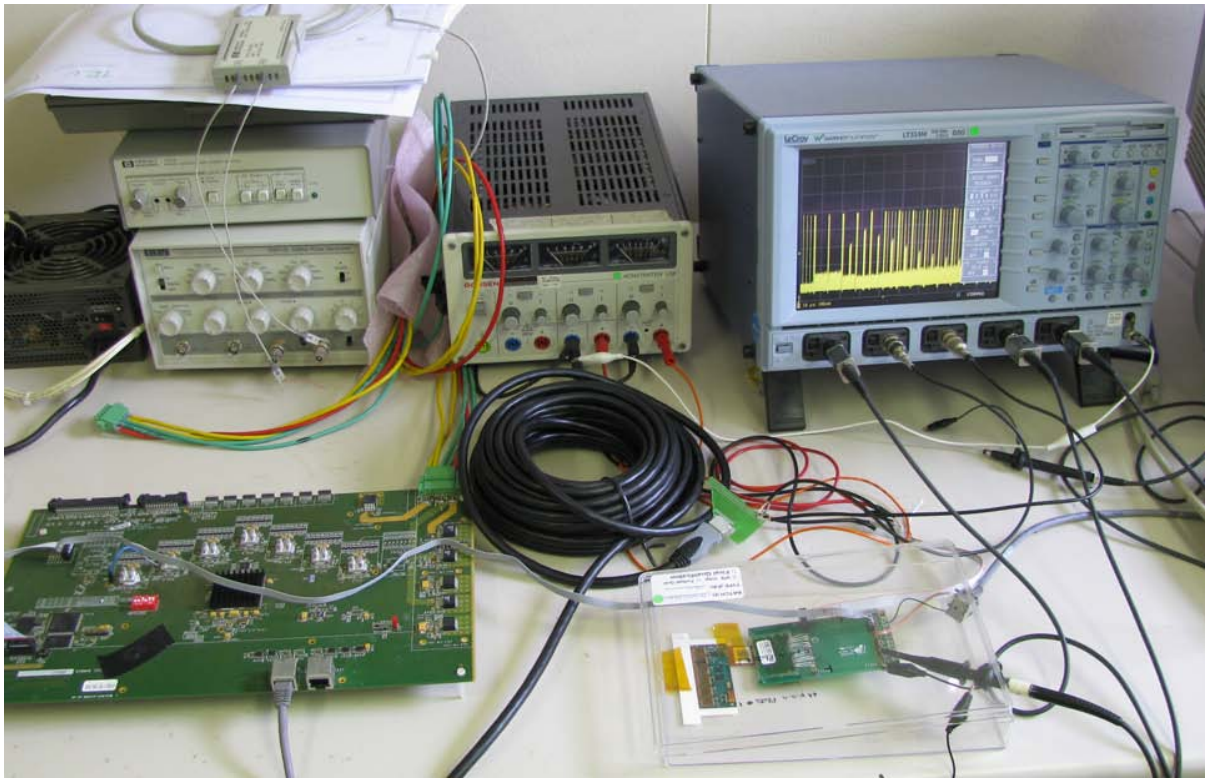
Position	HDMI Signal	APV25 Card	Beetle Card
Pin 1	TMDS Data2+	OUT 1+	OUT 1+
Pin 3	TMDS Data2–	OUT1-	OUT1-
Pin 4	TMDS Data1+	OUT2+	OUT2+
Pin 6	TMDS Data1–	OUT2-	OUT2-
Pin 7	TMDS Data0+	-	TRGOUT+
Pin 9	TMDS Data0–	-	TRGOUT-
Pin 10	TMDS Clock+	BCLK+	BCLK+
Pin 12	TMDS Clock–	BCLK-	BCLK-
Pin 13	CEC	RST_N	RESET
Pin 15	SCL (I²C Serial Clock)	SCL	SCL
Pin 16	SDA (I²C Serial Data)	SDA	SDA
Pin 19	Hot Plug Detect	-	Test Pulse

Pinout for
2 APV25/Beetle chips

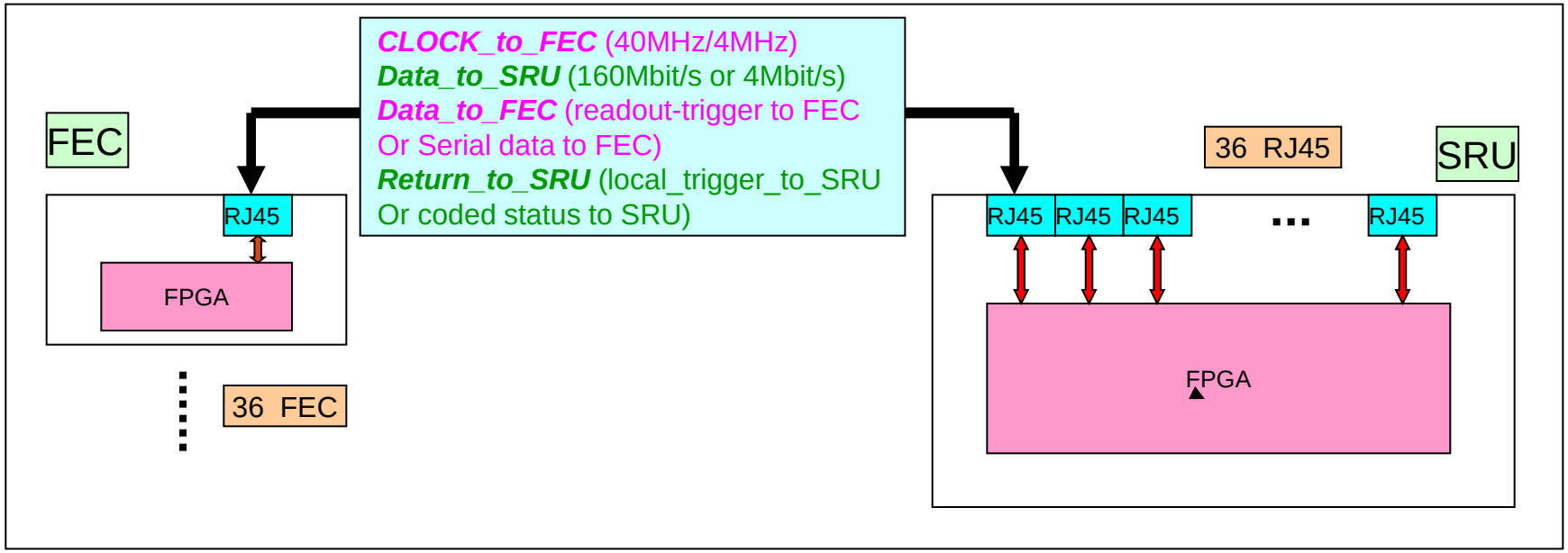
See talk on analogue chips
by S. Martoiu

Connection is already being tested

TestBench



DTC(Data-Trigger-Control) link

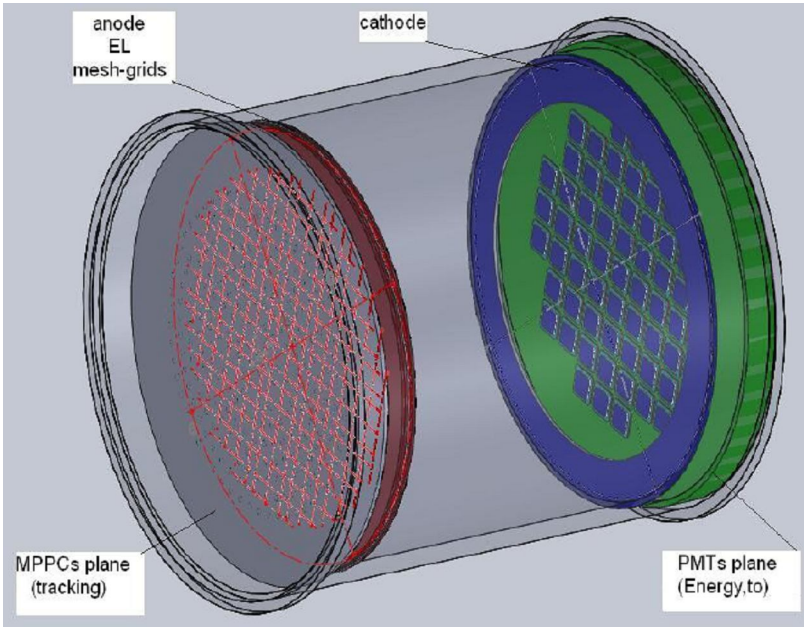


- ***Readout mode***
  - **Clock = 40 MHz to FEC**
  - **Data = 160 Mbit/s to SRU**
  - **Trigger = select = readout-trigger to FEC**
  - **Trigger =return = local trigger to SRU**

- ***Control mode***
  - **Clock = 4 MHz to FEC**
  - **Data_out = Serial data out to SRU**
  - **Data_in = Serial data in to FEC**
  - **Return = coded status to SRU (Error? Busy? ...)**

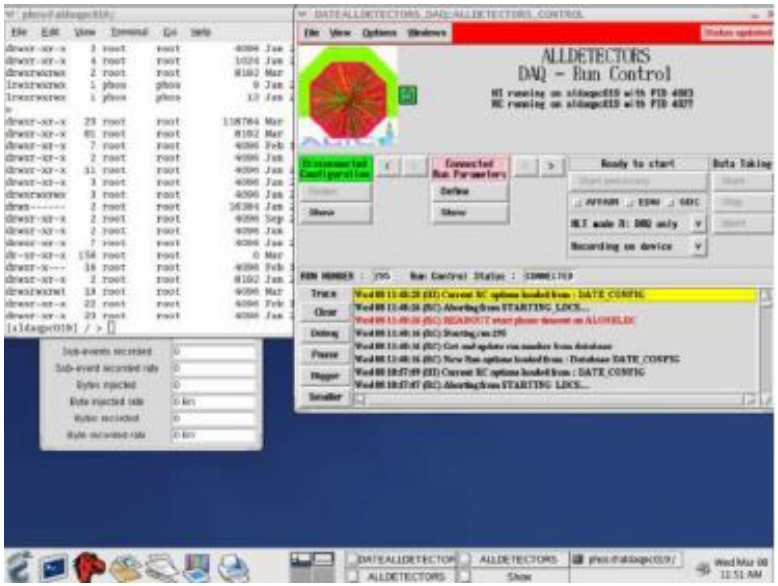
Quick overview of NEXT experiment

- **Search for the ββ0ν decay**
- **First measurement of ββ2ν in ^{136}Xe**
- **High pressure Xe gas TPC**
  - 100 Kg of enriched Xe gas
  - SOFT TPC concept
  - EL TPC
  - Good energy resolution ~ 1%
  - Full 3D tracking

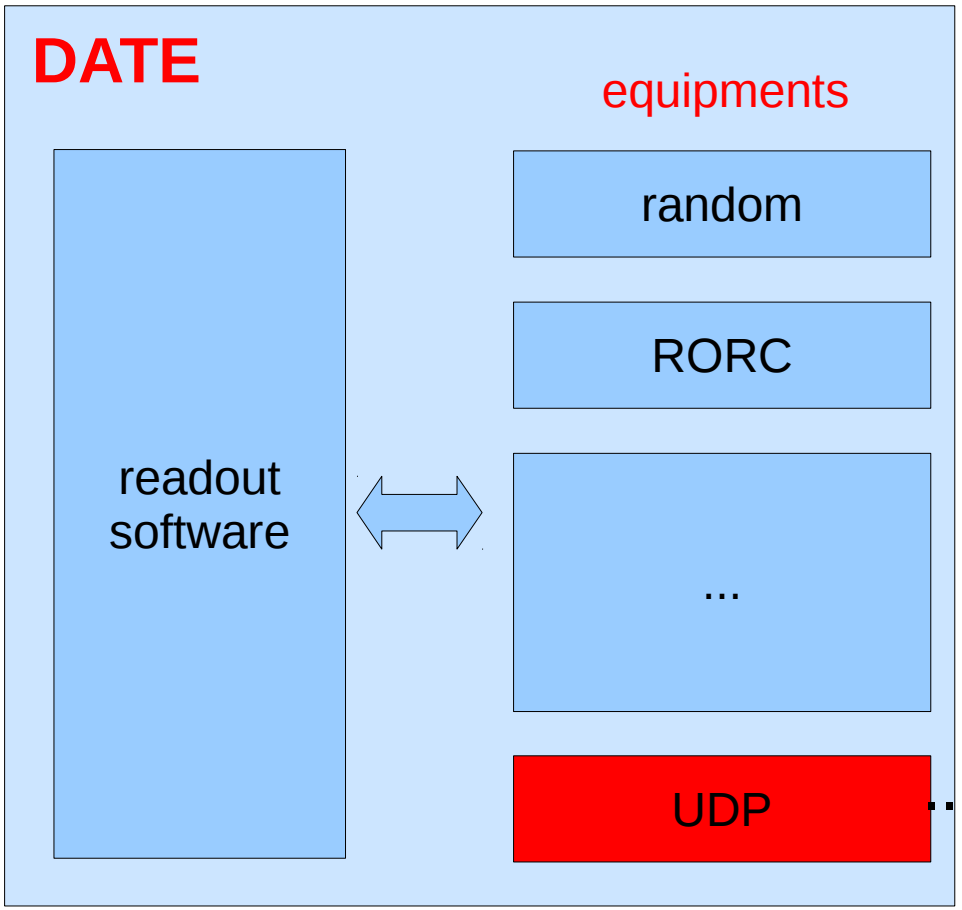


First scheme of NEXT online system

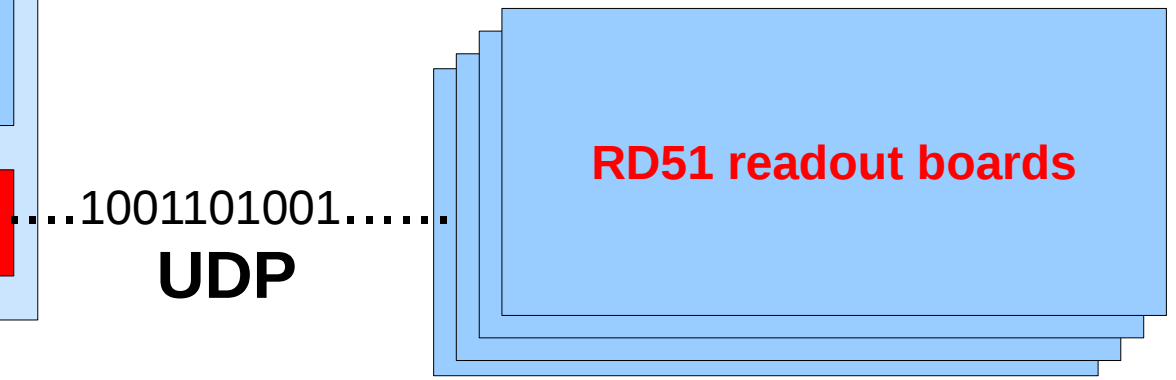
- **DAQ system using ALICE DATE software**
- **First release of the software ready to be installed in one machine in Spain**
  - Setup running at CERN using first prototype of RD51 readout board with a throughput around 120 MB/s (using 1Gbit link)
- **DAQ system of first prototype of NEXT experiment will include all DATE features in the same machine**



Between DATE and RD51 there are a lot of UDP packets

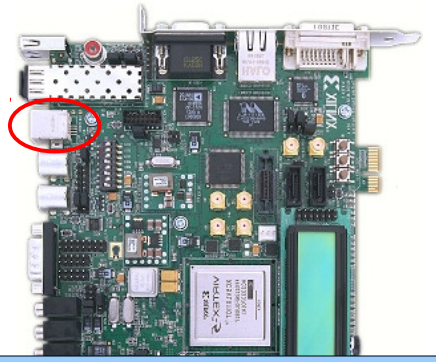


- **DATE** will receive data from the **RD51 readout boards** using an **Ethernet socket**.
- A new **equipment** for **DATE** has been developed to receive data through the Ethernet socket.
- The data will be prepared and sent as **UDP packets**.

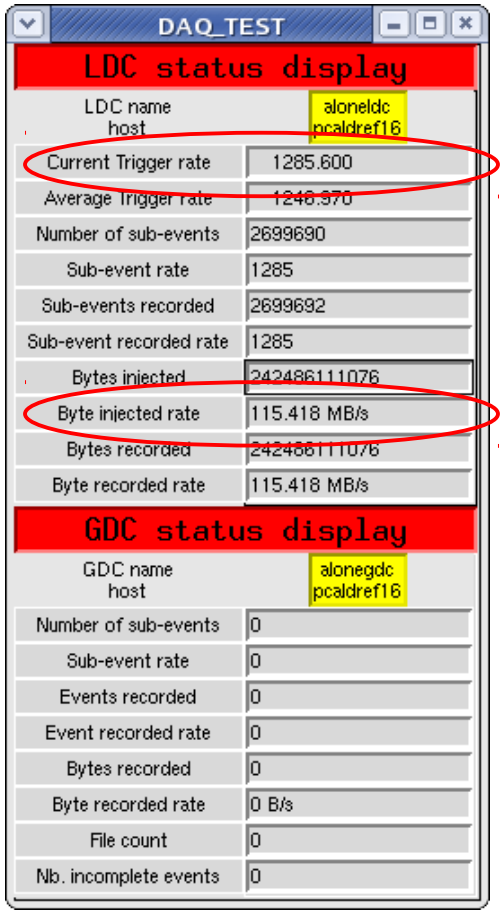


Test setup using a prototype readout board

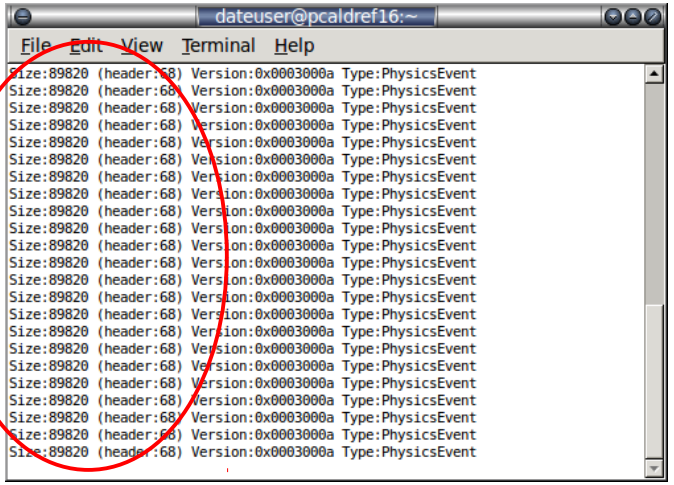
1 Gb



Firmware by
Alfonso Tarazona Martinez



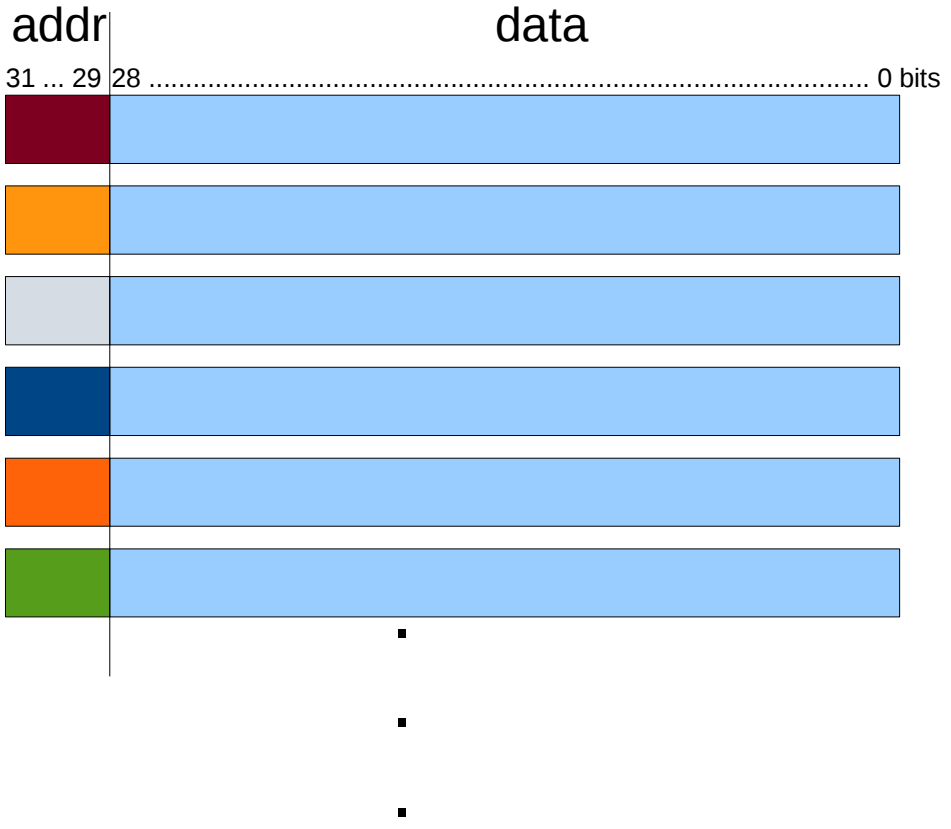
Size of the UDP packets: **9000 bytes**
MTU of the Ethernet card: **9000 bytes**
Event size: **10 packets per events → 89820 bytes**

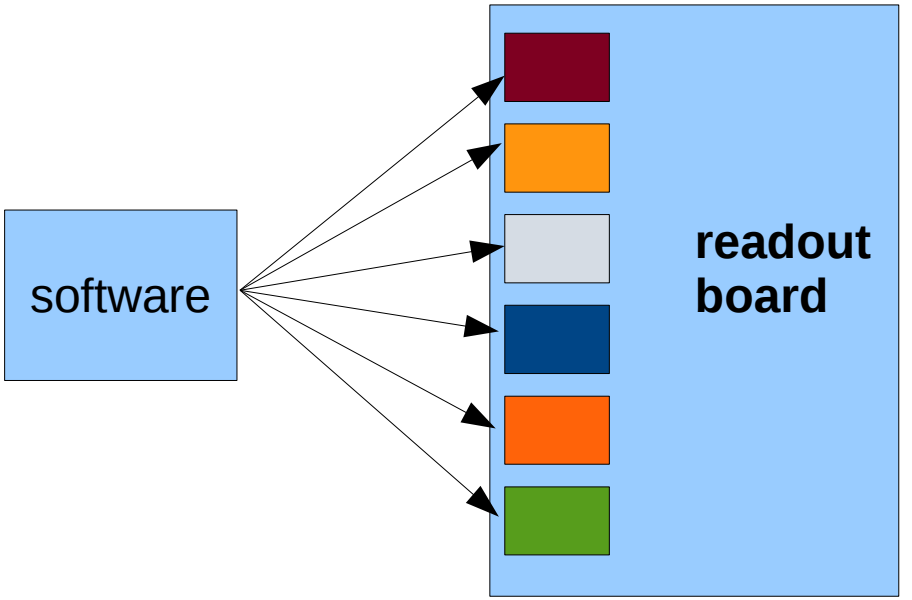


Readout board prototype based on a **Xilinx Virtex5** demo board

Using this configuration we have *tuned* the system to go as fast as possible reaching for the time being **120/124 MB/s** using event size of **89820 bytes (~75 M events – no errors)**

SLOW CONTROL (work in progress 2 IDEAS)





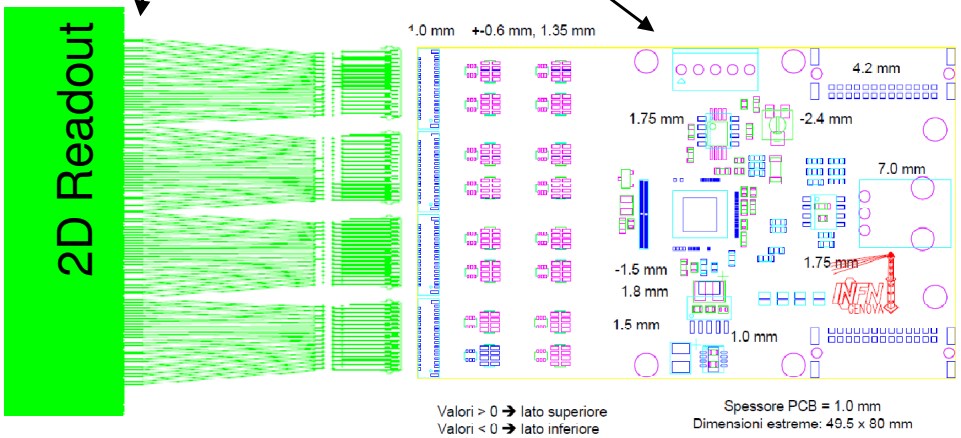
This solution is easy to implement via software but difficult to implement via VHDL. 29 bits of data is not a standard word and the board has to merge the information before analyzing the data.

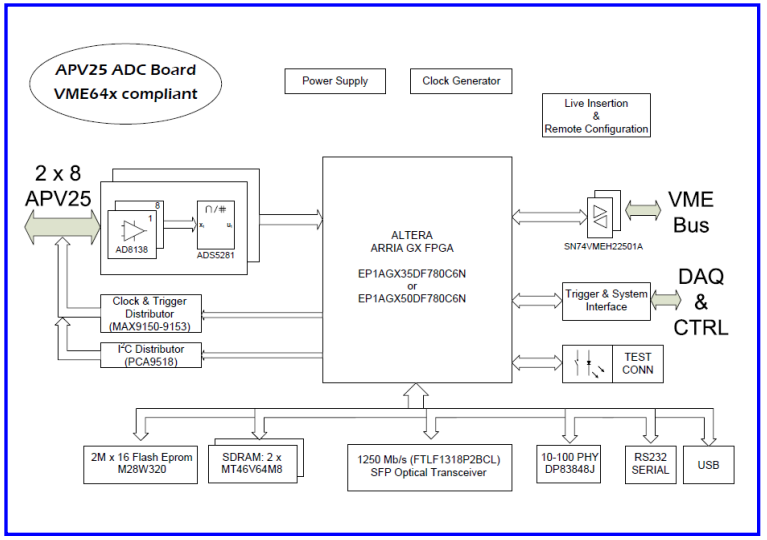
BETTER IDEA?

The readout board can define several ports (one for each service), the software will send 32 bits of data to the different ports. The board as soon as it receives a packet it stores the information in different FIFOs (connected to the ports) and it analyzes them when the communication ends.

Electronics Components

GEM ⇒ **FEC** ⇒ **ADC+VME Controller** ⇒ DAQ





General Criteria:

- Minimize development time
- Minimize material of FECs (which are partially along the particle path)
- Be compliant to JLab DAQ
- Maximize flexibilty (at least during prototyping)

Thanks to Michael Böhmer and Igor Konorov

Electronics Components

GEM ⇒ FEC ⇒ ADC+VME Controller ⇒ DAQ

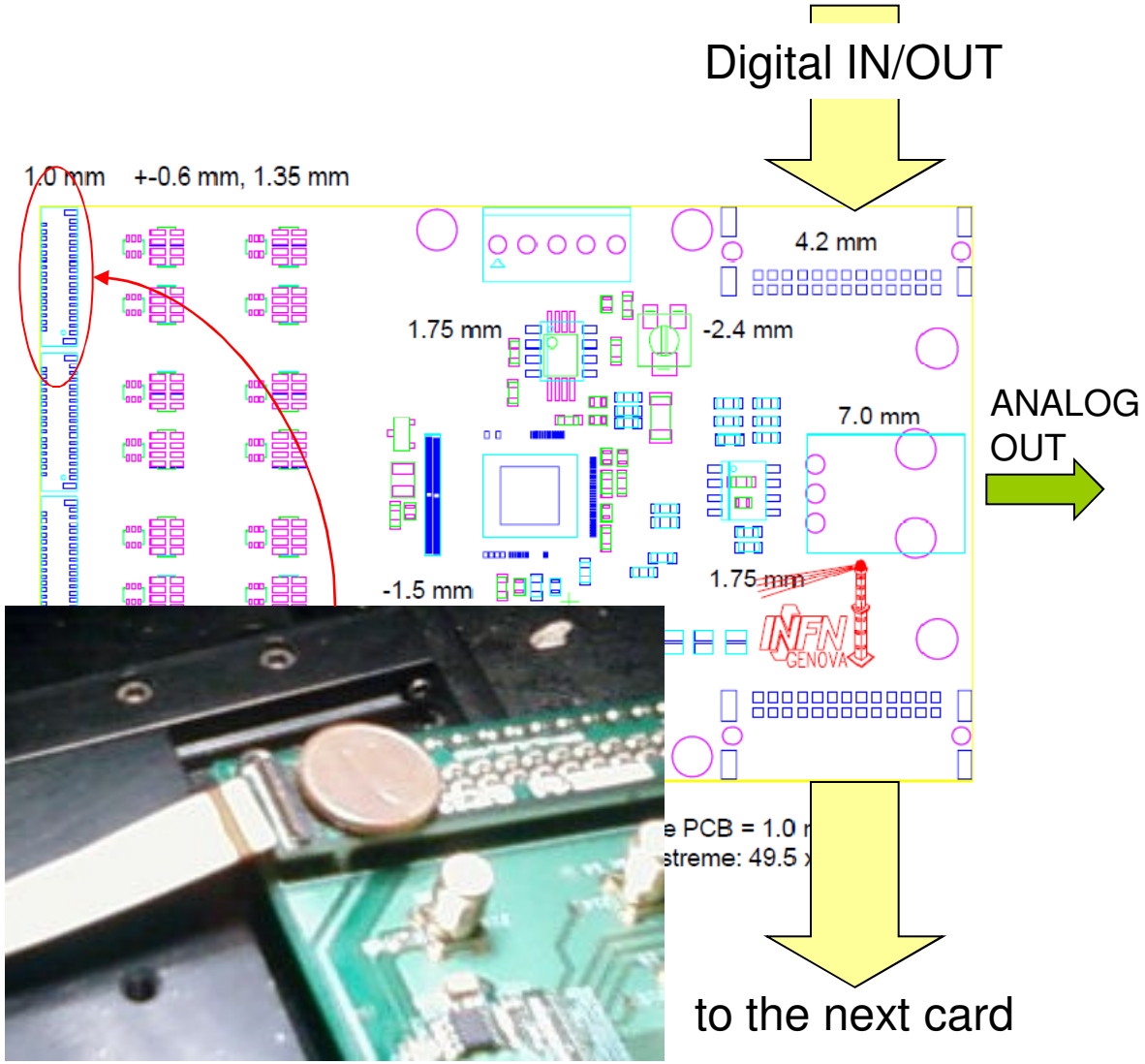
Front End card based on The APV25 chip (originally developed for SiD in CMS)

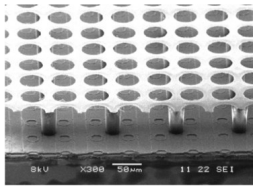
Bus like digital lines (CLOCK, trigger and I2C) & Low Voltages

Single differential line for the ANALOG out

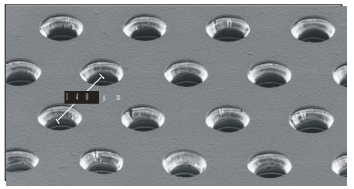
ZIF connectors on the GEM side (no soldering on readout foil)

First front-end prototypes available end of November/09





Task 1

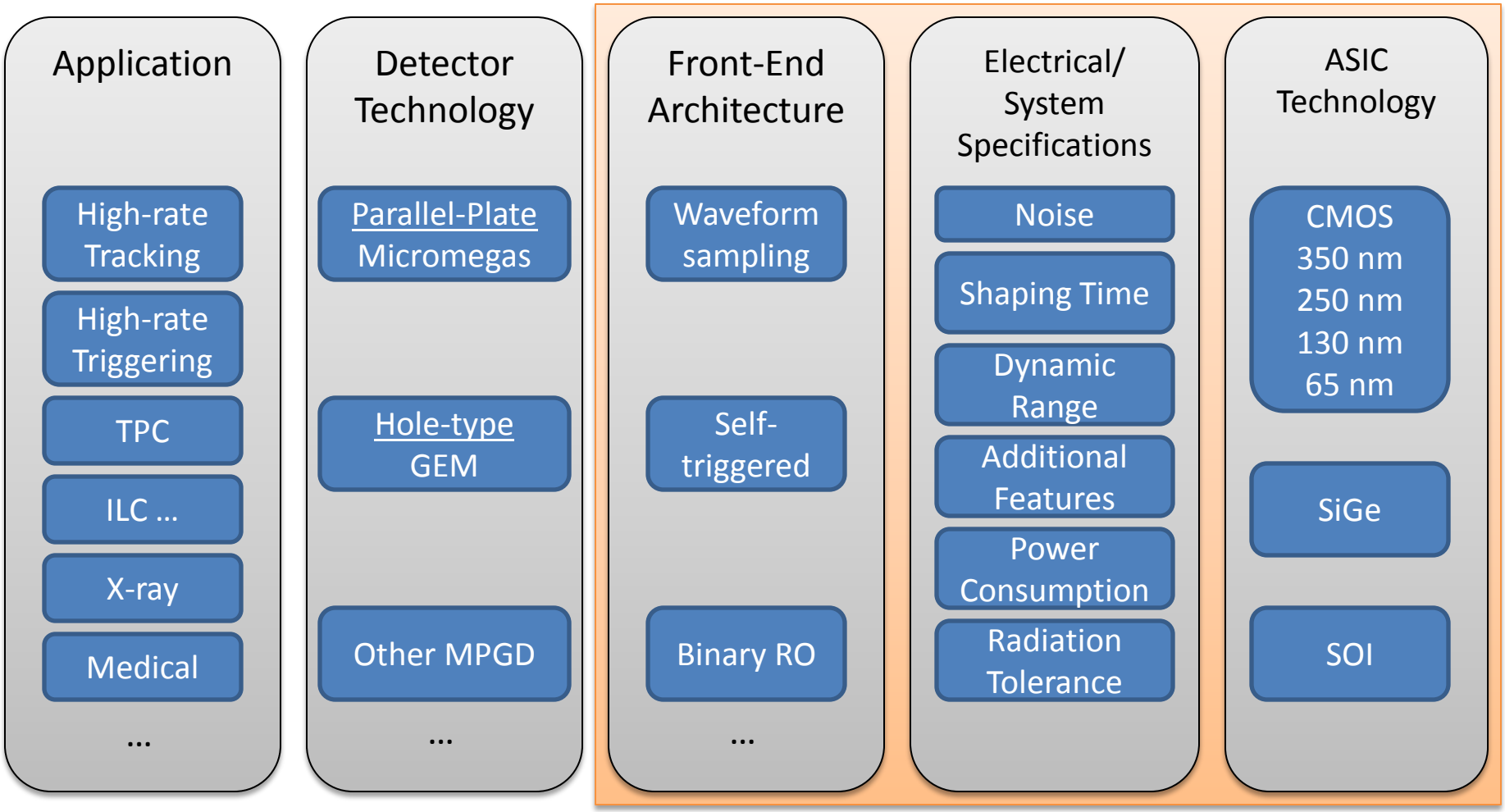


Definition of front end electronics requirements for MPGDs

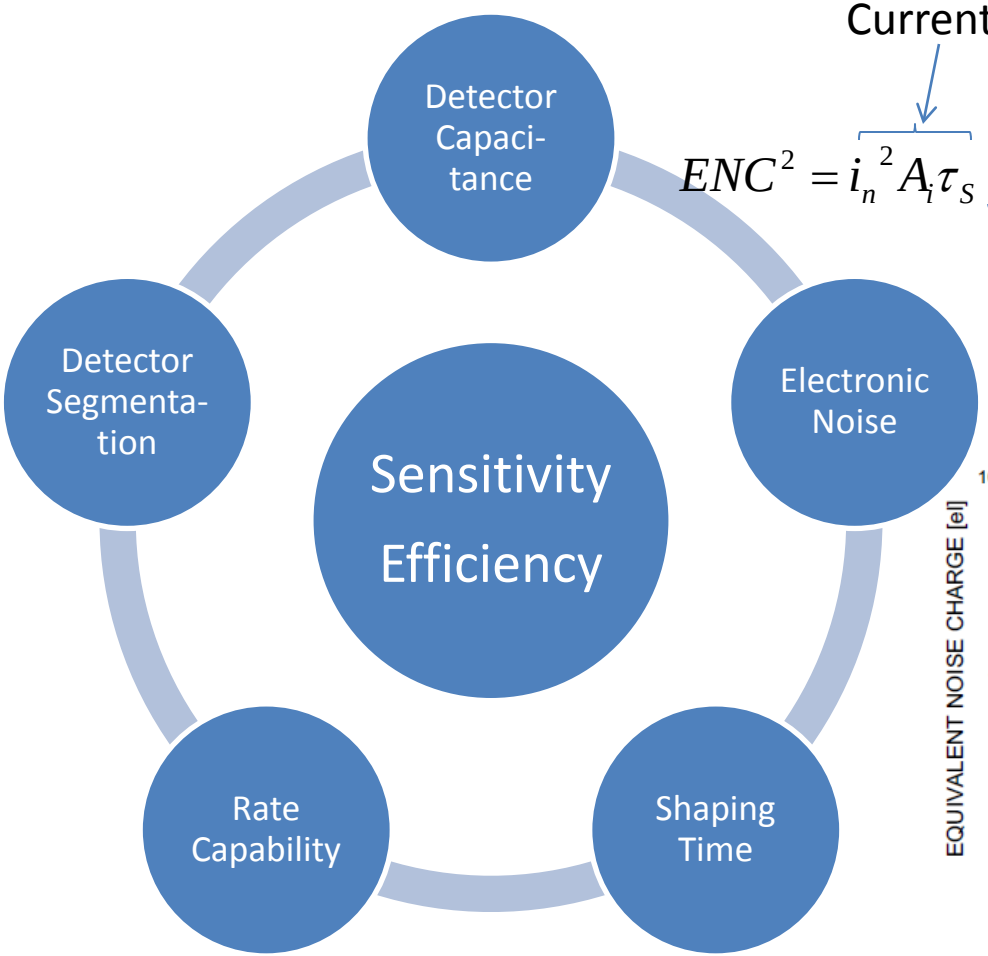
An extensive chip matrix was placed on the web.
1 contribution explained the details and important parameters were explained.

2 new chip designs were presented: MSGCROC and VFAT

“Ideal Chip” Specification



Sensitivity vs. Efficiency



Current Noise

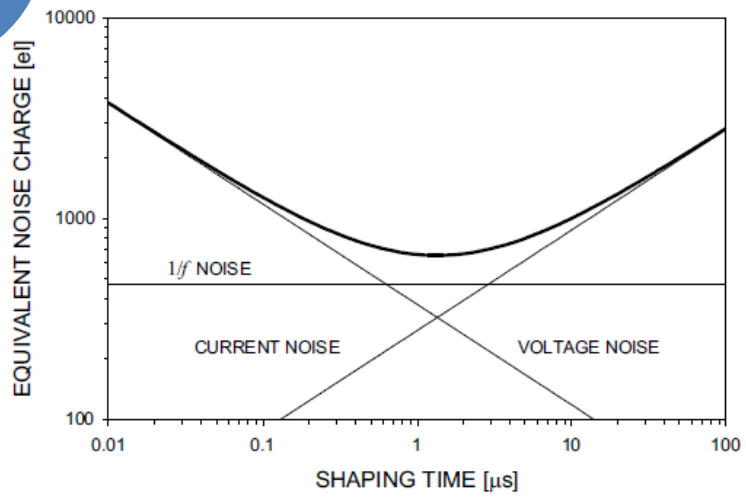
detector capacitance

$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

shaping time

White Noise

1/f Noise



From Chip Matrix to the Ideal Chip

Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
APV25	CMS	Si strip	128	50	270+38e/pF	20	both	A	40	2.7	PD, PR	0.25 CMOS	10
AFTER	T2K	TPC	72	100-2000 s-gauss	(350-1800) + (22-1.8)e/pF	19	both	A	1-50 (100)	7.5	VG,VS	0.35 CMOS	no
MSGCROC	DETNI	Gas strip	32	T: 25 E: 85	2000e @ 40pF	800	both	A,1	2ns TDC		VG, ZS	0.35 CMOS	no
Beetle	LHCb		128	25	500+50e/pF	17.5	both	A/1	40	5.2	F-OR	0.25 CMOS	40
VFAT	TOTEM		128	22	650+50e/pF	18.5 (cal)	both	1	40	4.47	F-OR	0.25 CMOS	50
NINO	ALICE	TPC	8	1	1900+165/pF	2000 th<100	both	1	async	30	BR	0.25 CMOS	no
CARIOCA	LHCb	MWPC	8	<15 @ 220pF	2000+40e/pF	250	both	1	async	46	BR	0.25 CMOS	20
PASA+ ALTRO	ALICE TPC	TPC	16	190_{fwhm} s-gauss	570e @20 pF	160	both	10	20	< 40	BC, TC, ZS	0.35,0.25 CMOS	
SVX4	CDF, D0	Si strip	128	100-360	410+45e/pF	60fC	neg	8	106 (212)	2	ZS	0.25 CMOS	20
SPIROC	ILC, T2K	SiPM	36	A:25-175 T: 10	A: 1/11pe; T:1/24pe	2000 pe	neg	8-12	100ps TDC	0.025 *pulse*	dual-gain	0.35 SiGe	no

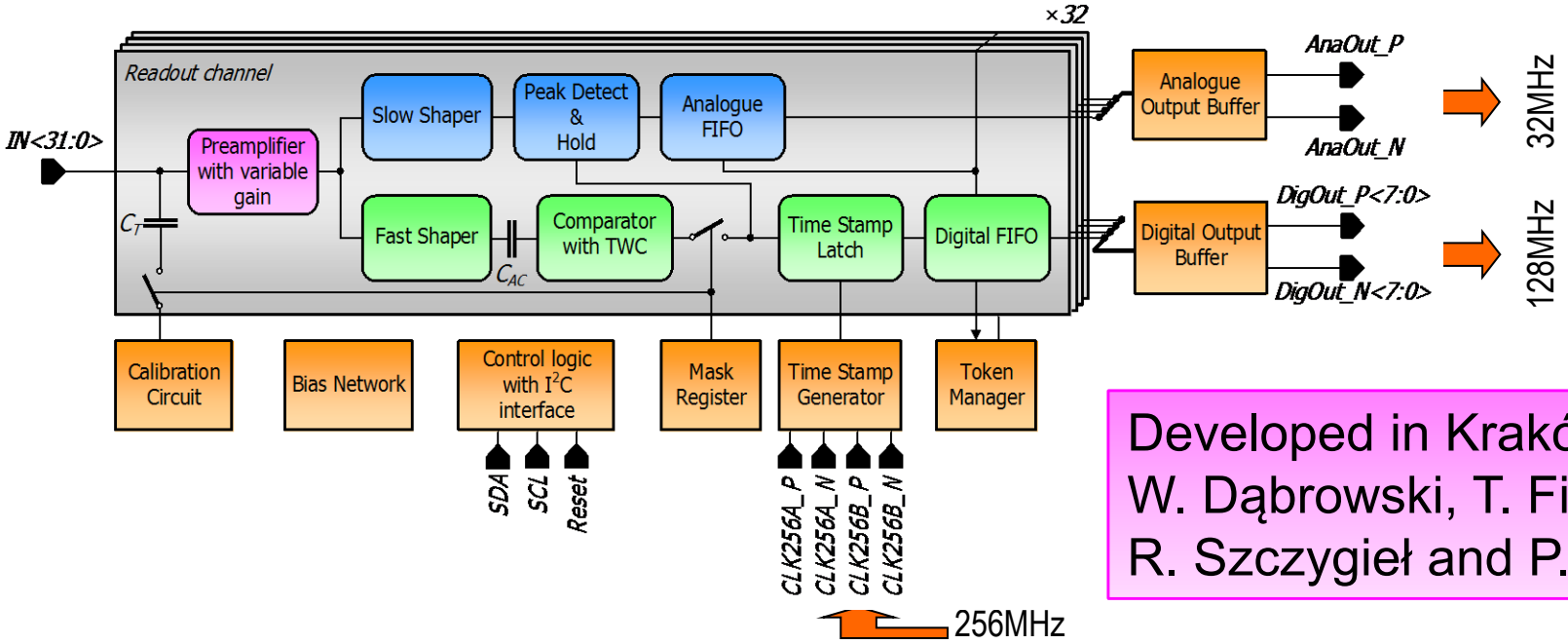
Legend: PD = peak detection, PR = pile-up rejection, VG = variable gain, VS = variable shaping, F-OR = fast-OR, BR = baseline restorer, BC = baseline correction, TC = tail correction, DC = data compression, ZS = zero suppression

- shaping time: 5ns .. 1us
- dynamic range: <100fC
- power: < 10 mW/ch (?)
- ADC accuracy: 10 bits (?)
- TDC accuracy: 1ns

…

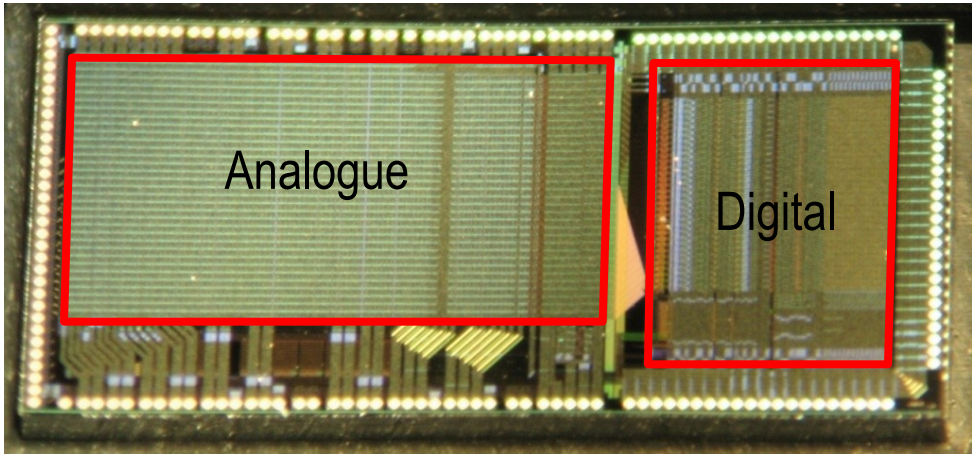
*We need an **APV25** chip with variable gain and shaping time like the **AFTER** chip, dynamic range like **MSGCROC,** integrated fast-OR like **Beetle**, integrated ADC like **SVX4,** digital signal processor like **ALTRO***

MSGCROC architecture



Developed in Kraków by:
W. Dąbrowski, T. Fiutowski,
R. Szczygieł and P. Wiącek

3.2x6.7 mm^2



0.35 μm CMOS process from Austria Microsystems

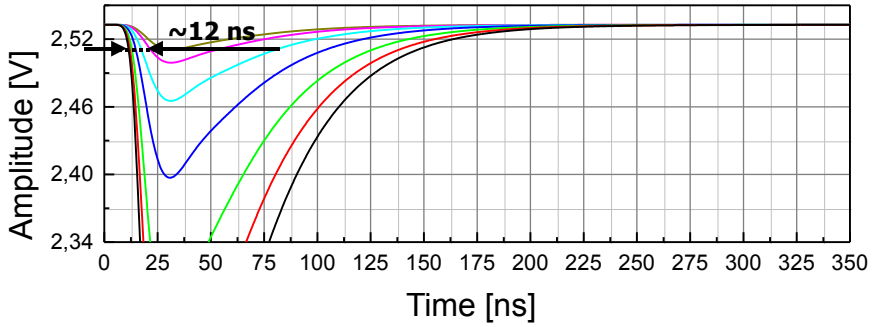
Input device: PMOS 2368μm/0.4 μm

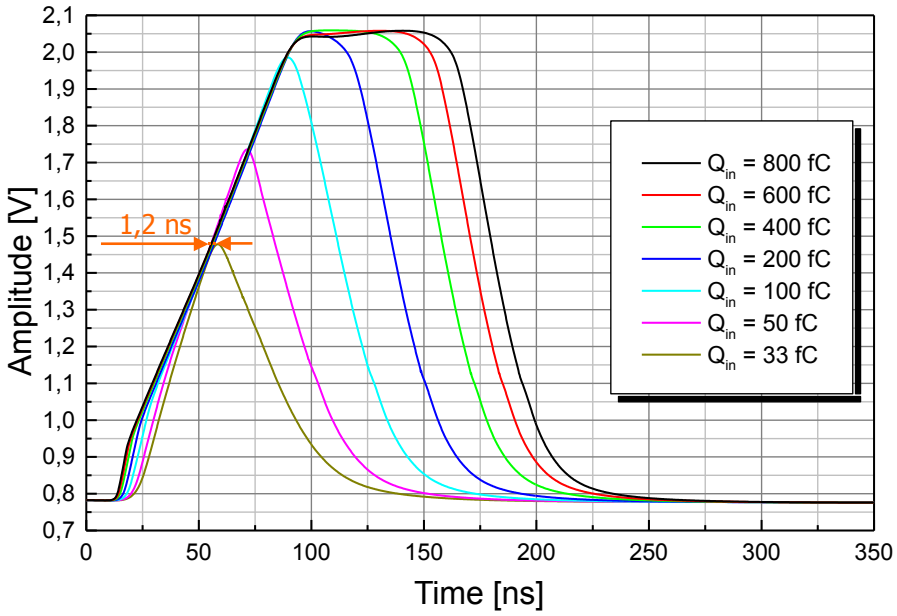
Bias current of the input transistor: 2.36mA (nominal)

Power consumption ~25 mW/channel (@ 3.3 V)

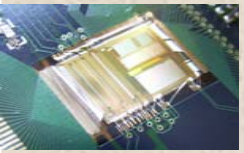
Separated analogue and digital power supply

Time Walk Compensation

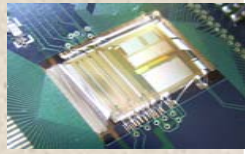




- Crossing of the same threshold level is relatively different in time for small and high signals
  - Gain x1
  - About 12 ns window
  - Compensated by TWC to 1.2 ns



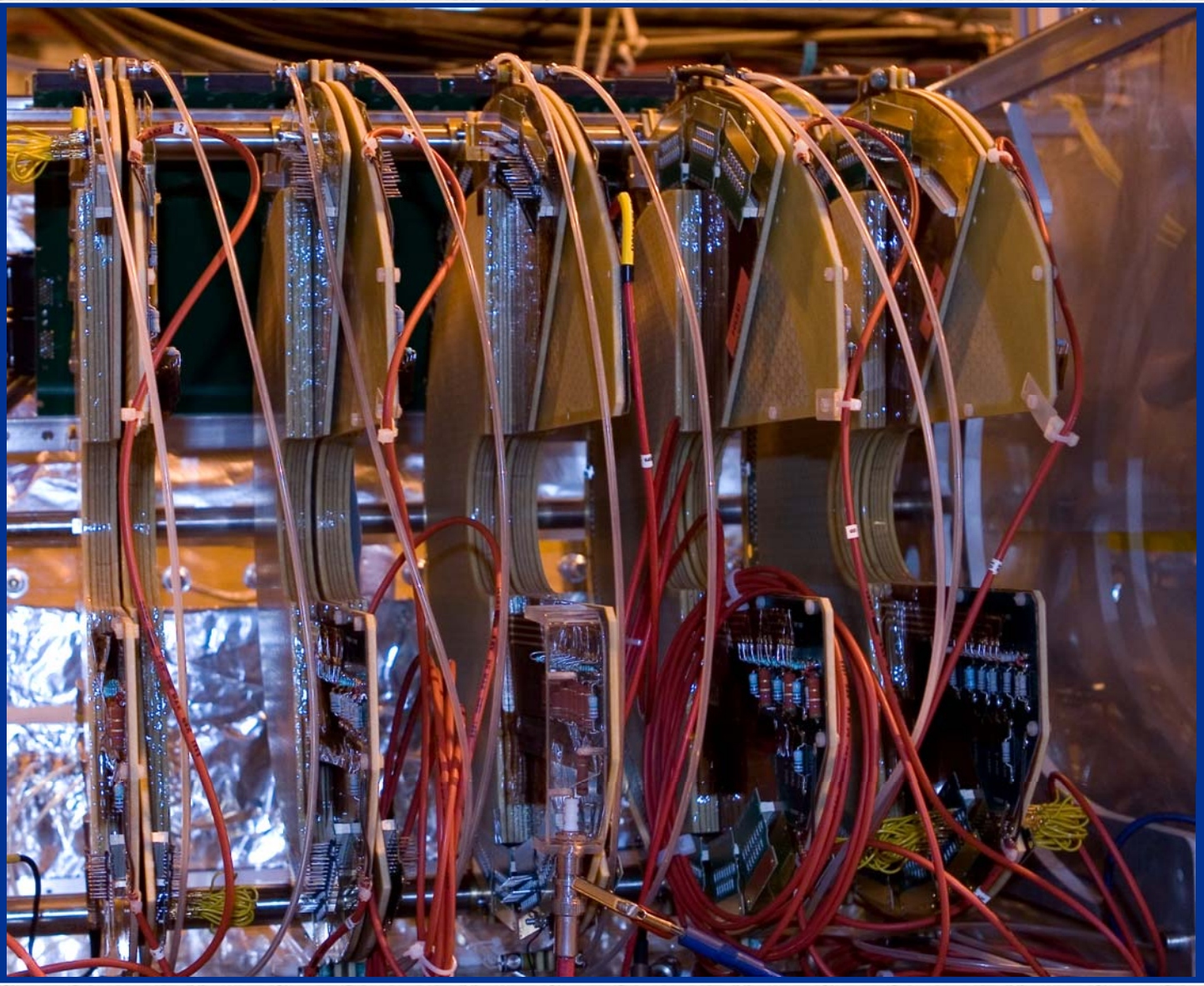
VFAT2 Key Features

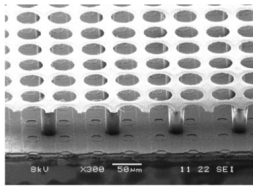


Trigger and Tracking Functions

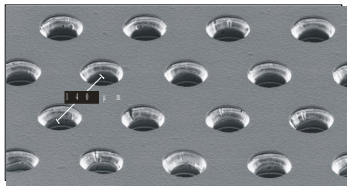
- **128 channel** low noise front-end chip for binary readout of capacitive sensors.
- **40MHz signal sampling** (dead time free)
- **Digital memory** Programmable LV1A latency up to 256 clock periods. Simultaneously storage of up to 128 triggered events.
- **Trigger building** Programmable "fast-OR" trigger building outputs
- **Internal calibration** via internal test pulses with programmable amplitude
- **Fully programmable** through an I^2C interface.
- **Data packet output** includes headers, counters, flags and CRC check
- **Radiation tolerant** design – suitable for use in demanding radiation environments both with respect to ionising radiation and Single Event Upset.

The T2 GEM detector





Task 3

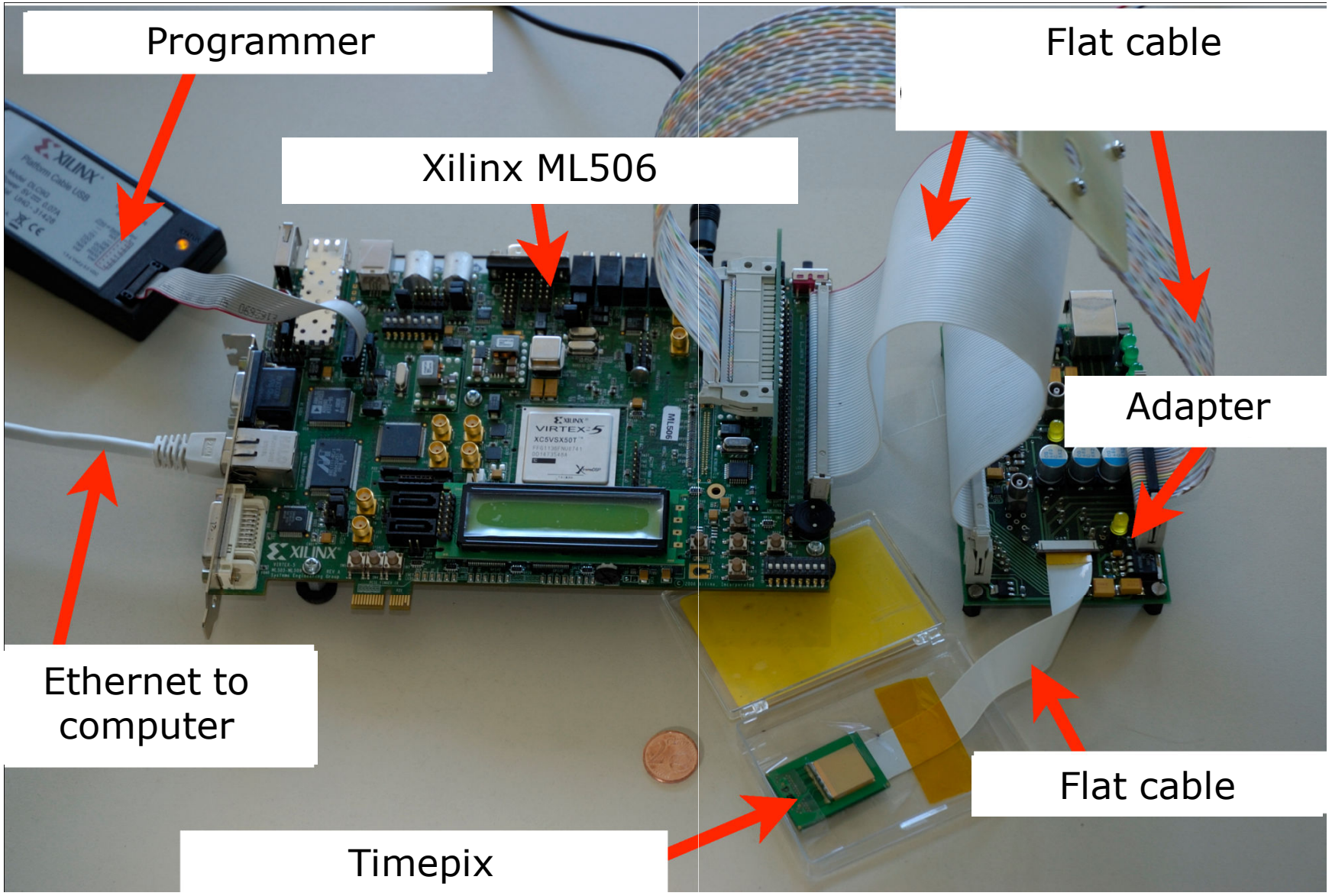


Development of large area detectors with pixel readout

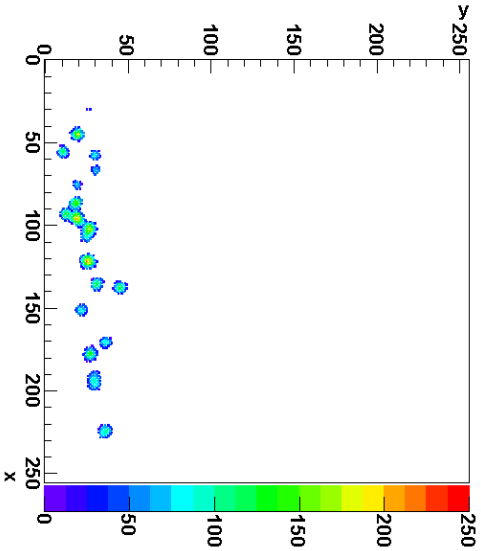
A new readout system for the Timepix was presented.

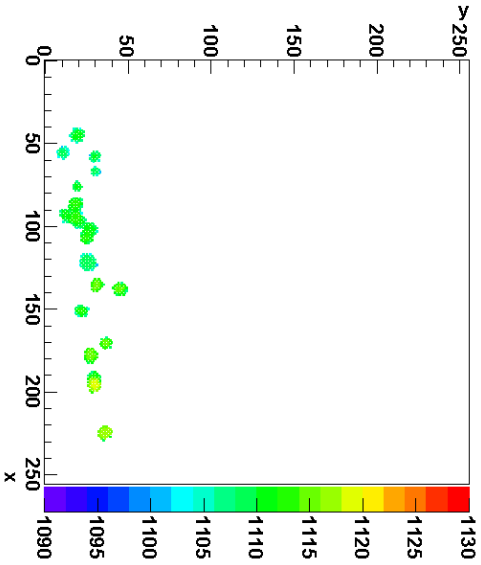
The development can be merged into the SRS giving the possibility to operate a large number of Timepix chip.

Lab test setup



Results: muons in the TPC



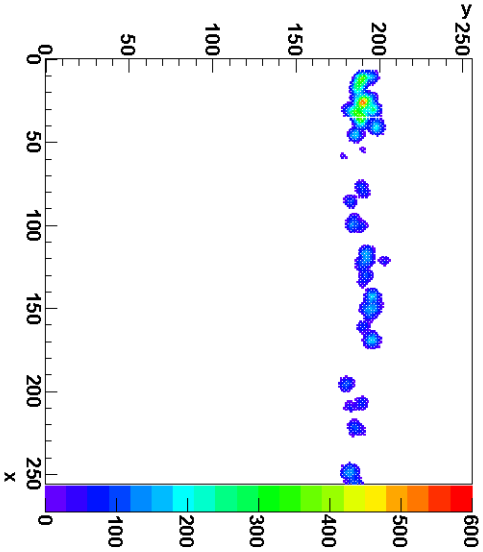


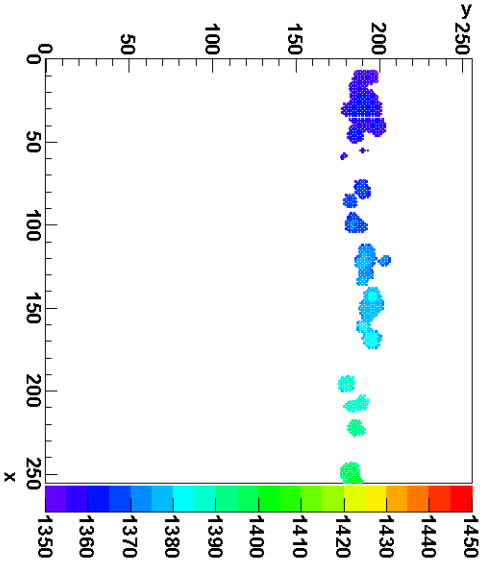
← Energy deposit →
(TOT mode)

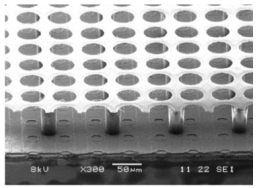
Muon tracks crossing the TPC
← at 8.9cm and 2.8cm →
distance to readout plane.

Both deposited charge and drift time measured concurrently by operating every other pixel in TOT or common stop mode

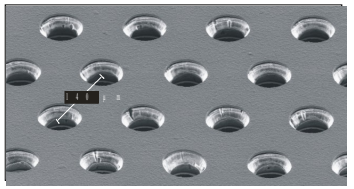
← X-Y-Z*drift* view →
(common stop mode)







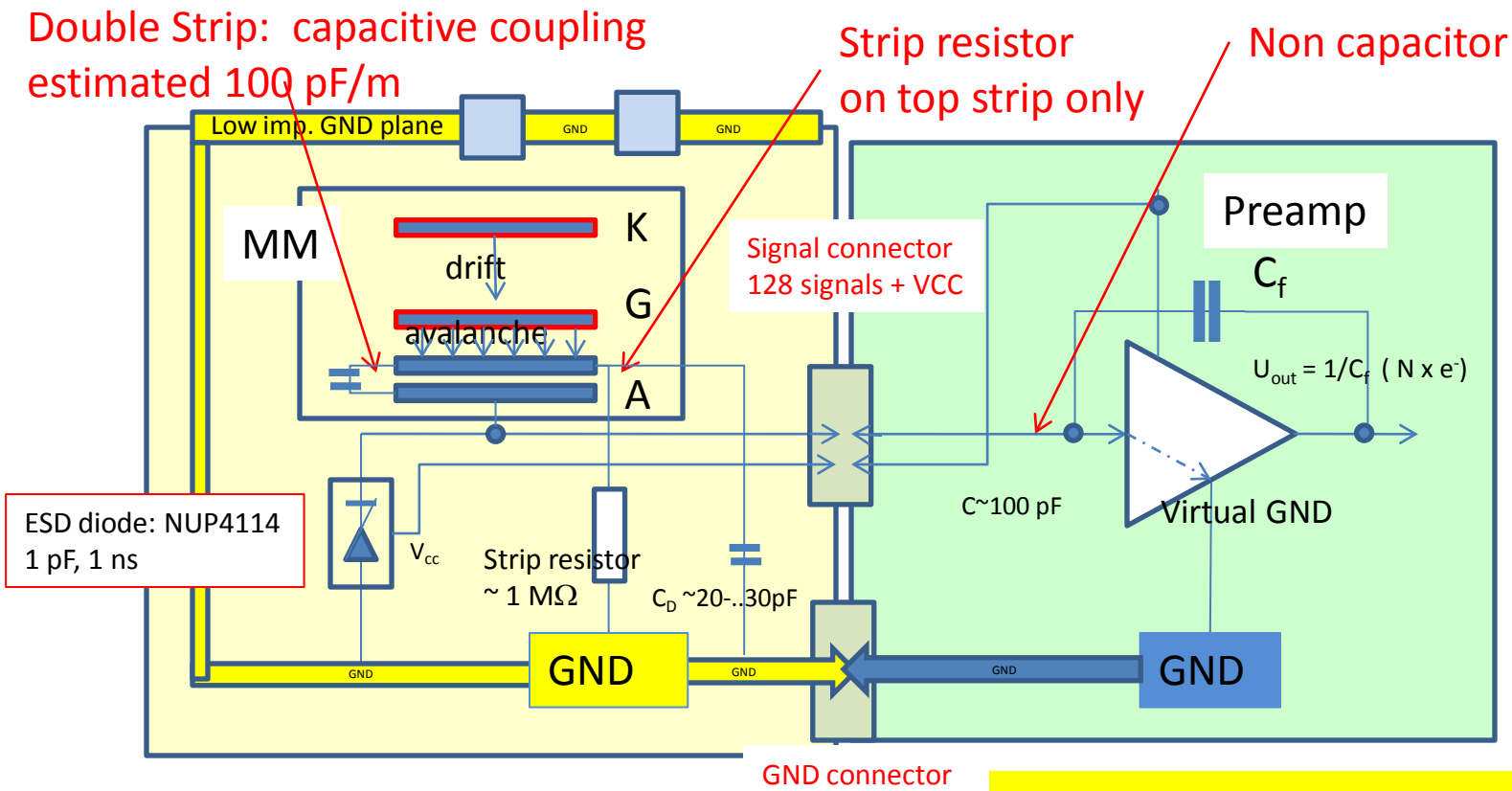
Task 5



Discharge protection strategies

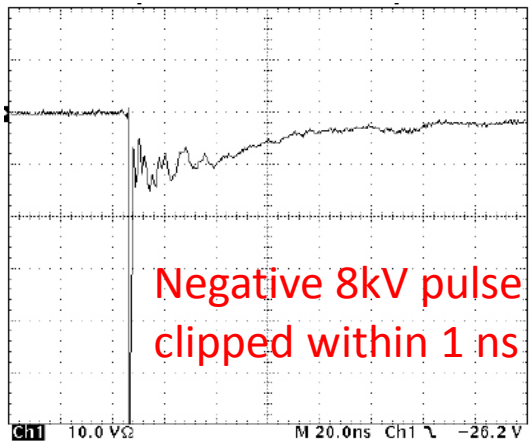
A new idea for discharge protection was presented
ESD diodes

MM chamber: Integrate coupling capacitor in double strip design



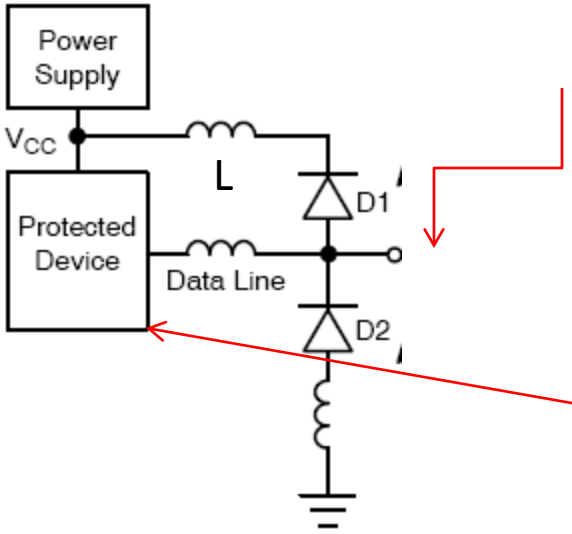
High sparc immunity expected:
Sparc-charge contained on chamber
Capacitively induced charge clipped by ESD diode on chamber

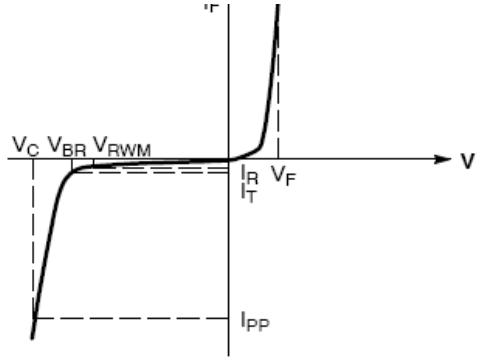
ESD clipping performance



IEC 61000–4–2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



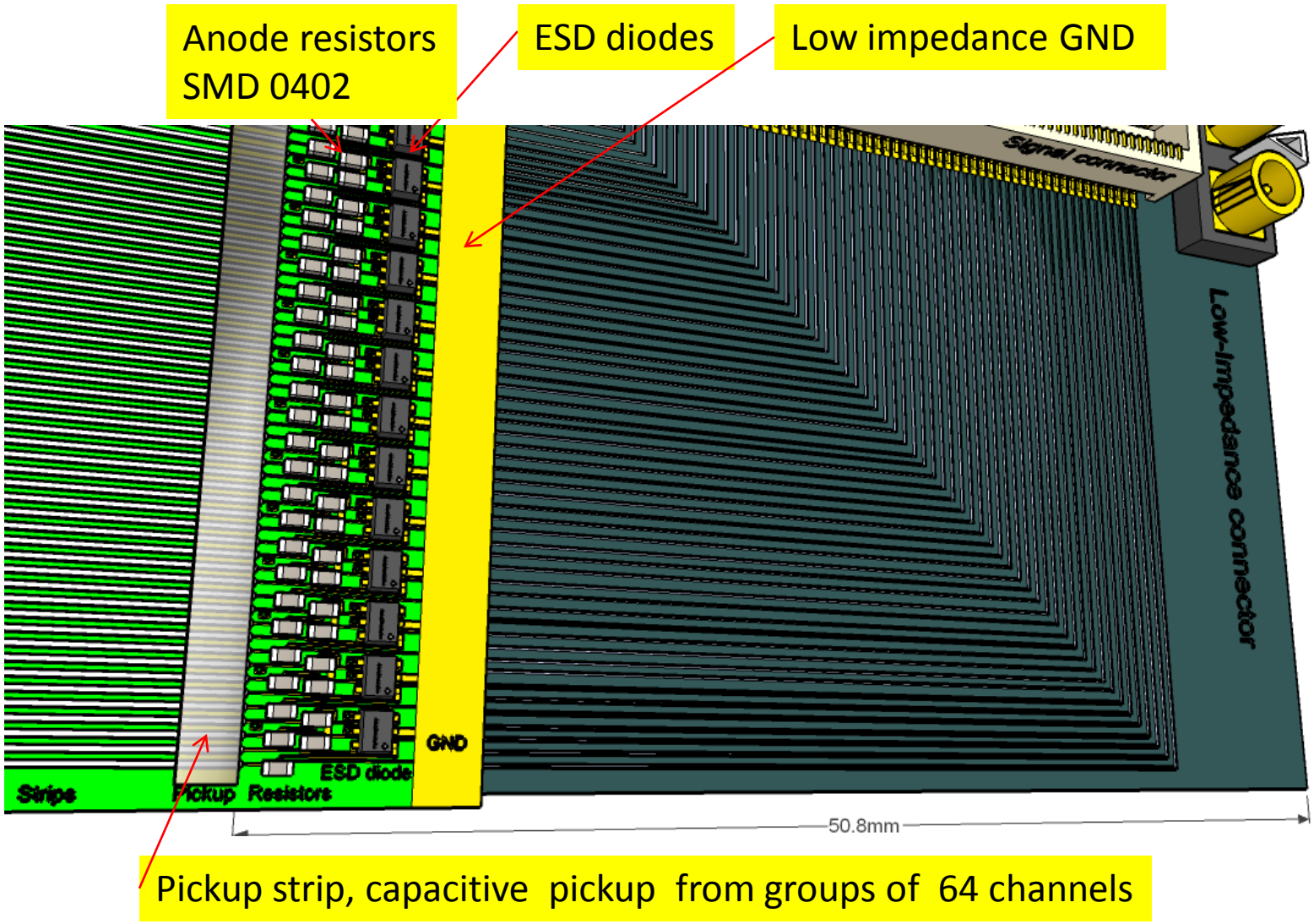


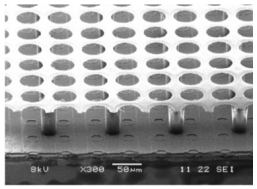
Negative clipped: $V_n = -V_f - L \times dI_{esd}/dt$

Positive clipped: $V_p = V_{cc} + Vf + L \times dI_{esd}/dt$

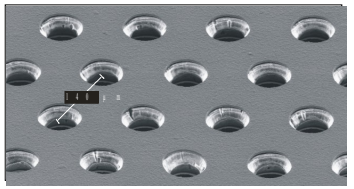
Minimize the inductive part L !

ESD Implementation on chamber





Conclusion



- Very active core group driving the projects (especially SRS) ahead:

- Scalable Readout System well on track:
  - first HW components will be tested in the next few weeks
  - connections are being tested
  - first two chips (APV25/Beetle and Timepix) are being worked on

- Starting to look at other tasks
  - collecting information on 'ideal chip' and spark protection

ANY PARTICIPATION OR NEW IDEAS/INPUT IS VERY WELCOME