PRESENT AND FUTURE INTER PIXEL COMMUNICATION ARCHITECTURES IN TIMEPIX/MEDIPIX DERIVED READ OUT CHIPS

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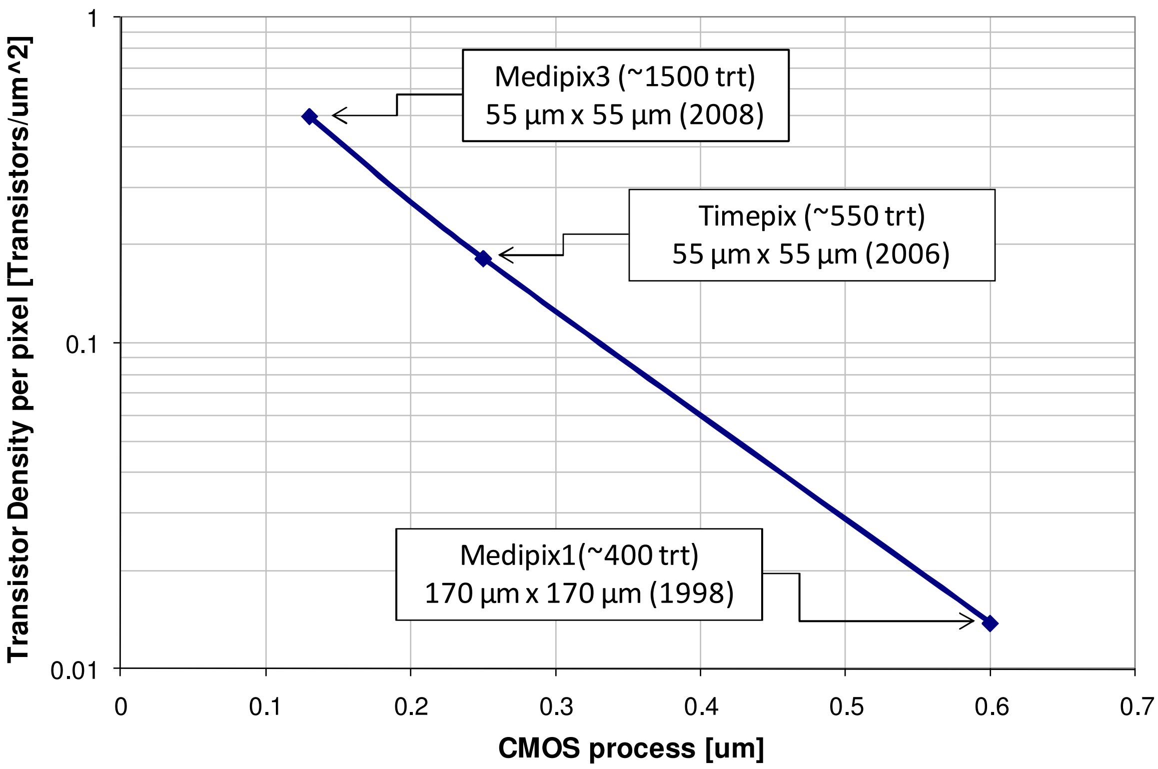
*on behalf of the Medipx3, Timepix2 and VELOpix design teams

Outline

- Technology motivation
- Medipix3
- Timepix2
- LHCb VELO upgrade → VELOpix (~2013)
- Conclusions

Technology motivation

- The evolution in CMOS technology is motivated by decreasing price-per-performance for digital circuitry → increased transistor density



- While this evolution in CMOS technology is by definition very beneficial for digital this is not so for analog circuits (low VDD, transistor leakage,…)

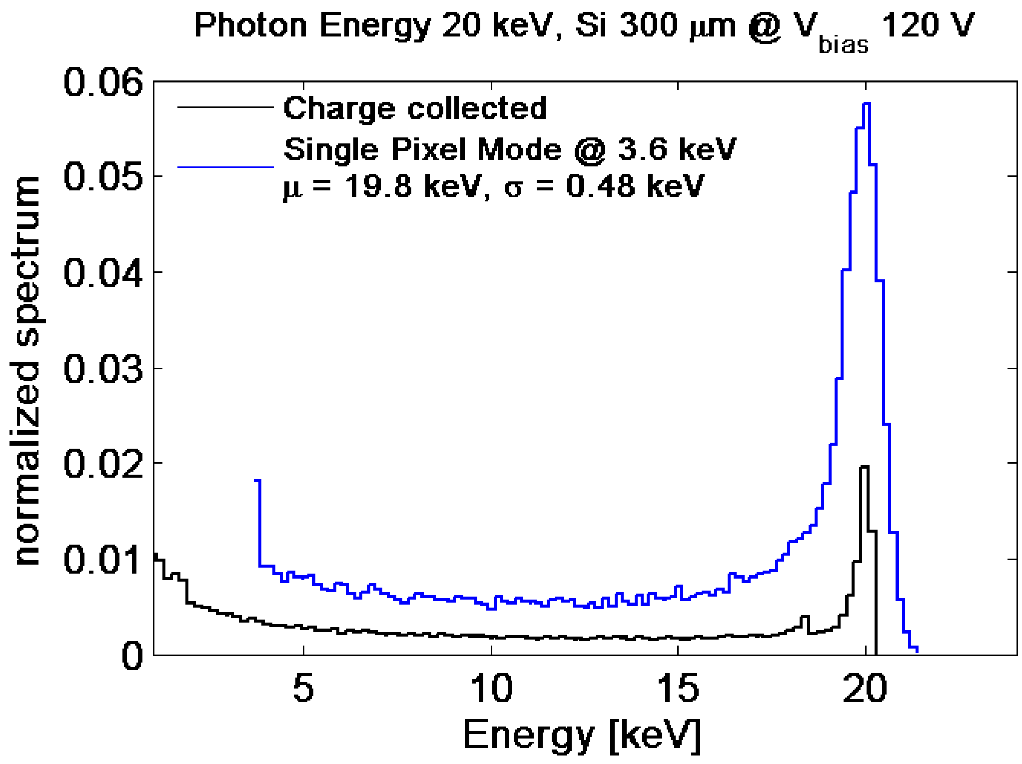
The Medipix3 Collaboration

Motivation
Medipix3
Timepix2
VELOpix
Conclusions

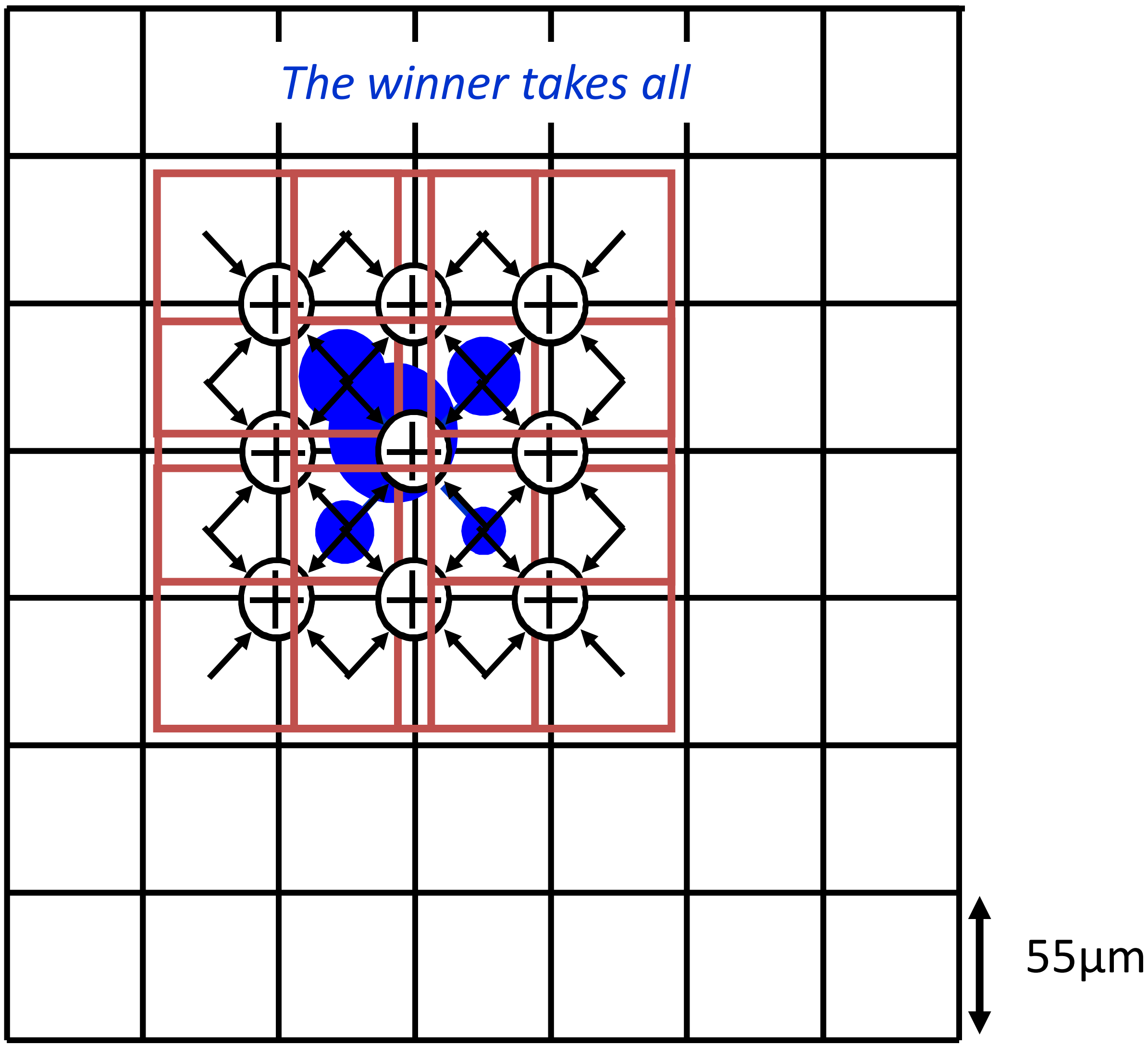
- University of Canterbury, Christchurch, New Zealand
- CEA, Paris, France
- CERN, Geneva, Switzerland,
- DESY-Hamburg, Germany
- Albert-Ludwigs-Universität Freiburg, Germany,
- University of Glasgow, Scotland, UK
- Leiden Univ., The Netherlands
- NIKHEF, Amsterdam, The Netherlands
- Mid Sweden University, Sundsvall, Sweden
- Czech Technical University, Prague, Czech Republic
- ESRF, Grenoble, France
- Universität Erlangen-Nurnberg, Erlangen, Germany
- University of California, Berkeley, USA
- VTT, Information Technology, Espoo, Finland
- ISS, Forschungszentrum Karlsruhe, Germany
- Diamond Light Source, Oxfordshire, England, UK
- Universidad de los Andes, Bogota, Colombia
- AMOLF, Amsterdam, The Netherlands
- ITER International Organization, Cadarache Centre, France

Medipix2 simulation

- The Medipix2/Timepix devices (square pixels of 55 µm) show an energy spectrum distortion due to charge sharing between adjacent channels

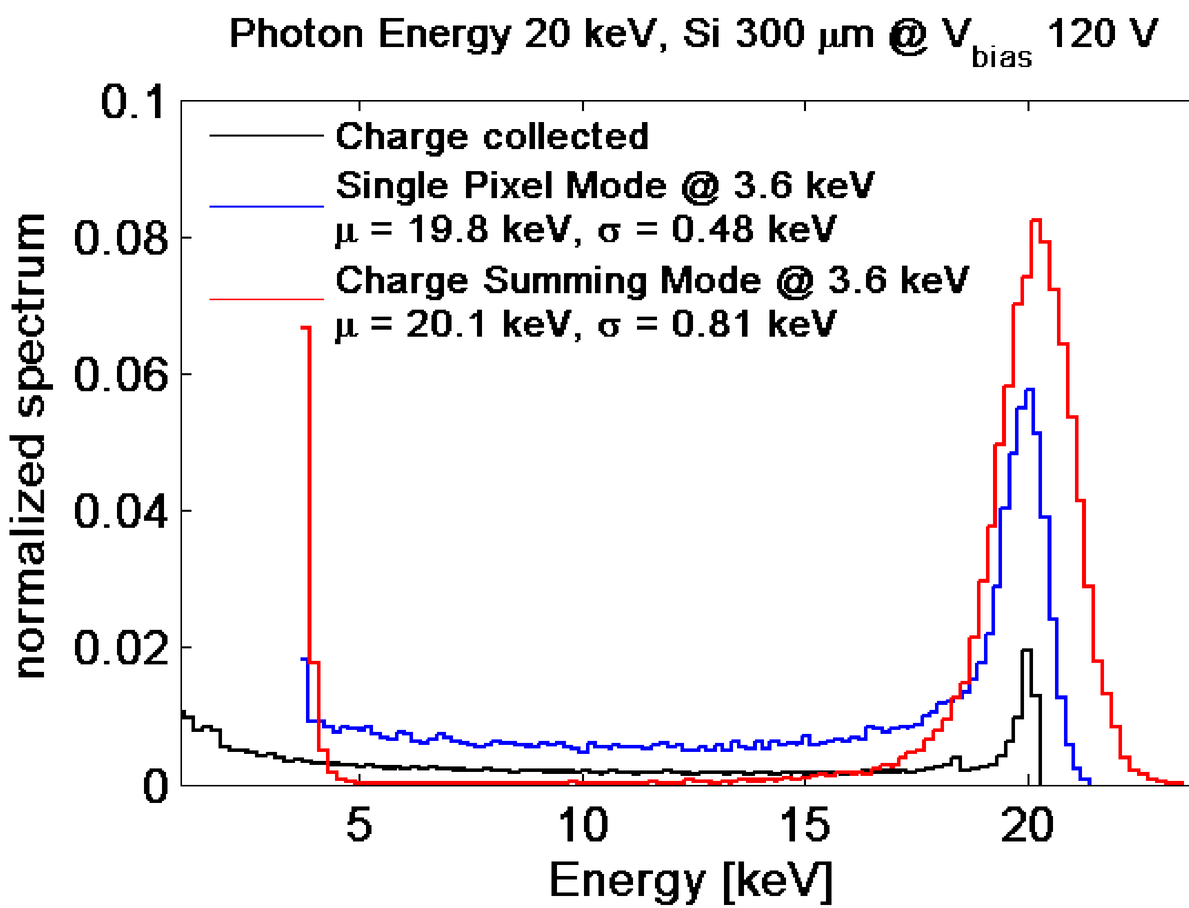


Charge summing and allocation concept



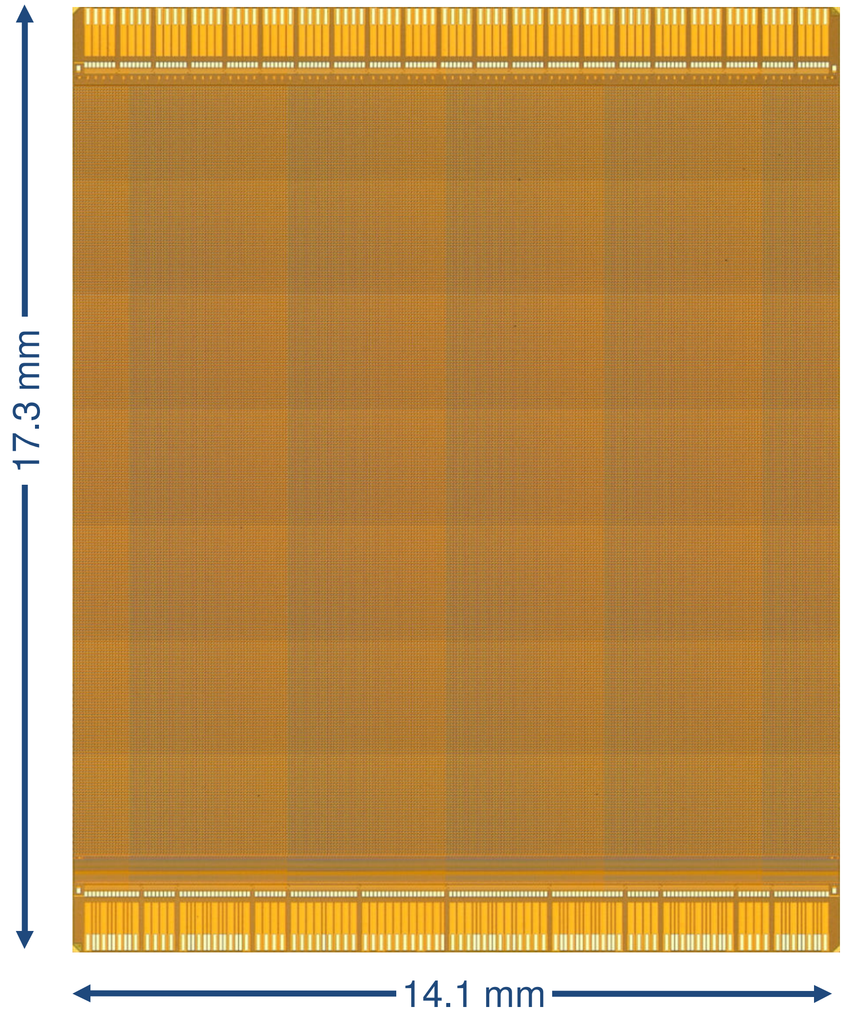
Medipix3 simulation

- Pixel spectrum is reconstructed → Colour imaging



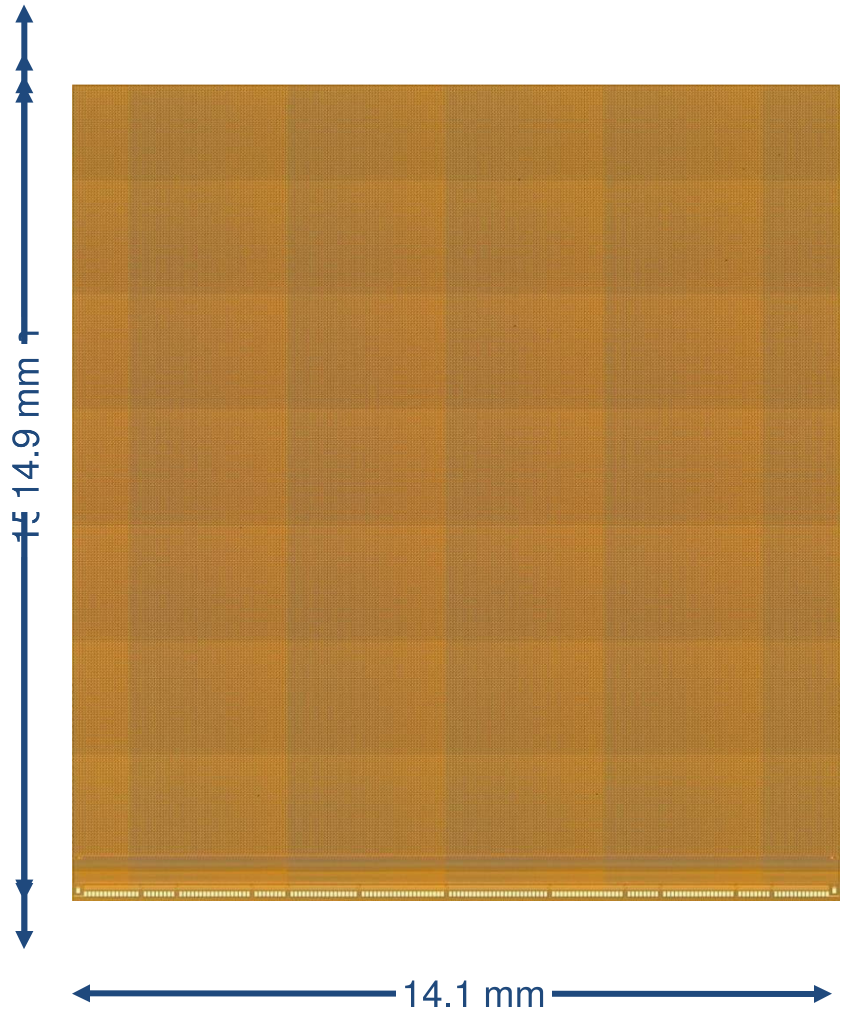
The Medipix3 (2009)

- Pixel matrix of 256 x 256 pixels (55 µm x 55 µm)
- Bottom periphery contains:
  - LVDS drivers and receivers (500 Mbps)
  - Band-Gap and 25 DACs (10 9-bit and 15 8-bit)
  - 32 e-fuse bits
  - EoC and 2 Test pulse generators per pixel column
  - Temperature sensor
  - Full IO logic and command decoder
  - TSV landing pads
- Top periphery contains:
  - Power/Ground pads
  - TSV landing pads
  - Pads extenders
- > 115 Million transistors
- Typical power consumption:
  - 600 mW in Single pixel mode
  - 900 mW in Charge summing mode
- 130nm CMOS IBM-DM process



Multiple dicing options

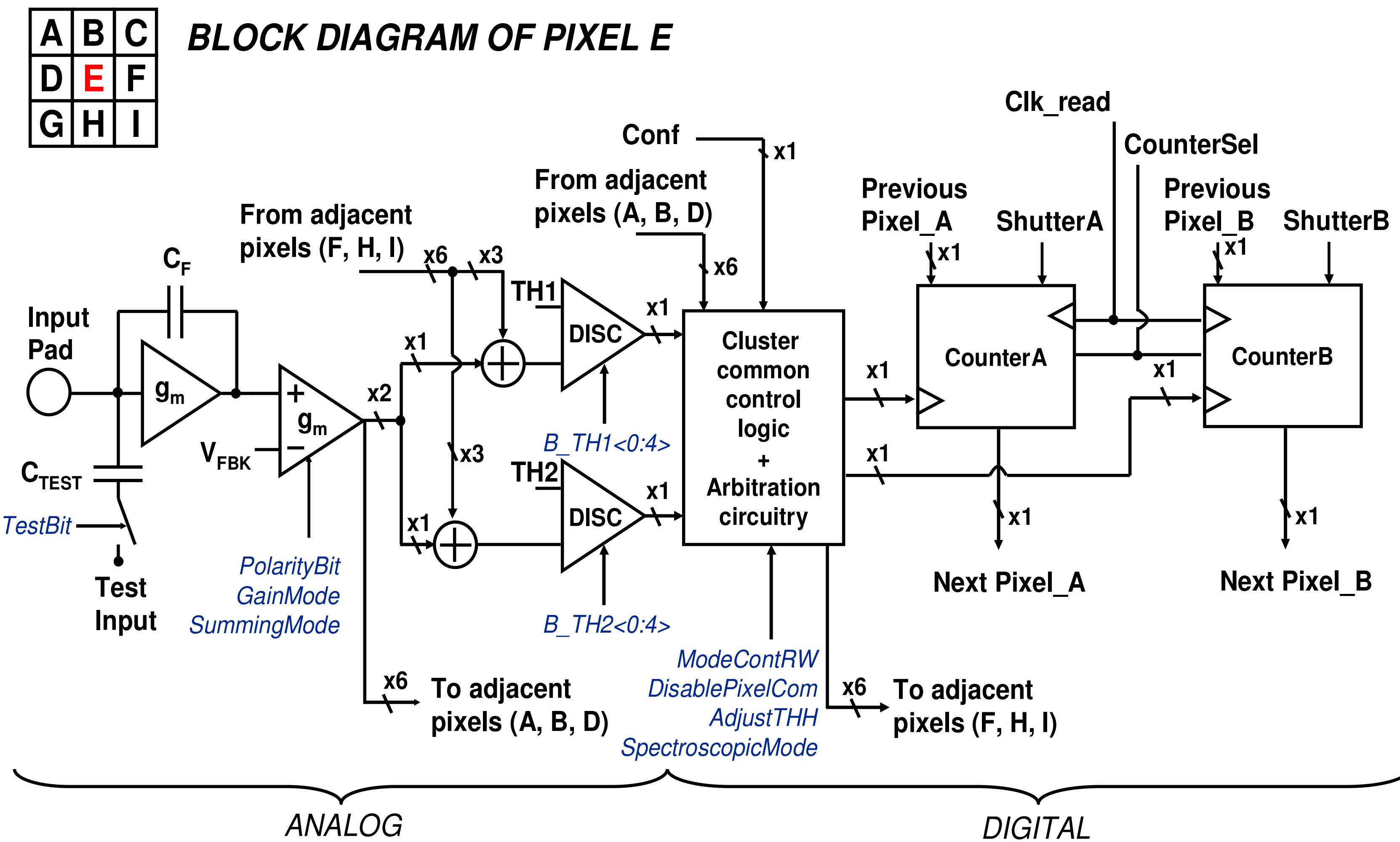
	X [µm]	Y [µm]	Active Area
Medipix2 and Timepix	14111	16120	87.1%
Medipix3 top and bottom WB	14100	17300	81.2%
Medipix3 bottom WB	14100	15900	88.4%
Medipix3 top and bottom TVS	14100	15300	91.9%
Medipix3 bottom TVS	14100	14900	94.3%



Medipix3 pixel Modes

Pixel Operation Modes	Pixel size	# Thresholds
Single Pixel	Fine Pitch Mode → 55 µm x 55 µm	2
Charge Summing		
Colour Mode	Spectroscopic Mode → 110 µm x 110 µm	8
Colour Mode with charge Summing		
Pixel Gain Modes	**Linearity**	**# Thresholds**
High Gain Mode	~10 ke^-	2
Low Gain Mode	~20 ke^-	
Pixel Counter Modes	**Dynamic range**	**# Counters**
1-bit	1	2
4-bit	15	2
12-bit	4095	2
24-bit	16777215	1
Pixel Readout Modes	**# Active Counters**	**Dead Time**
Sequential Count-Read (SCR)	2	Yes
Continuous Count-Read (CCR)	1	No

Medipix3 Pixel Schematic

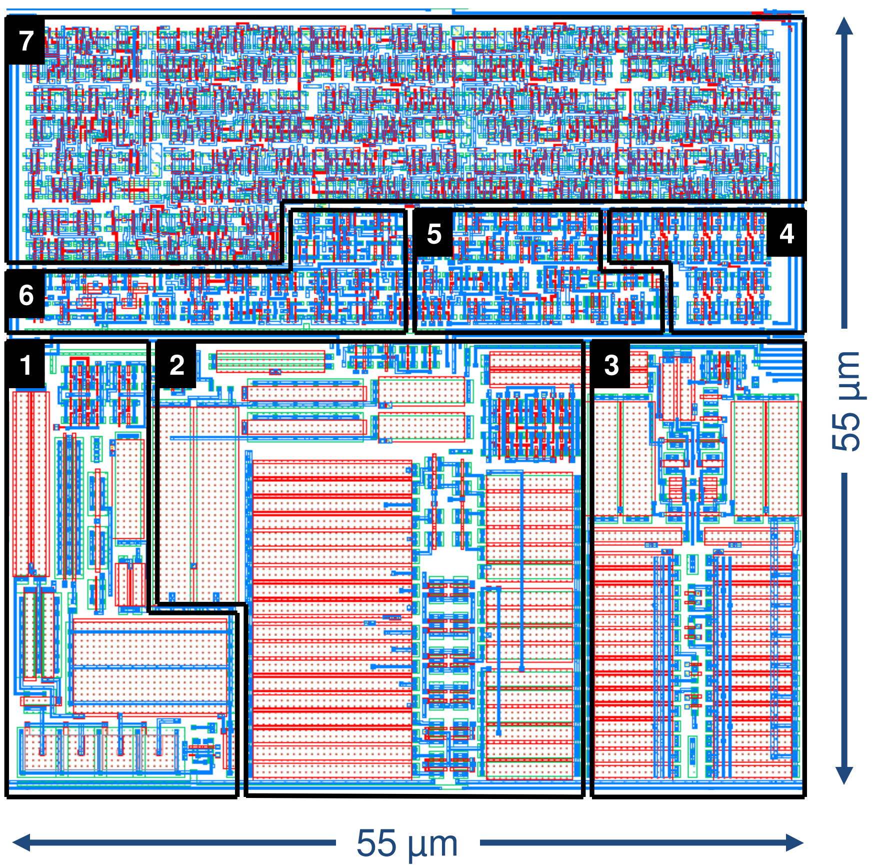


Pixel Layout

- Fully exploit the available 130 nm CMOS technology
- Full custom layout fits ~1500 transistors per pixel

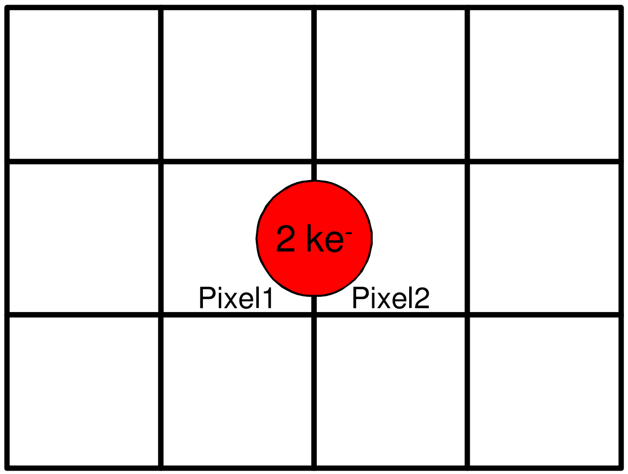
Motivation
Medipix3
Timepix2
VELOpix
Conclusions

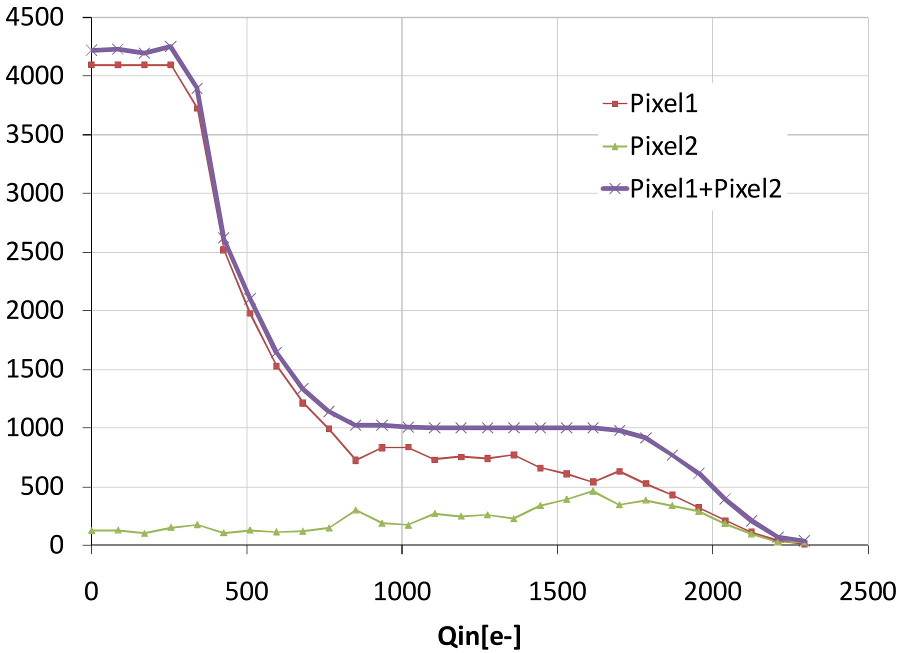
1. Preamplifier
2. Shaper
3. Two discriminators with 5-bit threshold adjustment
4. Pixel memory (13-bits)
5. Arbitration logic for charge allocation
6. Control logic
7. Configurable counter



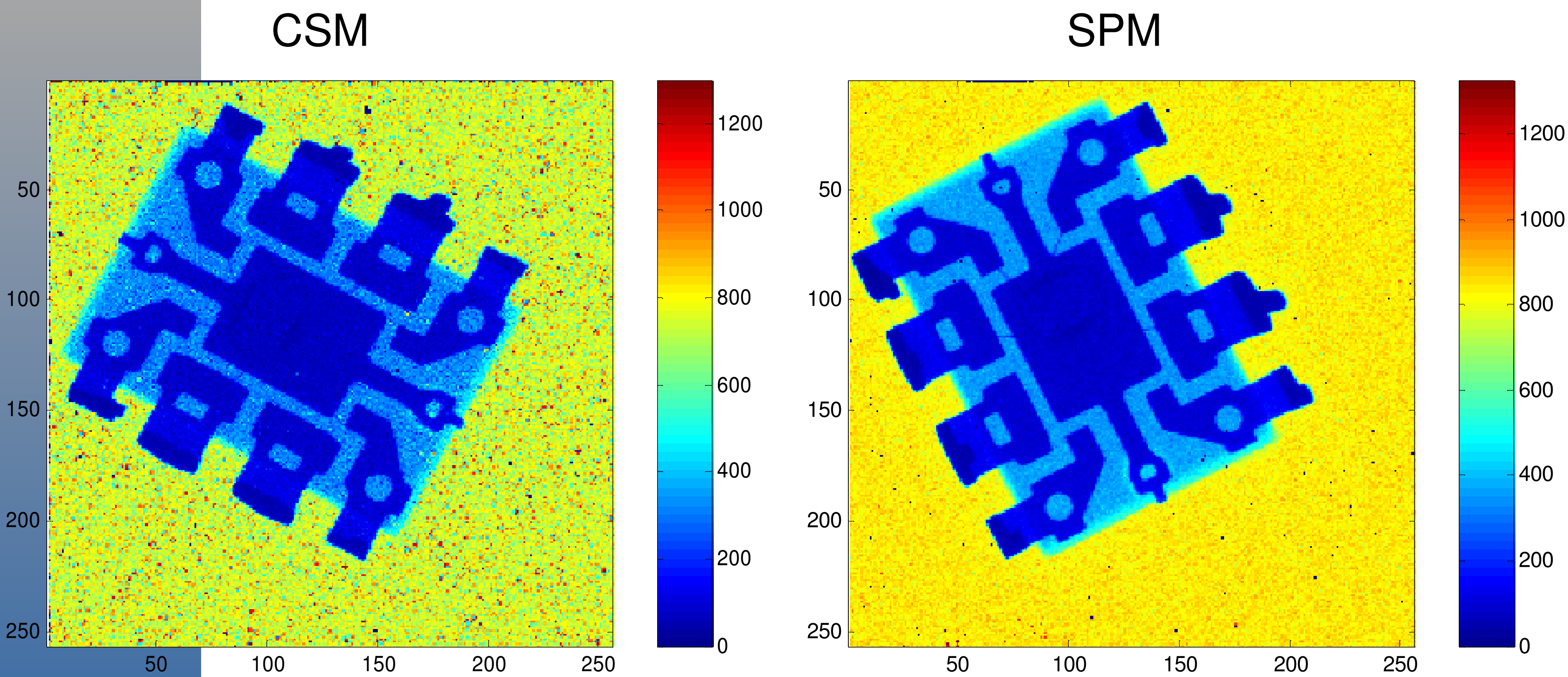
Medipix3 s-curve in charge summing mode

- Energy of incoming particle is reconstructed after charge summing and hit allocation architecture





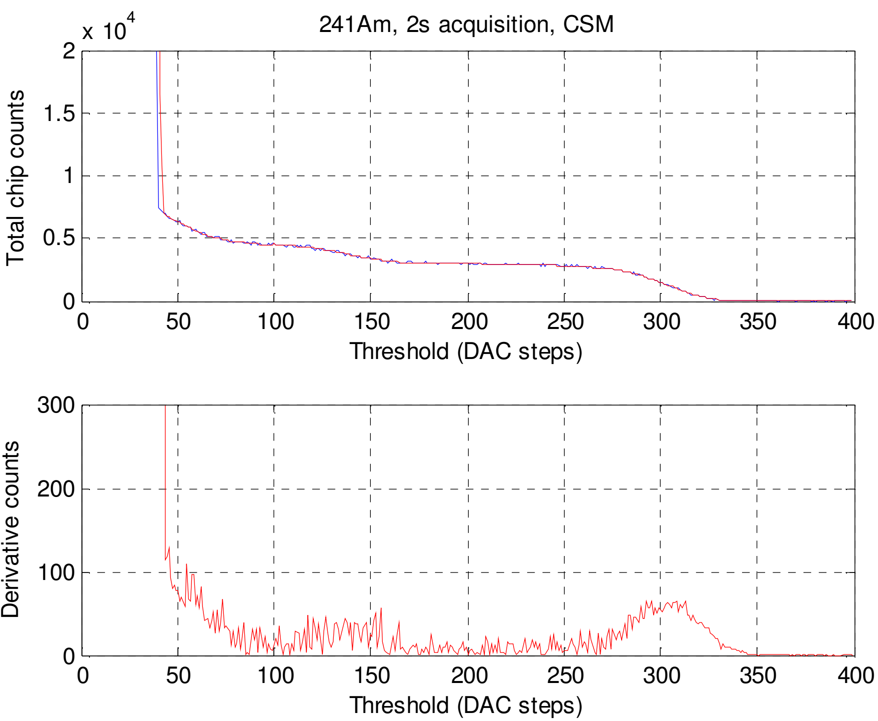
Imaging in CSM and SPM



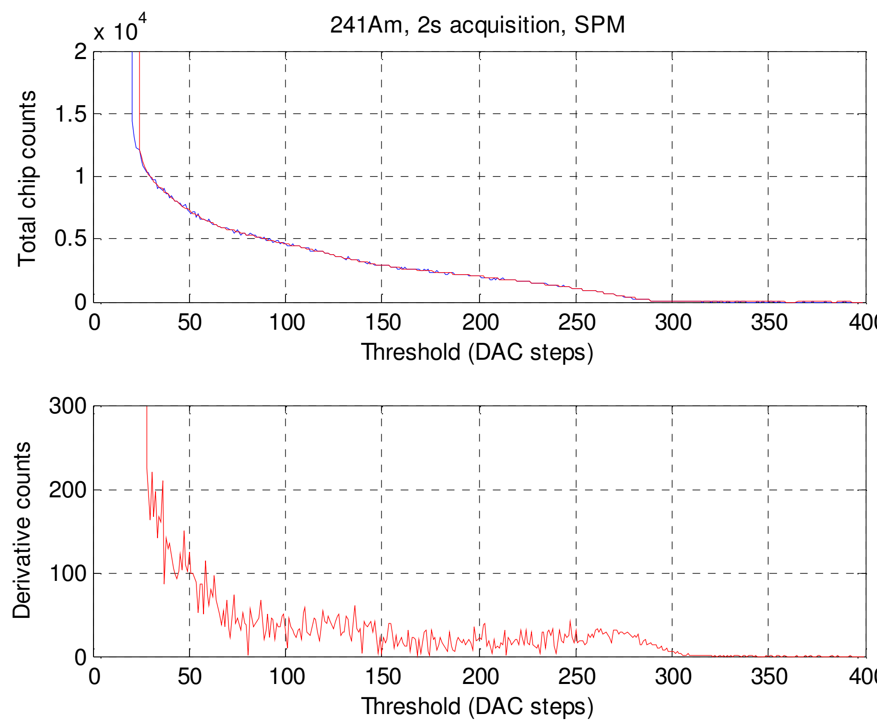
X-ray 60kV, 10mA, Acq=0.1s

Spectroscopic behavior (CSM and SPM) Am^{241}

CSM



SPM

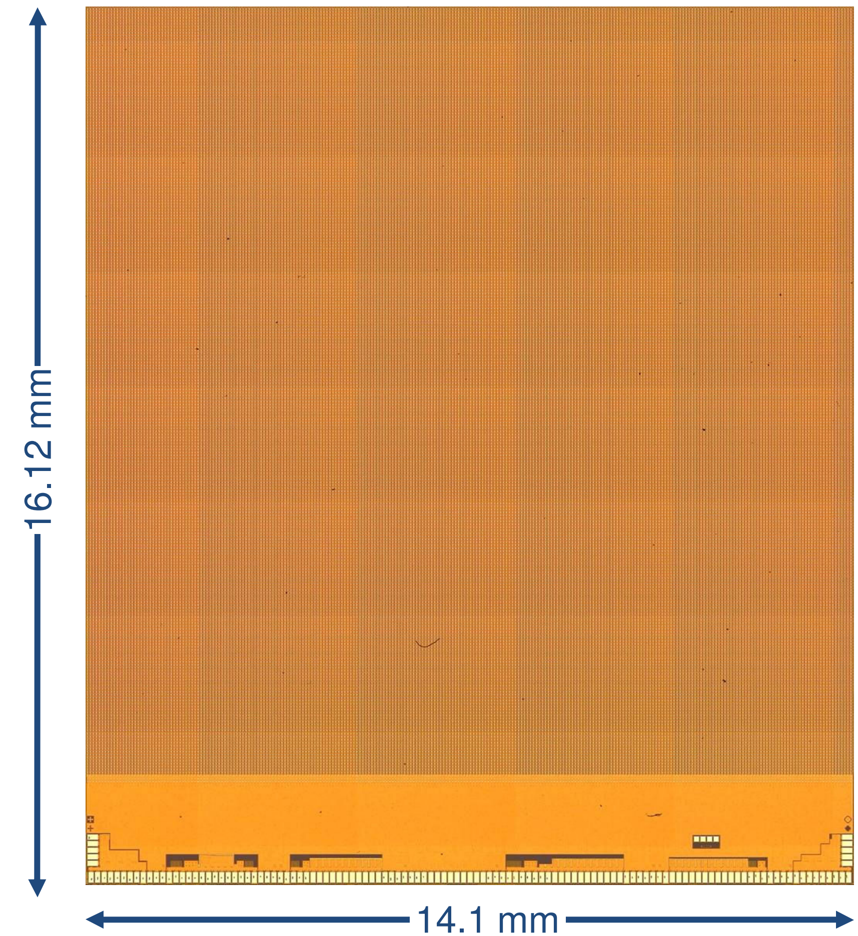


Pixel measurements summary

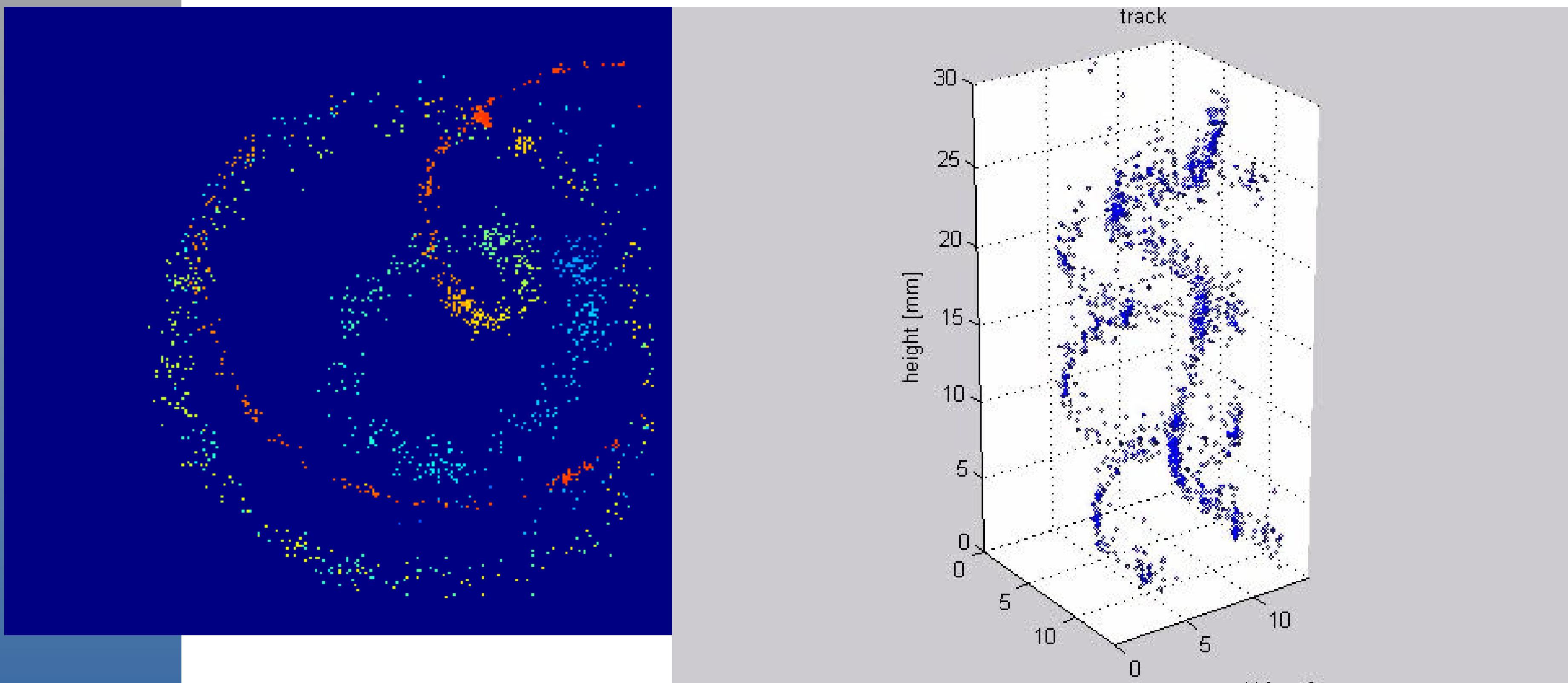
		Single Pixel Mode	Charge Summing Mode
CSA Gain		11.4 mV/ke^-	
CSA-Shapper Gain	High Gain	34 nA/ke^-	
	Low Gain	20 nA/ke^-	
Non-Linearity	High Gain	<5% up to 10 ke^-	
	Low Gain	<5% up to 20 ke^-	
Peaking time		~110 ns	
Return to baseline	High Gain	<1.5 µs for 12 ke^-	
	Low Gain	<2.5 µs for 25 ke^-	
Electronic noise (unbonded)	High Gain	~60 e^-rms	~130 e^-rms
Unadjusted Threshold spread	High Gain	~2300 e^-rms	~3200 e^-rms
Adjusted Threshold spread	High Gain	~150 e^-rms	~210 e^-rms
Minimum threshold	High Gain	~1100 e^-	~1500 e^-
Pixel power consumption	High Gain	8 µW	15 µW
	Low Gain		

Timepix chip (2006)

- Pixel matrix of 256 x 256 pixels (55 µm x 55 µm)
- Pixels are configurable:
  - Event counting
  - TOT
  - Arrival time
- External clock (up to 100MHz) is used as a time reference
- Minimum threshold ~750 e-
- > 35 Million transistors
- Typical power consumption <1 W with 100 MHz external clock
- 250nm CMOS IBM process



Example - Timepix coupled to Ingrid



90Sr with NEXT-4 in a B field of 195 mT (M. Fransen, Nikhef)

From Timepix to Timepix2

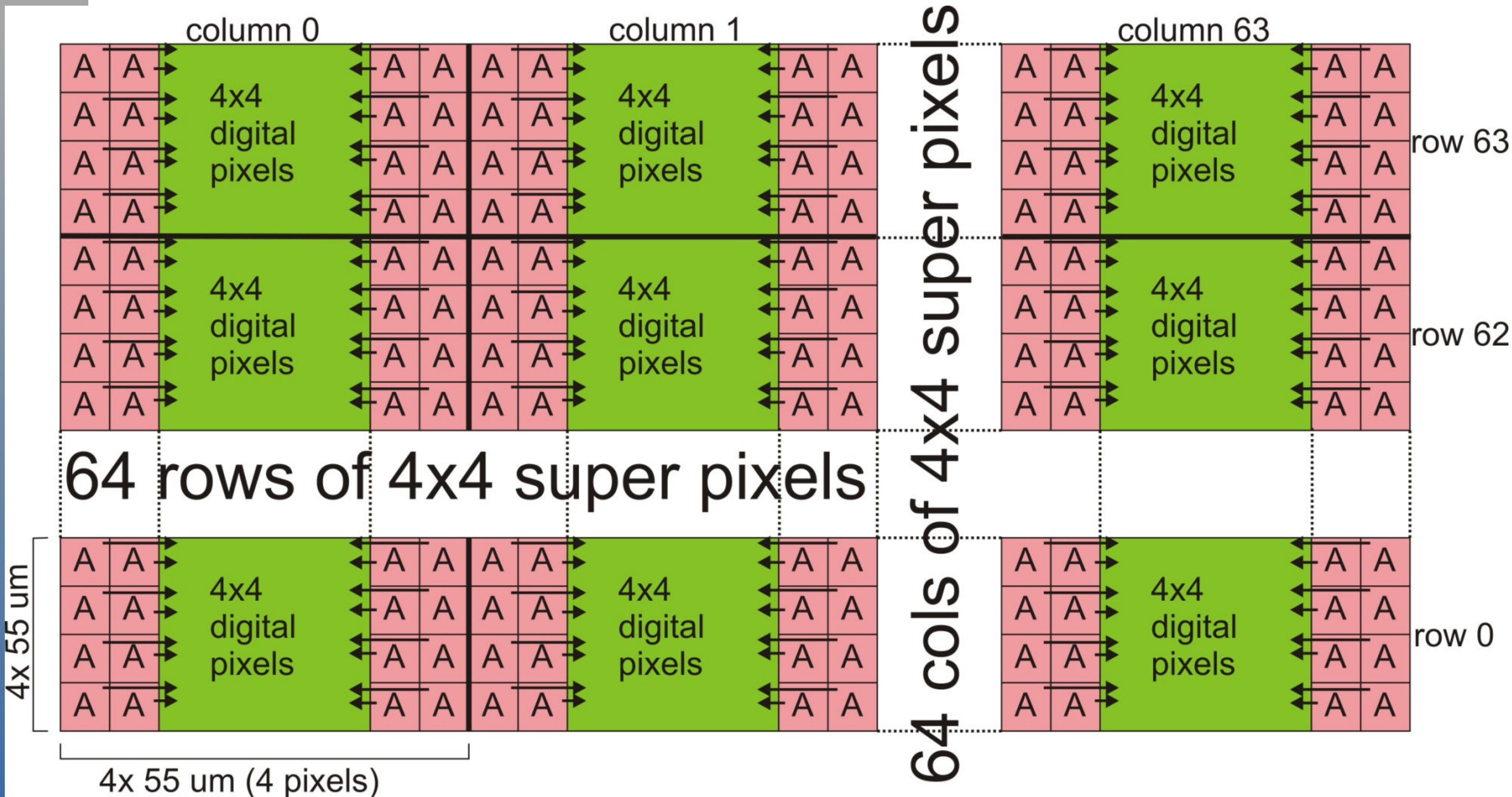
- Timepix chip (2006) architecture originally designed for imaging is used for single (or sparse multiple) event readout

- Non triggerable
- Full frame readout only
  - Serial readout (100 MHz): ~100 fps
  - Parallel readout (100 MHz): ~3000 fps
- Either arrival time OR amplitude information
- Timewalk > 50ns (Preamp rise time ~100 ns)
- 6-metal CMOS 0.25 µm

Timepix2 requirements

- Time resolution 1-2 ns (local oscillator)
- Pixel size 55 x 55 µm
- Time stamp and TOT recorded simultaneously
- Triggerable externally
- Fast OR
- Sparse data only
- No event counting mode
- Configurable → HEP platform for many projects
- 8-metal CMOS-DM 0.13 µm

Timepix2 proposed pixel architecture

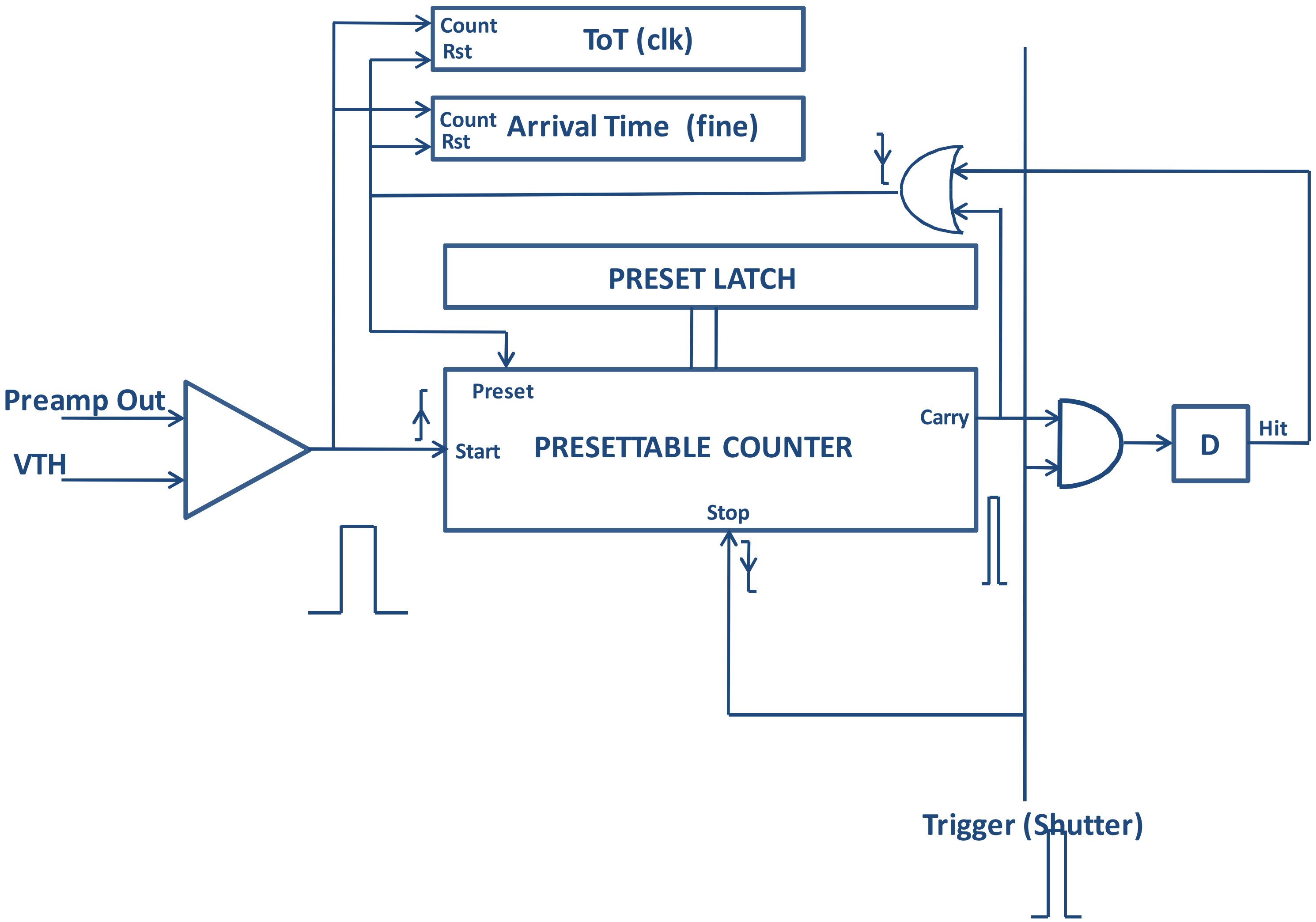


Super pixel (4x4)

- Advantages:
  - Shared analog (bias, power) and digital (clock, common logic, etc) resources
  - Good to isolate analog from digital
  - Use standard cells in digital blocks as much as possible
  - Faster column readout (8 bit parallel bus)

- Disadvantages:
  - Lost of uniformity (not all pixels look the same): Different Cin and cross-talk
  - Efficient shielding must be designed to avoid cross-talk between digital and input

Preliminary proposed pixel architecture

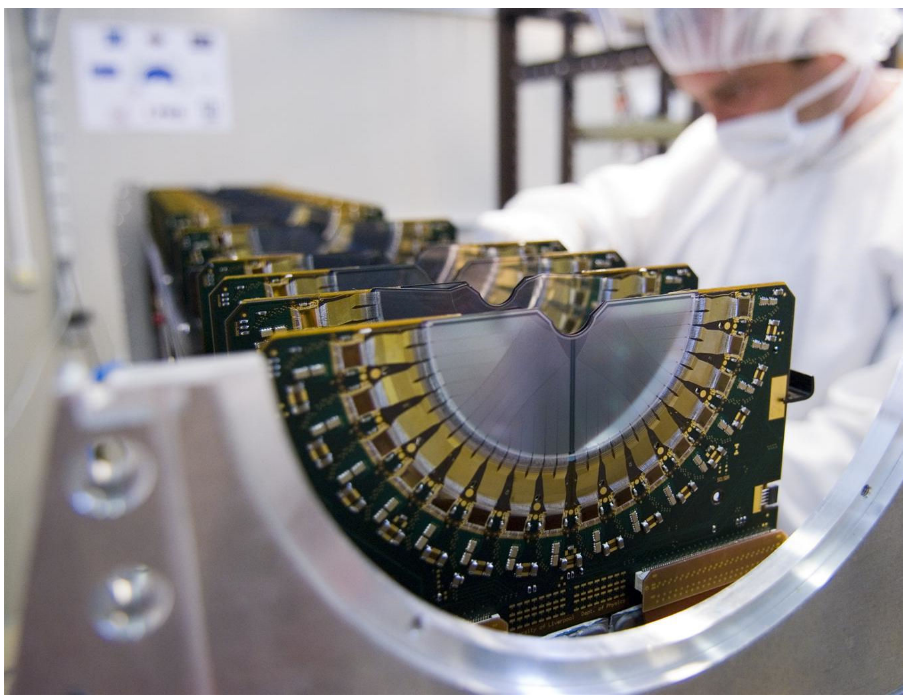


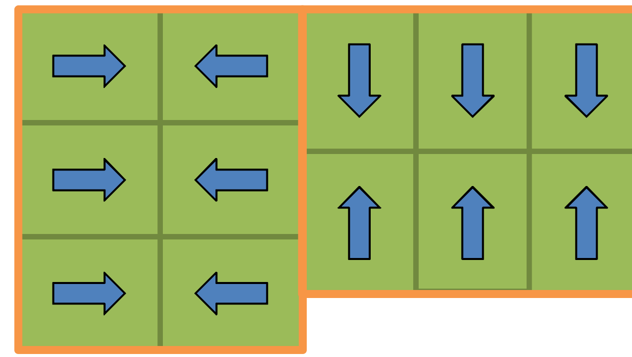
Why an LCHb upgrade?

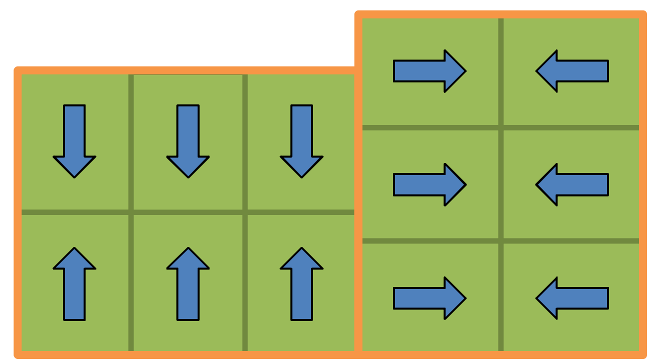
- LHCb upgrade wants to increase the b-event yield by a factor >10 to efficiently address remaining open physics questions and aims to collect 100 fb^{-1} in 5 years
- Increasing the luminosity x 10 is rather 'easy' for LHCb (enhanced beam focusing can be introduced at 'any' time and does not require an LHC-upgrade).
- Solution: Only a more sophisticated trigger can maintain good efficiencies. Decided not to rebuild new & more complex L0-trigger electronics, but execute the trigger algorithms on all data in software
- A new DAQ system must transfer all, zero-suppressed front-end data straight into a large computer farm, through a huge optical network & router
- **All front-end electronics must be adapted or rebuilt to digitize, zero-suppress and transmit event data at 40MHz**

From VELO to VELOpix

- The LHCb Vertex Detector (VELO, r-phi strip detector) will be replaced in ~2015 by an upgraded version of the Timepix chip high resolution pixel detector







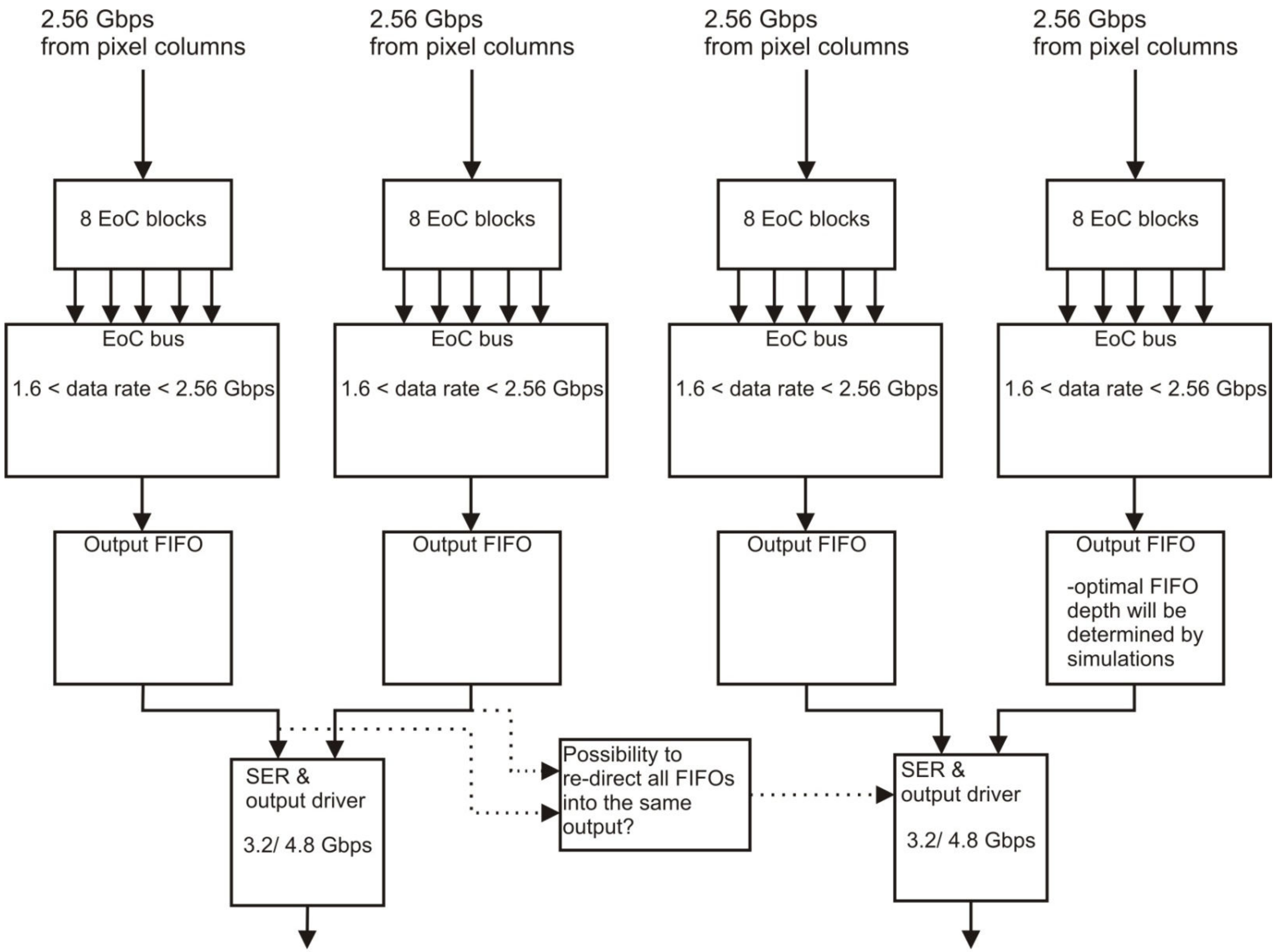
Why pixels?

- The square pixel (55um x 55um) results in equal spatial precision in both directions, removing the need for a double sided modules and saving a factor 2 in material
- The extremely low occupancy (< 2 ppm) environment is ideally suited to the time-over-threshold conversion, as the efficiency will not suffer from the relatively large (1us) dead time
- It is a very 'economic' way (power & space) to obtain >6 bit digitization
- Through-silicon-via technology allows a novel module assembly.

- Average particle rate per BX
- Average data rates (Gbit/s)

VELOpix chip digital architecture (T. Poikela)

- Data compression at super-pixel → pack and send pixels TOT value
- Token pass column readout architecture (8 bit at 40 MHz → 320 Mbit/s)



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Analog synergy between Timepix2 and VELOpix

	Timepix2	VELOpix
Analog requirements	Very similar (see previous slide)	
General working mode	Free-running or Triggered with programmable preset	Fully free-running (40 Mfps)
Pixel matrix	256 x 256	
Arrival time resolution	25ns (BX) / 1 .. 2ns	25ns (BX)
TOT dynamic range	8-12 bits	4 bits
Pixel architecture	Super Pixel: 4x4	
Layout architecture	Cluster together the digital parts of the pixel	
Readout	Sparse (token pass) 8-bit parallel column readout	
Fast OR	Yes	
Readout speed	flexible (serial to parallel)	~fixed by experiment

Advantages of designing Timepix2 before VELOpix

- Timepix2 is an approved project by the Medipix3 collaboration with an assigned budget (2-engineering runs)
- Timepix2 will be build in 130nm IBM-DM reusing many blocks from Medipix3
- Timepix2 and VELOpix analog frontend have almost identical specs
- The general working mode (Triggered vs Imaging) doesn't exclude similar column readout schemes in both projects (4x4 clustering, 8-bit column parallel bus, 40 MHz clock, …)

- Due to the pixel logic density VELOpix will probably have to be designed in 90nm (or even 65nm?) → Timepix2 will be a very good tool to check most of the required functionality in the VELO upgrade.

Conclusions

- Following Moore's law ASIC designers are able to implement more functionality per pixel while maintaining the compact pixel area when a more downscaled process is used
- Medipix3 uses a analog and digital inter-pixel communication in order to correct the effects of charge-sharing
- Timepix2 and VELOpix are successors of the Timepix chip which will exploit the high integration density of deeper submicron technologies
- The Timepix and VELOpix developments may have important lessons for the future Linear Collider Detector