Architecture of a Level 1 Track Trigger for the CMS Experiment

Ulrich Heintz (*Brown University*)

for

U.H., M. Narain (*Brown U*)

M. Johnson, R. Lipton (*Fermilab*)

E. Hazen, S.X. Wu (*Boston U*)

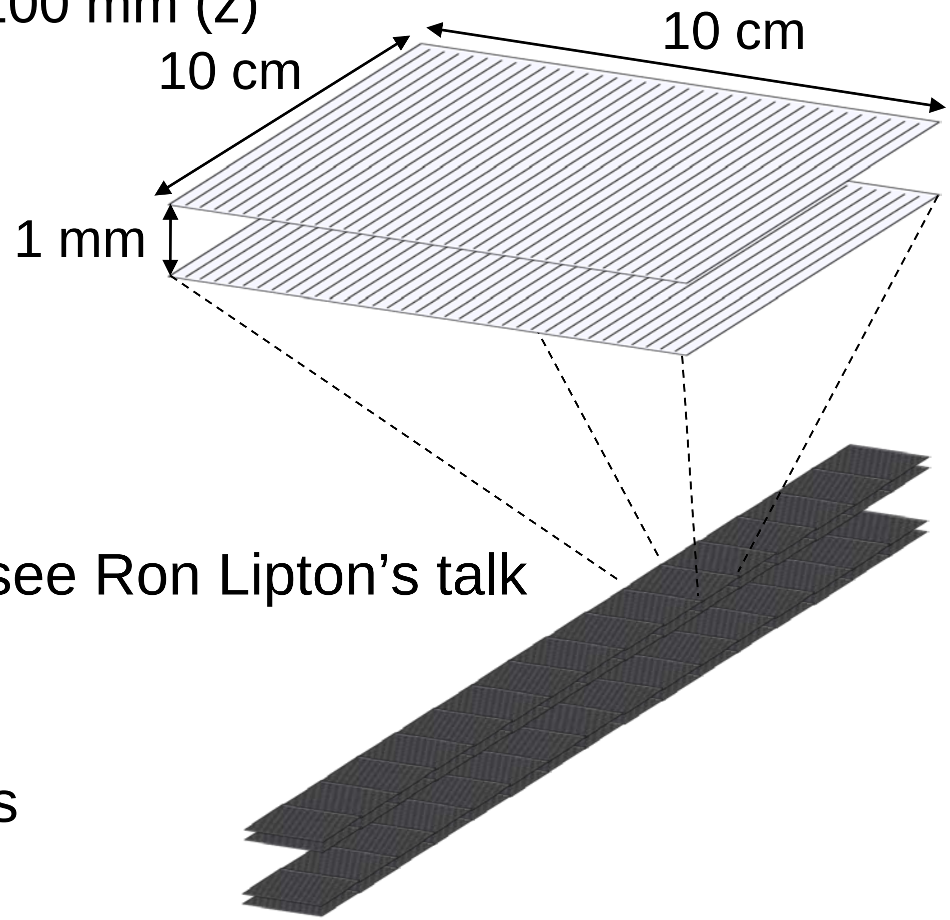
Workshop on Intelligent Trackers, LBNL, February 3-5, 2010

the problem

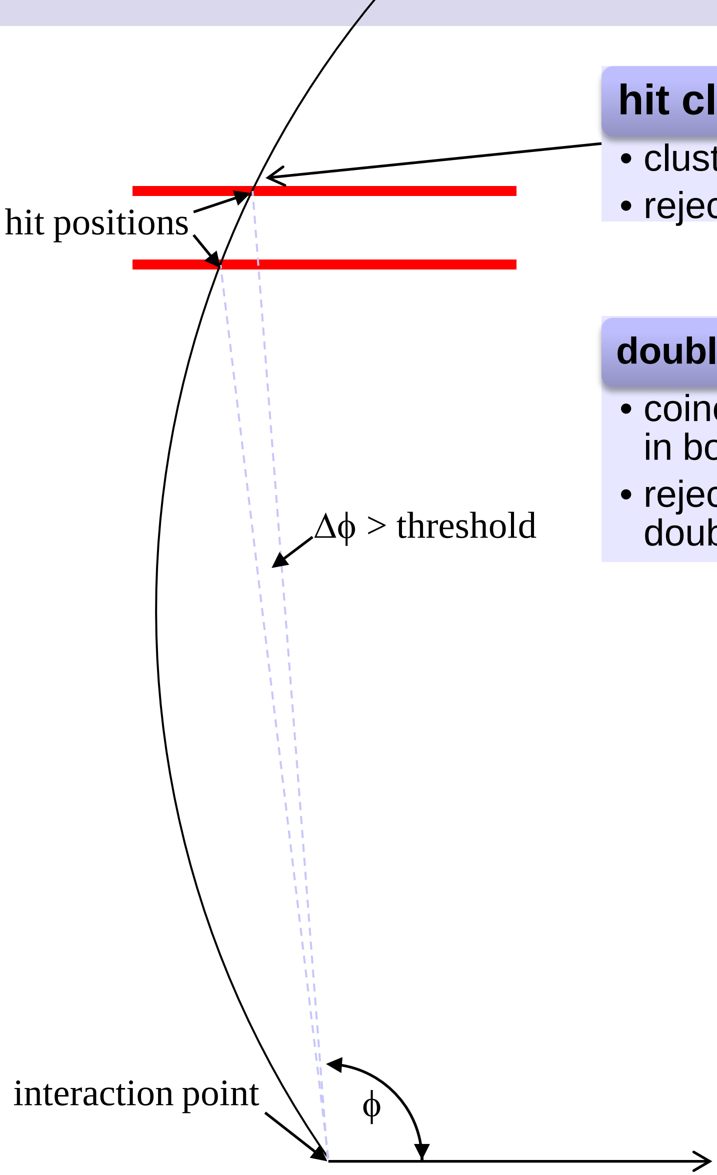
- SLHC
  - luminosity = 1035/cm2/s
  - 25 ns bunch spacing
  - ≈300 pp interactions/xing on average
- CMS
  - must keep level 1 trigger rate < 100 kHz
  - add tracking to level 1 trigger
    - trigger on tracks matched to electrons or muons
    - trigger on isolated tracks (e.g. from τ-leptons)
    - must be efficient down to low pT (≈2 GeV)

3D detector design

- silicon strip sensors
  - active area ≈100 mm (ϕ) x 100 mm (z)
  - ≈100 μm strip pitch
  - ≈1-5 mm strip length
- sensor stack
  - two coplanar sensors
  - spaced apart by ≈1 mm
  - one readout IC
  - for details of construction see Ron Lipton's talk
- rod
  - two layers of sensor stacks
  - spaced apart by ≈4 cm
  - for details of construction see Bill Cooper's talk



low-pT hit rejection

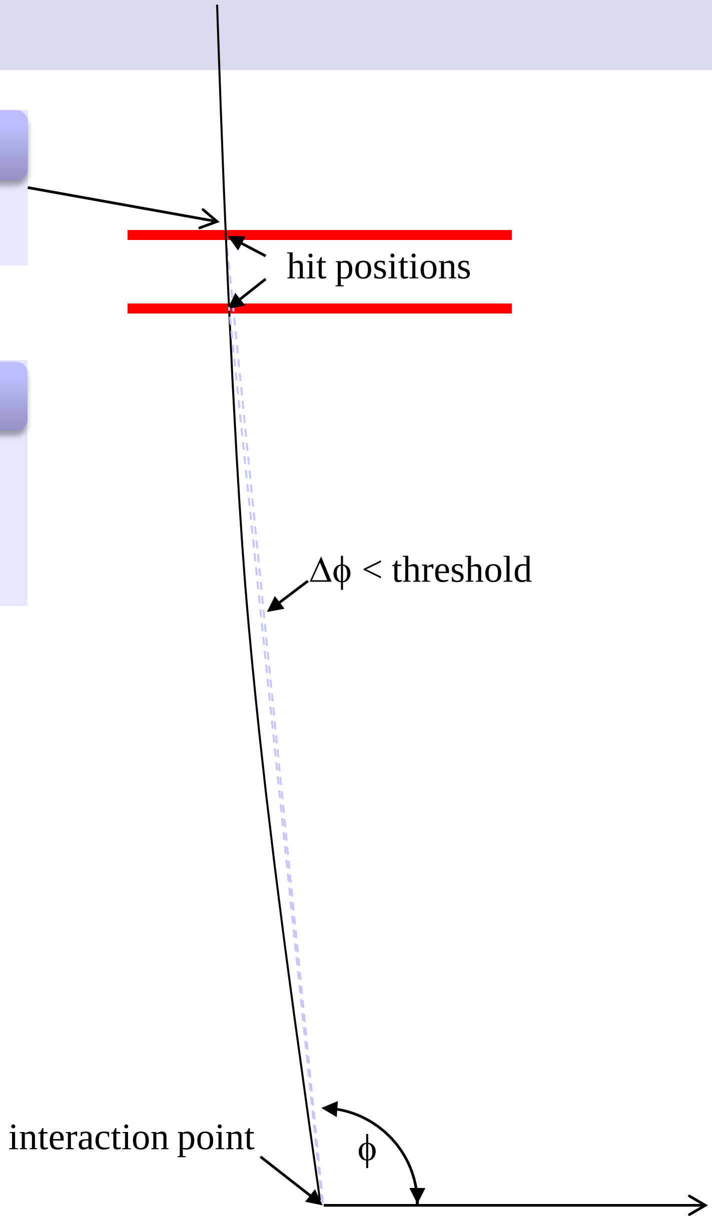


hit clusters

- cluster adjacent pixels
- reject clusters >2 pixels wide

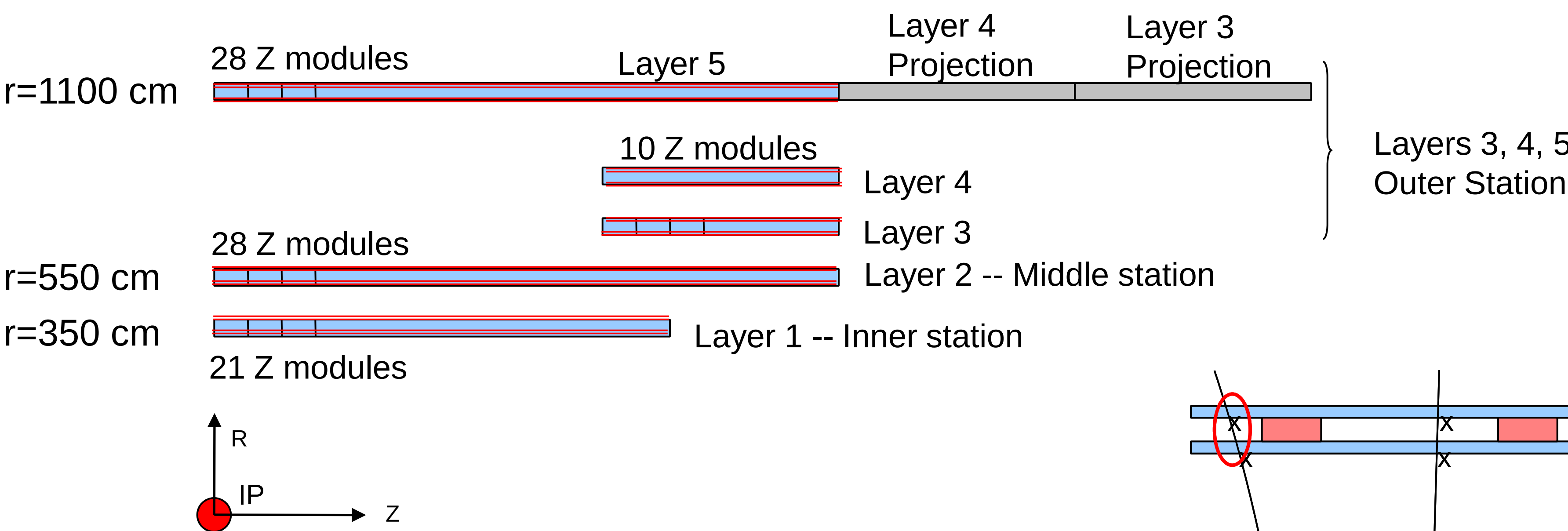
doublets

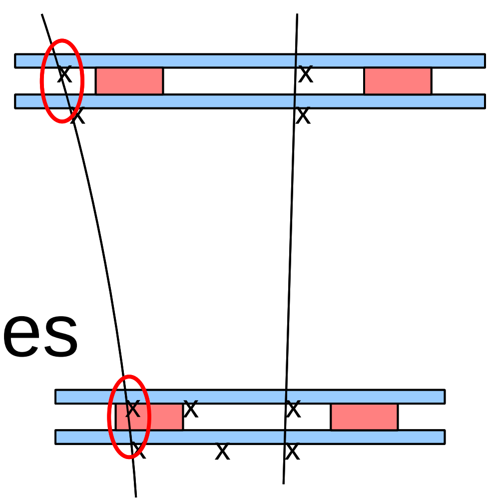
- coincidence between clusters in both sensors
- reject single clusters and doublets from soft tracks



detector geometry

- here: six layers of sensor stacks
  - three stations with two stacks $\approx$ 4 cm apart



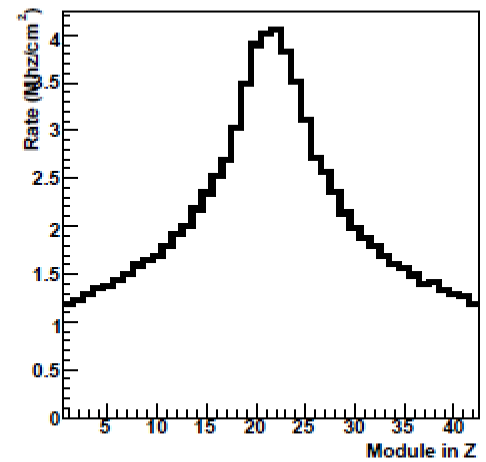


- same ideas apply to other geometries

rates

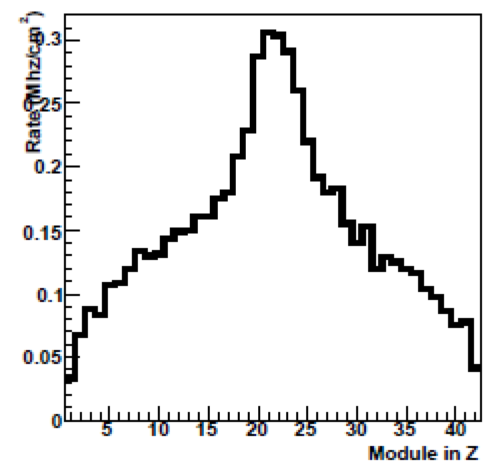
- MC simulation
  - PYTHIA minimum bias, <n>=200
  - cluster rate

R = 35 cm	R = 55 cm	R = 110 cm	@ z=0
≈4	≈1.6	≈0.2	MHz/cm^2
≈10	≈4	≈0.5	/xing/module



  - doublet rate
    - 1 mm stack separation

R = 35 cm	R = 55 cm	R = 110 cm	@ z=0
≈0.3	≈0.13	≈0.025	MHz/cm^2
≈0.7	≈0.3	≈0.06	/xing/module



data transmission off detector

- optical fiber links
  - average rate ≈$^1/_2$ max rate @ z=0
  - safety factor of ≈10
  - 20 bits/doublet
  - assume bandwidth of fiber links <10 Gb/s
  - inner station
    - ➔1.5 MHz/cm^2
    - 42 modules in z ➔ 4200 cm^2
    - ➔ 250 Gb/s per rod (2 stacks)
    - ➔ 30 links per rod
  - assume other stations have same number of hits
  - ➔ ≈2160 links for entire tracker

ϕ: 10 bits
z: 7 bits
pT: 3 bits

basic idea for off-detector processing

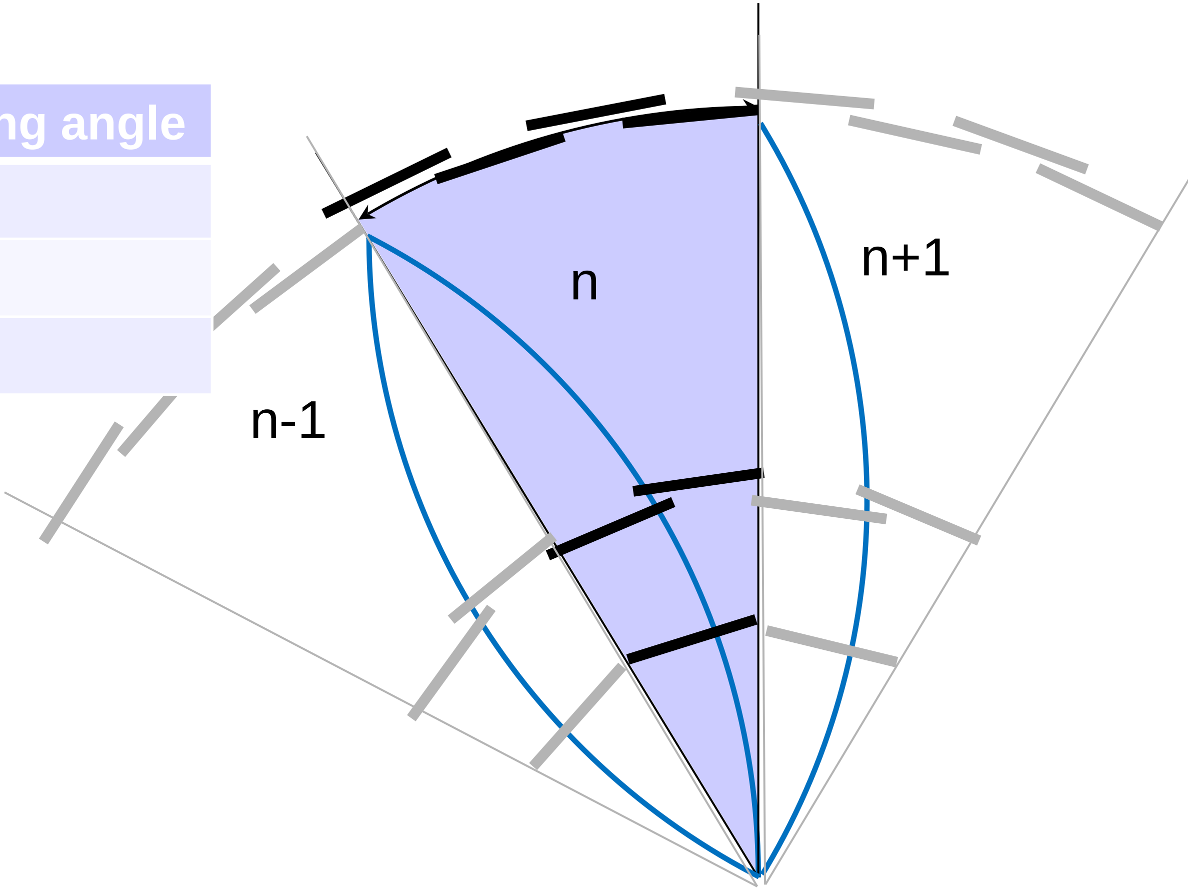
- for each sector
  - represent every possible hit combination by a logic “equation”:

    $S_{1i} \cap S_{1o} \cap S_{2i} \cap S_{2o} \cap S_{3i} \cap S_{3o}$
  - create a table of all possible equations in FPGA
  - load all hits for an event into registers in FPGA
  - evaluate all equations simultaneously in one clock cycle
  - equations which are satisfied correspond to reconstructed tracks
  - timing dominated by time needed to load hits into FPGAs
- problem
  - if we tried to do all six layers at one time
  - too many equations
  - too many inputs
  - need to factor problem

sector structure

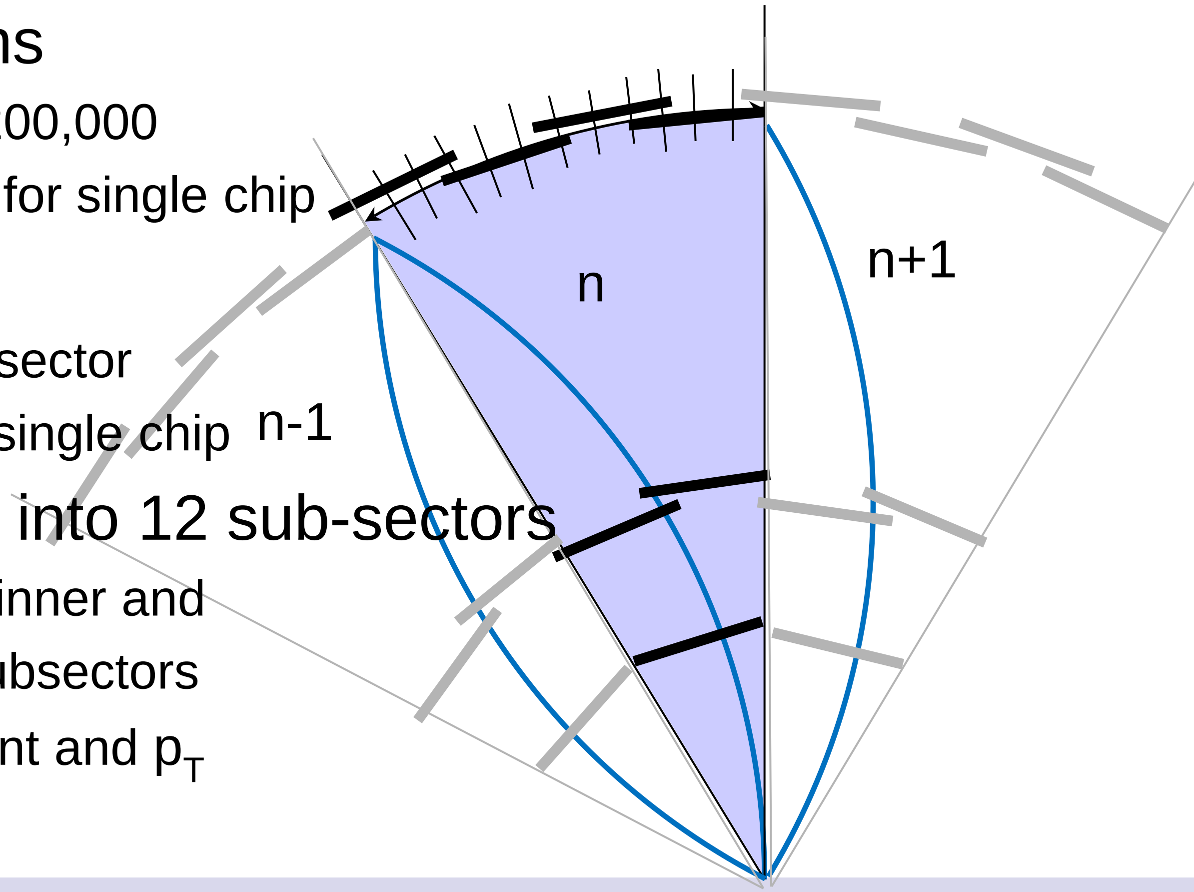
- trigger logic handles inputs from sectors n-1, n, n+1
- tracks must be contained in 3 adjacent sectors
- sector size determines min p_T for full acceptance

min p_T	sector opening angle
2 GeV	18^o
→ 2.5 GeV	15^o
5 GeV	7.5^o



equation count

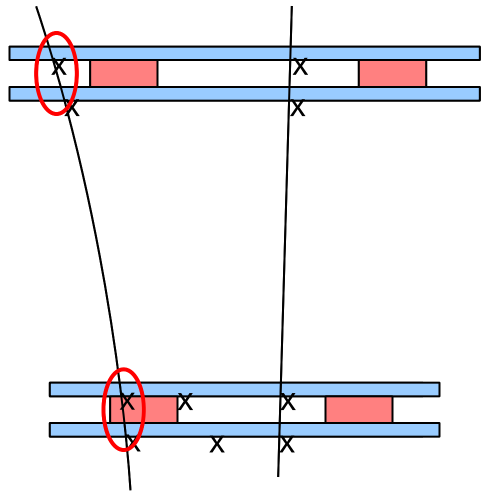
- assume azimuthal position resolution ≈ 0.1 mm
- number of ϕ positions per sector:
  - ≈ 2900 in outer station
  - ≈ 1450 in middle station (for each outer station position)
- number of equations
  - ≈ 2900 * 1450 = 4,200,000
  - too many equations for single chip
- number of fibers
  - 90 fibers from each sector
  - too many inputs for single chip
- divide outer station into 12 sub-sectors
  - route tracklets from inner and middle stations to subsectors using interaction point and p_T



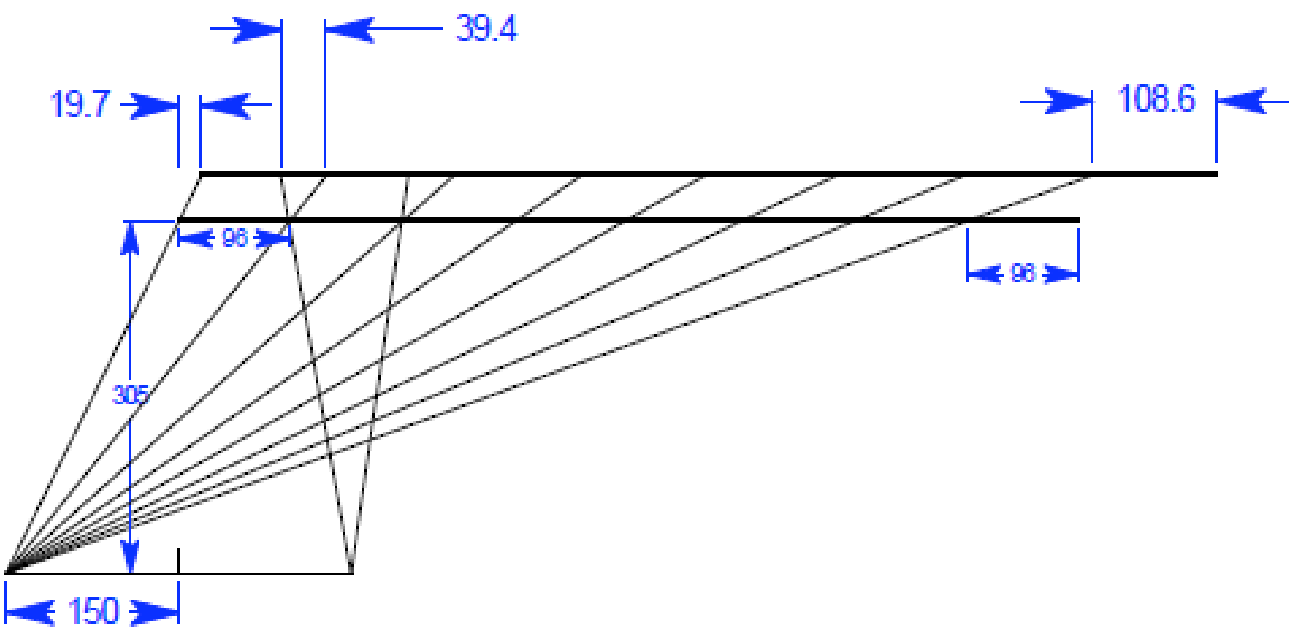
tracklets

- double stacks allow local track finding on each rod
- combine stubs from the two stacks in each station to form tracklets
  - drop in rate by about factor 4 (but need ≈30 bits/tracklet)
  - for each stack in inner layer need to process data from two adjacent stacks in z in outer layer

stub (2-layer coincidence)



Tracklet
(4-layer coincidence
with P_T validation)



tracklet processing

- processing done off detector
  - input 30 fibers per station
  - fits into current FPGA   (44 inputs at 10 Gb/s)
  - must do all processing in 25 ns
- local to each module
  - 42 modules in inner layer
  - need information from top and bottom stacks plus neighboring stack(s) for z overlap
  - sensor overlap in ϕ so no rod to rod communication
- data volume
  - 8 stubs/event/module @ 20 bits/stub ➔160 bits
  - fits into FPGA registers
  - compare all hits between stacks simultaneously in ϕ and z
    - z range restricted by length of IP
    - ϕ range restricted by min. p_T

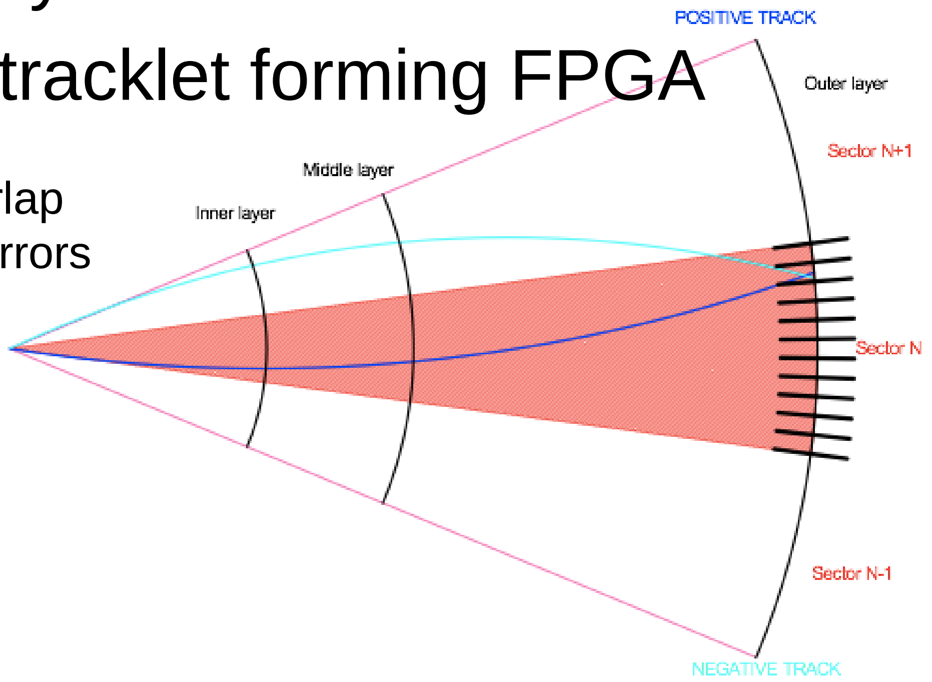
tracklet bandwidth

- simulation shows tracks are half the stub rate
- safety factor
  - 10 included fluctuations
  - should be less over rod ➔ use safety factor of 6
  - track density drops faster than stub density with z
  - use same density as for stubs (conservative)
- 40 tracklets/rod @ 30 bits/tracklet = 48 Gb/s

tracklet output

- sort tracklets by destination segment
  - send over dedicated fiber line
  - 12 segments/sector times 3 sectors = 36 fibers
    - 48 Gb/s divided among 36 fibers so 8 Gb/s fiber OK
  - project to 2 different layers
  - 72 output fibers from tracklet forming FPGA

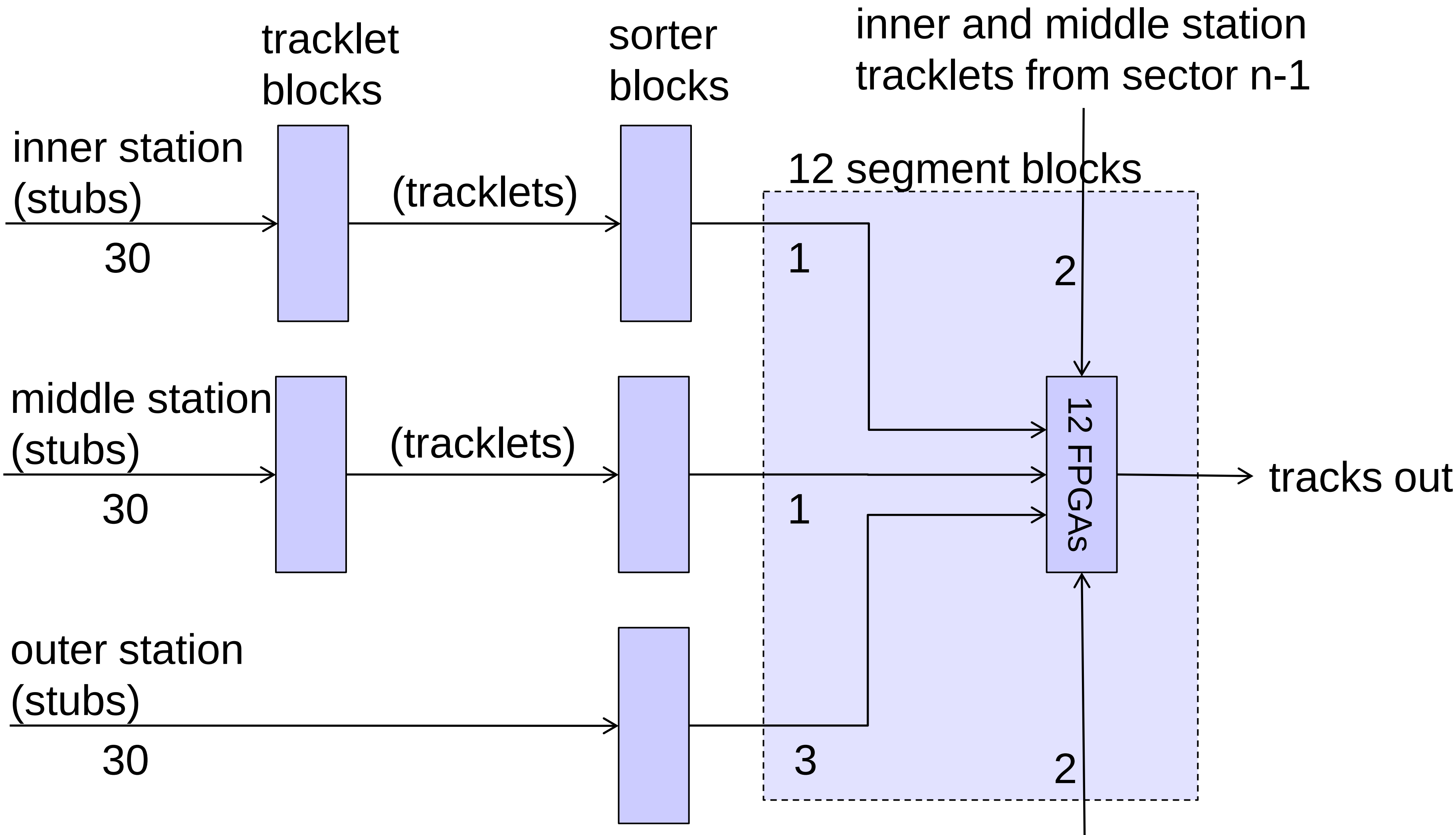
Segments must have overlap
to account for projection errors
(about 10% of segment)



sector processor

- receive tracklets from 2 stations in 3 sectors plus stubs from anchor layer in home sector
  - 1 fiber/rod/layer/sector for inner and middle layers
  - 3 rods times 3 sectors plus 3 for anchor station = 12 input fibers
  - plus 1 fiber for trigger output
- need to compare all possible combinations of input tracklets so need all tracklets in registers in FPGA
  - 3 times 40 tracklets/station = 120 tracklets in 12 segments
  - 10 tracklets/segment times 30 bits = 300 bits so OK
- output tracks ordered in p_T - highest first

sector processor



use additional sector processors pinned to inner, middle station

duplicate eliminator

- find tracks in all 3 layers simultaneously
  - ➔remove duplicate tracks
- receive data from 12 segments times 3 anchor stations or 36 fibers
- tracks ordered in pT ➔ simplifies search
- output tracks on perhaps 4 fibers

pipeline stages

- tracklet block
  - (1) load stub data from sensors
  - (2) form tracklets from stubs
  - (3) sort tracklets by destination segment
  - (4) transfer to segment processor
- segment processor
  - (5) receive tracklet data from 3 stations
  - (6) find tracks
  - (7) check z consistency
  - (8) transfer tracks to duplicate eliminator
- duplicate eliminator
  - (9) receive track data from all 3 layers
  - (10) compare inputs, eliminate duplicates
  - (11) send track data to L1 trigger

- $\approx$11 total pipe line stages for system
- $< 1\ \mu s$

optical link power

- 30 fibers in inner station/sector
- about same number of tracks in all stations ➔ 90 fibers/sector
- 24 sectors ➔ 2160 fibers
- power ≈1 watt/driver ➔ 2 kW

summary

- robust design
  - can lose a stub in any layer and still form track
  - sensor or chip failure does not impact trigger efficiency
- not constrained by FPGA size
- getting all required data into one place is an important constraint
- very large number of high speed links
  - reliability, mass, power of fiber links are critical
- verify rate estimates with LHC data