A high efficiency readout architecture for a large matrix of pixels.

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Alessandro Gabrielli, **Filippo Maria Giorgi**, Mauro Villa
I.N.F.N. & University of Bologna

Outline

- ▸ Target operating conditions
- ▸ Matrix overview
- ▸ Readout architecture
- ▸ Simulations & Efficiencies
- ▸ Demonstrator chip submission
- ▸ Applications

Target conditions

- An architecture that can be integrated with **hybrid pixel** sensors or **MAPS** (Monolithic Active Pixel Sensor)

- **100 MHz/cm²** hit rate (compatible with the rate foreseen in SuperB Layer0)

- **0.25 – 2.0 µs** BCO clock:
  - Time Counter clock, represents the time granularity of the events.

- **60-100 MHz** Matrix Readout Clock

- **3 Gbit/s** data bus bandwidth per chip

Matrix Overview

320 pxl

256 pxl
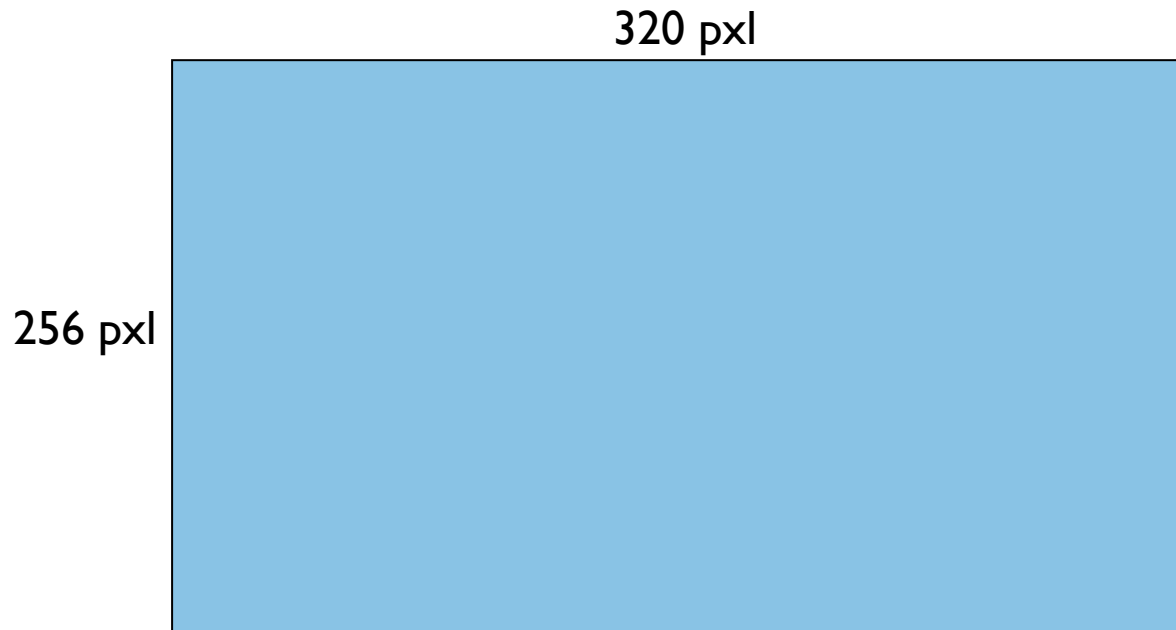
- 80K pixel matrix
- Total area ~ 1.3 cm^2
- 130 Mhit/s
- 40 microns pitch

Matrix Overview
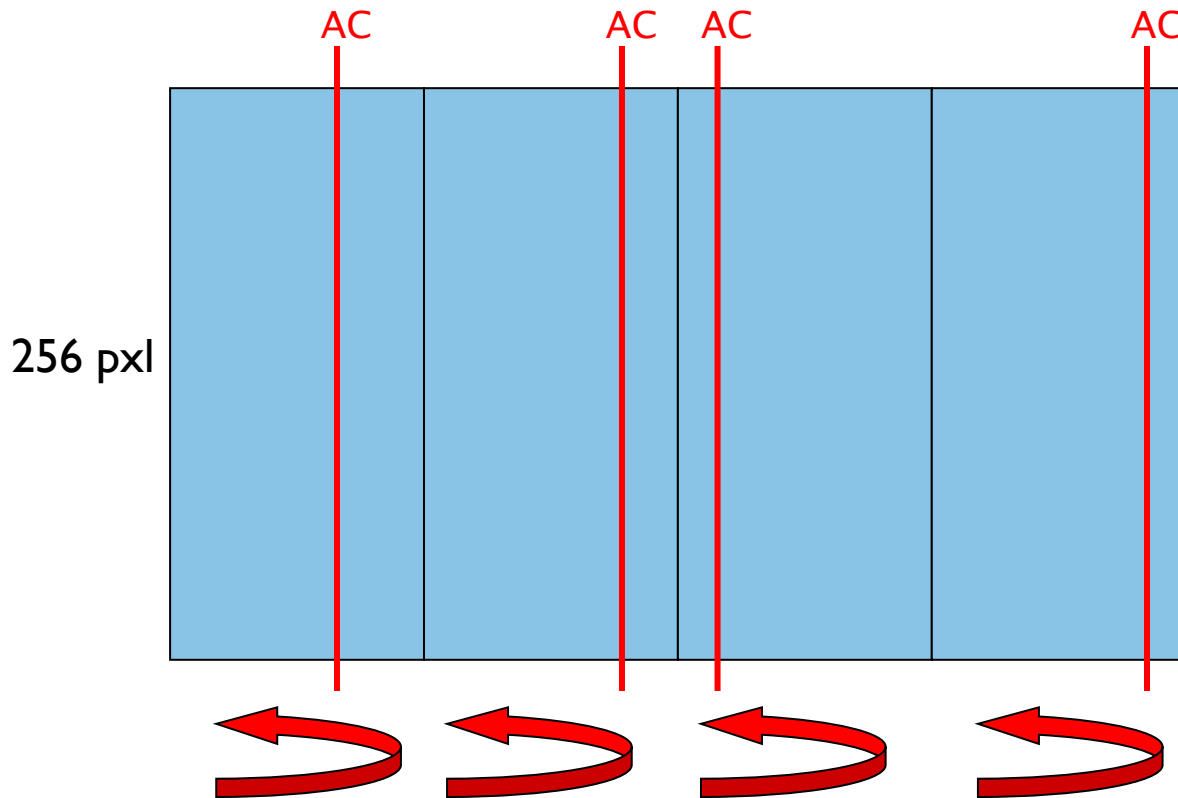
256 pxl

AC AC AC AC
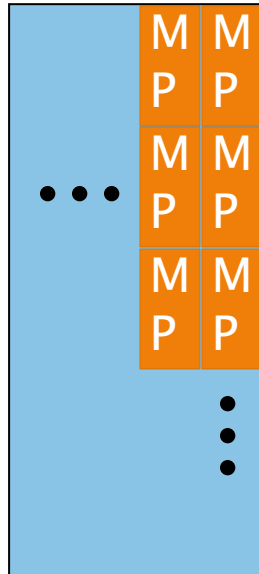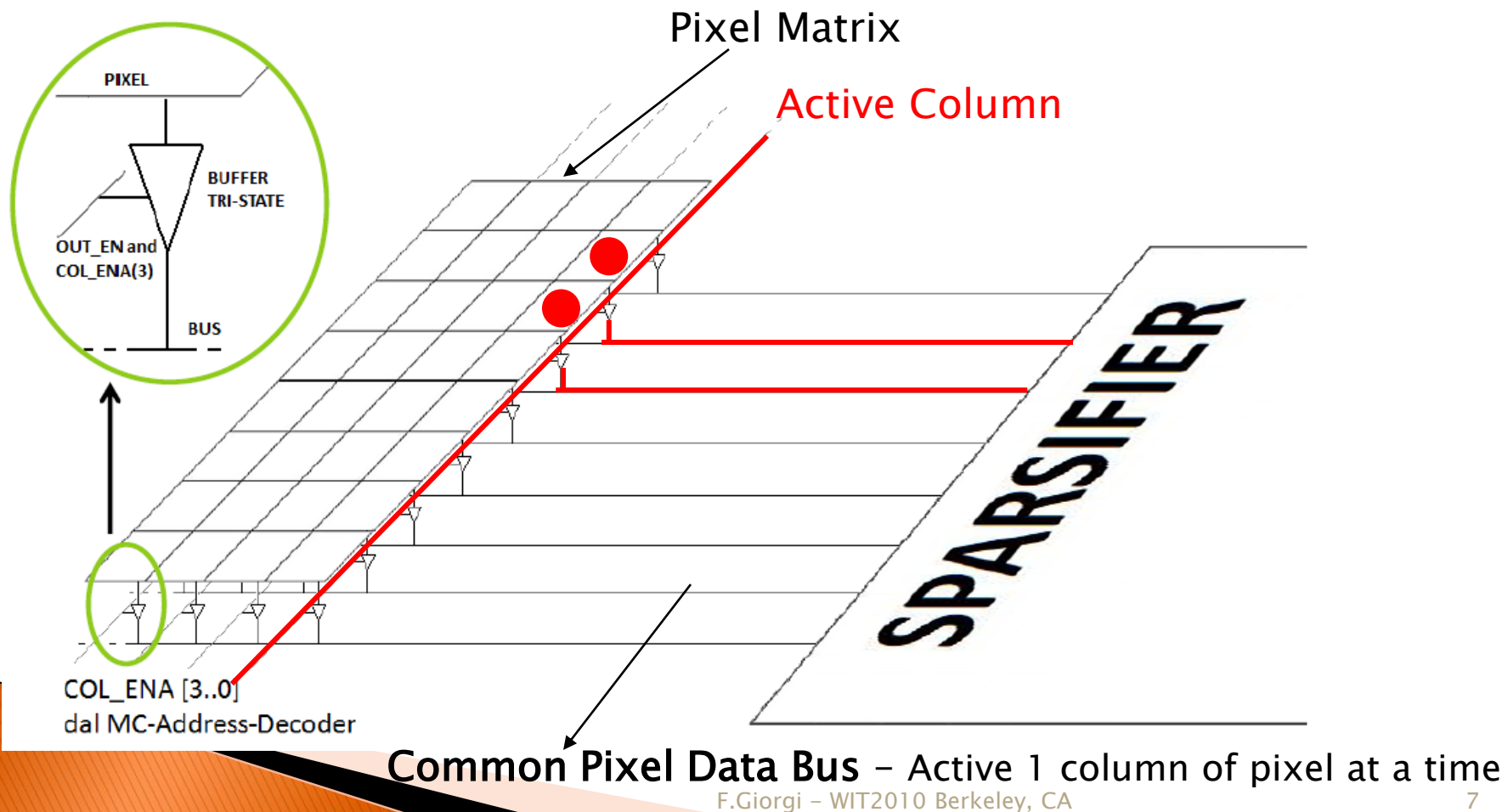
- 80K pixel matrix
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- 40 microns pitch

- 4 indep. submatrices
- 4 indep. column scans
- 4 active columns (AC) read in 1 clk

1024 pixels analyzed in 1 CLK cycle:
@50MHz → 5 Gpxl/s

Matrix Overview

M P	M P
M P	M P
M P	M P

• Pixel groups called Macro Pixels
• MP shape 2x8 pxl
• Reduce logic in every pixel
• Reduce global routes towards readout logic.

• 80K pixel matrix
• Total area ~ 1.3 cm^2
• 130 Mhit/s
• 40 microns pitch

• 4 indep. submatrices
• 4 indep. column scans
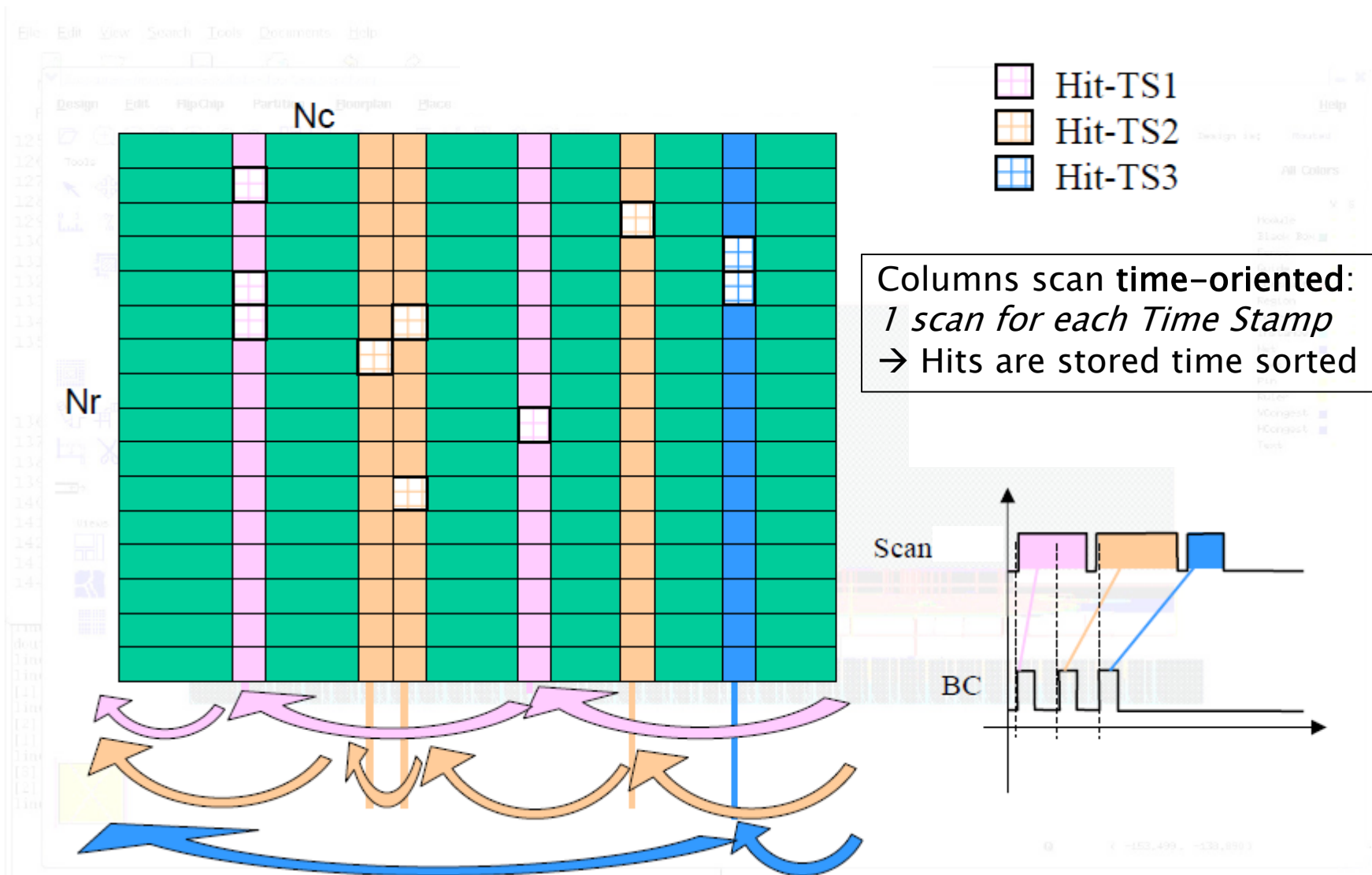• 4 active columns (AC) read in 1 clk

1024 pixels analyzed in 1 CLK cycle:
@50MHz → 5 Gpxl/s

Matrix overview

- Binary **pixels matrix**
- Hit readout through a column-wide **shared data-bus**

Pixel Matrix

Active Column

PIXEL

BUFFER TRI-STATE

OUT_EN and COL_ENA(3)

BUS

SPARSIFIER

COL_ENA [3..0]
dal MC-Address-Decoder

Common Pixel Data Bus – Active 1 column of pixel at a time

Submatrix Scan Policy

Hit-TS1
Hit-TS2
Hit-TS3

Columns scan **time-oriented**:
*1 scan for each Time Stamp*
→ Hits are stored time sorted

The Macro Pixels

- Matrix is divided into MPs: **group of pixels** (2x8)
  - MP global lines:
    - **Fast-OR line:** (MP output) inclusive OR of all pixel latches.
    - **Freeze line:** (MP input) disable the reception of new hits.
  - On BCO clock edge all MPs **with active fast-OR** :
    - Gets frozen
    - Are associated to the current value of BCO counter (Time Stamp) in a LUT memory of the readout
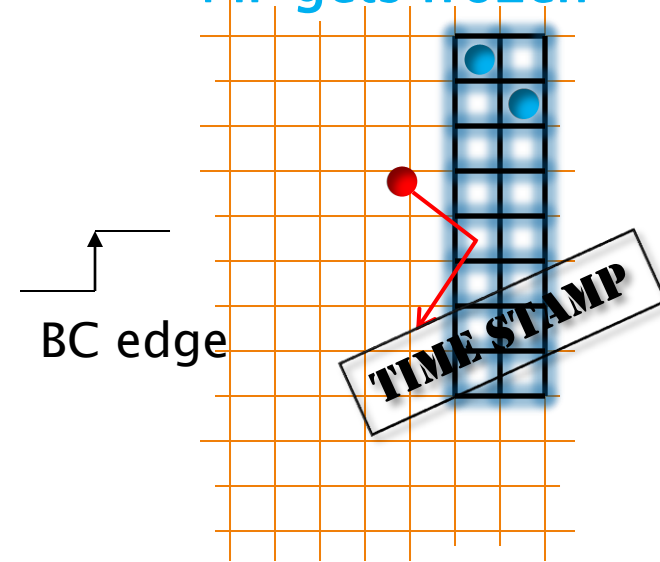   - Waits to be scanned and reset
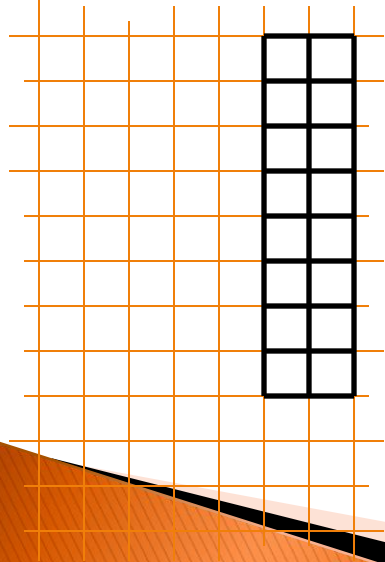
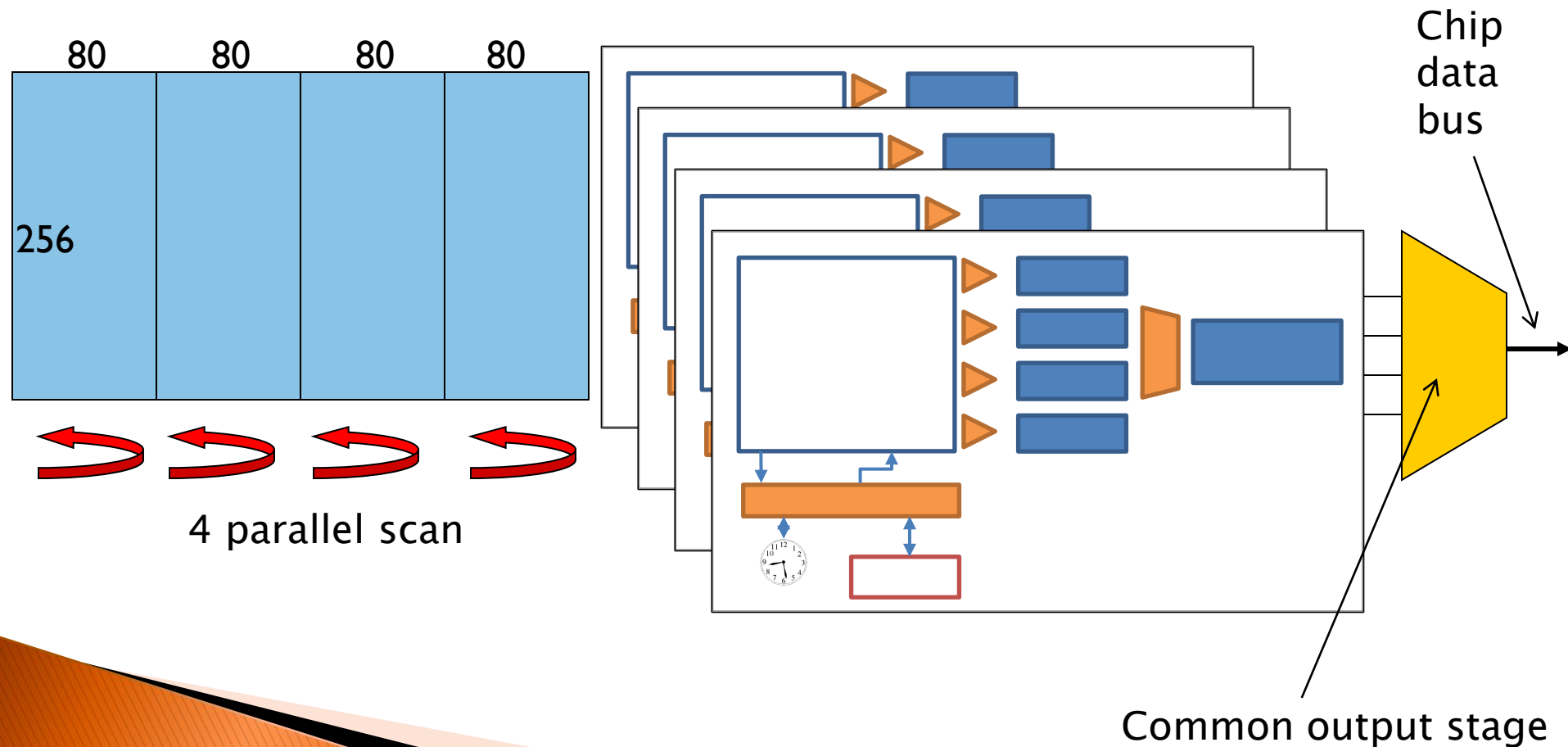**MP reset after read**   **Active Fast-OR**   **MP gets frozen**
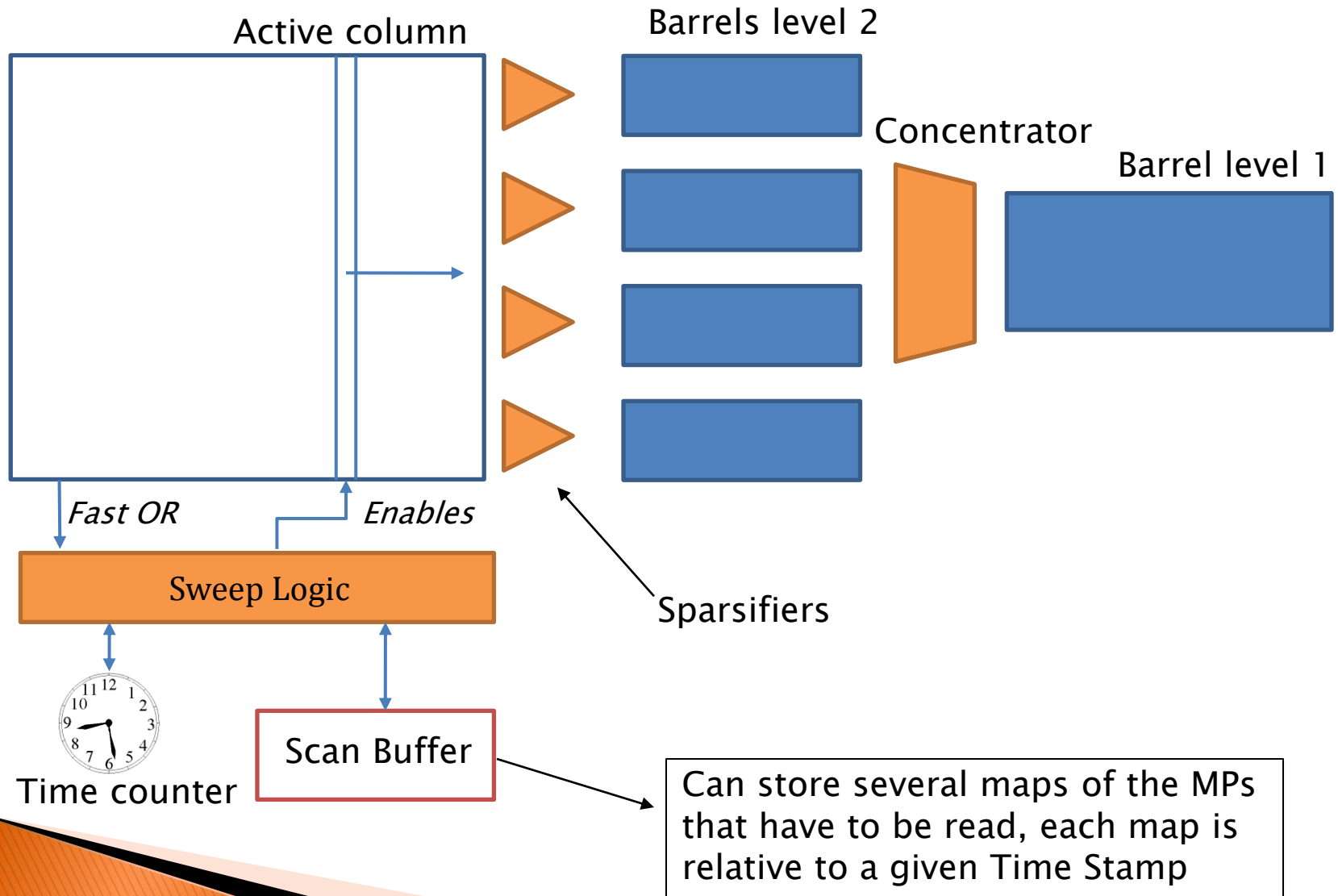
BC edge

TIME STAMP
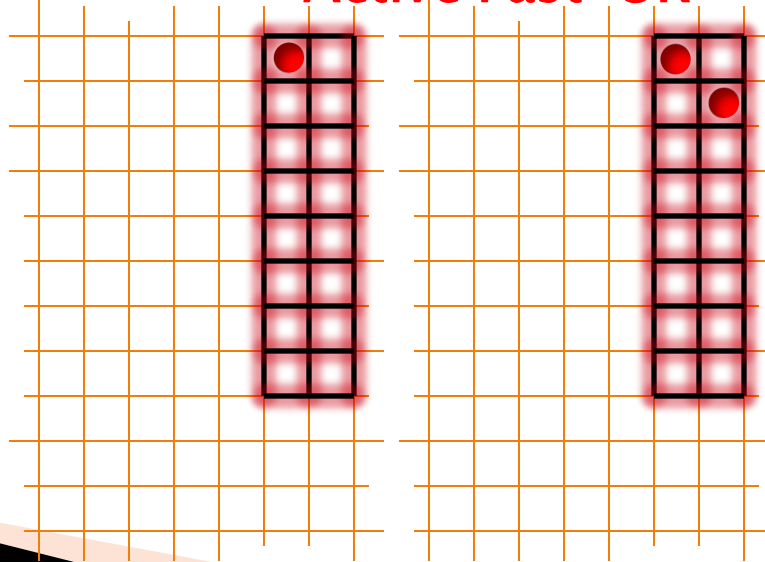
Matrix readout architecture

- Each sub-matrix scan has its own readout & scan logic
- All readout working in parallel
- Common final output stage

80   80   80   80

256

4 parallel scan

Chip data bus

Common output stage

Sub-matrix readout architecture

Active column

Barrels level 2

Concentrator

Barrel level 1

Fast OR

Enables

Sweep Logic

Sparsifiers

Time counter

Scan Buffer

Can store several maps of the MPs that have to be read, each map is relative to a given Time Stamp

Zone sparsification
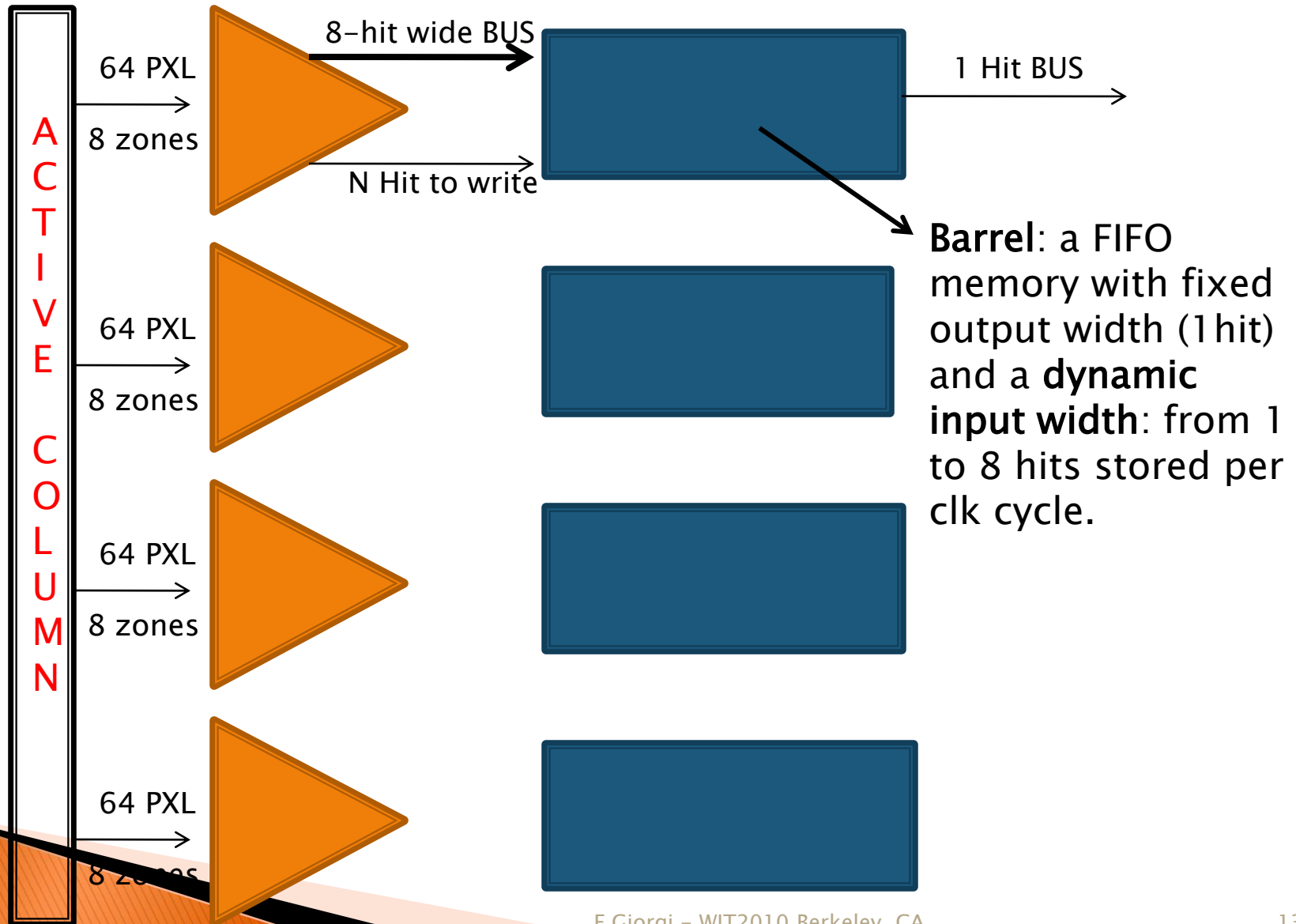
Active Column

Zone 0
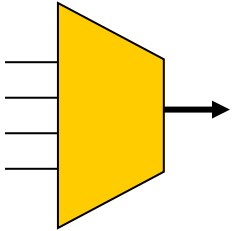
Zone 1
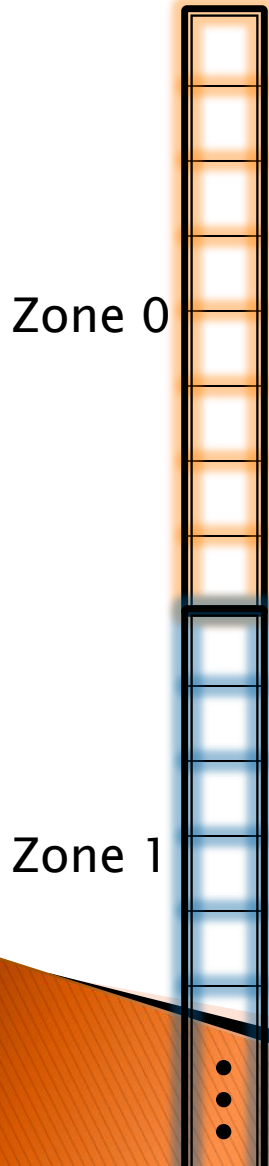
Active Column

- The **256 pixels** of the Active Column are **divided into 32 vertical zones** (1x8 pixels each)
- Every **HIT** stored in FIFO queue contains the information of a zone, **not of a single pixel**:
  - HIT= (**Zone address**+ **Zone pattern**)
    - X zone address = Column address for 80 columns →7 bits
    - Y zone address : 32 vertical zones → 5 bits
    - Zone pattern: 8-pixel zone → 8 bits

- **Time Stamp**: since the hits are time sorted, the relative TS word is stored at the beginning of each hit sequence. TS is 8-bit wide

TS

The sparsifiers and barrels

ACTIVE COLUMN

64 PXL

8 zones

8-hit wide BUS

N Hit to write

1 Hit BUS

64 PXL

8 zones

64 PXL

8 zones

64 PXL

8 zones

Barrel: a FIFO memory with fixed output width (1 hit) and a **dynamic input width**: from 1 to 8 hits stored per clk cycle.

Output stage data-bus solutions

1. FULL resolution Hit + time stamp
   - 8 bit TS   (modulo 256 BCO counter)
   - 9 bit X address (320 pixels)
   - 8 bit Y address (256 pixels)
   - TOT   **25 bits**
   - → expected rate 130 MHit/s per chip = 130MHz x 25bit = <u>3.2 Gbps</u>

2. Zone sparsification & time sorting of the hits (TS heading the relative hits, 1 MHz BC clock) lead to:
   - 2 bit Barrel L2 address (→1/4 of submatrix: 80x64 pxl)
   - 2 bit Barrel L1 address (1 submatrix: 80x256 pxl)
   - 7 bit X address (80 pixels)
   - 3 bit zone Y address (8 vertical zones for each L2 barrel)
   - 8 bit zone pattern
   - TOT 22 **bits**
   - → expected rate: 130 (+1 TS) * 22 = <u>2.8 Gbps</u>

   BUT: assuming a x4 cluster factor of the form 2x2: in 87.5% of cases 2 hits only & in 12.5% are required 4 hits
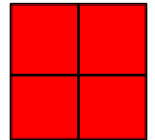
   - → [(22*2)* 0.875 + (22*4)*0.125] *25 Mtrack s^{-1} cm^{-2} * 1.3 cm^2
     - Weighted average ~ <u>1.6 Gbps</u>

VHDL model simulations

- VHDL models verification
- First-order estimation of the optimal parameters of the architecture in several working conditions:
  - Barrels depth
  - Zone width
- Long batch runs for efficiency estimation in function of the operating conditions (RDclk, rate etc…)
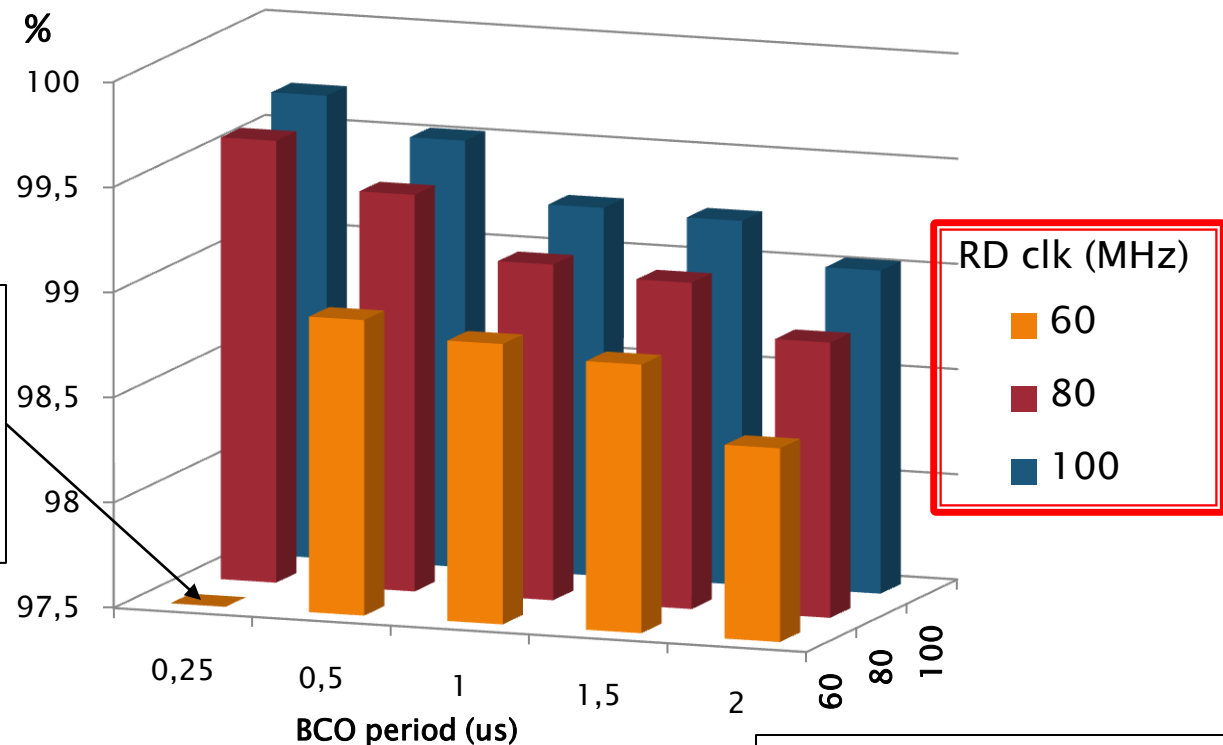
Efficiencies

- Two sources of inefficiency due to digital readout:
  - ◦ **Frozen MP inefficiency**: the hits generated on a frozen MP or on an already activated pixel are lost.
  - ◦ **Overflow inefficiency**: when a buffer is full it looses the eventual incoming hits.

- NO sensor efficiency is taken into account in these simulations. We give numbers relative to the digital readout architecture only.

Frozen MP Efficiency @ 100 MHz/cm^2

(1-ineff.)

(Random and no clusters → **no zone benefits** at this rate)

Efficiency drop induced by the overflow of *Scan Buffer* →
Longer freezing time

Overflow efficiency 100%
No barrel overflow

| frozen effi.					BCO (us)		
		0,25	**0,5**	**1**	**1,5**	**2**
	100	99.7	99,5	99,3	99,2	99,0
Rd_clk (MHz)	**80**	99,6	99,4	99,1	99,1	98,8
	60	97,5	98,9	98,8	98,8	98,4

NB: with a double rate, Rdclk=80MHz and BC=1 us → efficiency is 97.6%

SuperPix0 – demonstrator with smaller matrix

- Submitted Sept. 2009
- Technology STM 130 nm
- Hybrid Pixels Matrix 128x32 pixels, 50 μm pitch (1/20 of the target matrix area)
- Only 2 readout instances implemented
  - The readout instances are oversized respect to the matrix height (32 vs 256 pixels), but the connections implemented allows to stimulate all the components.
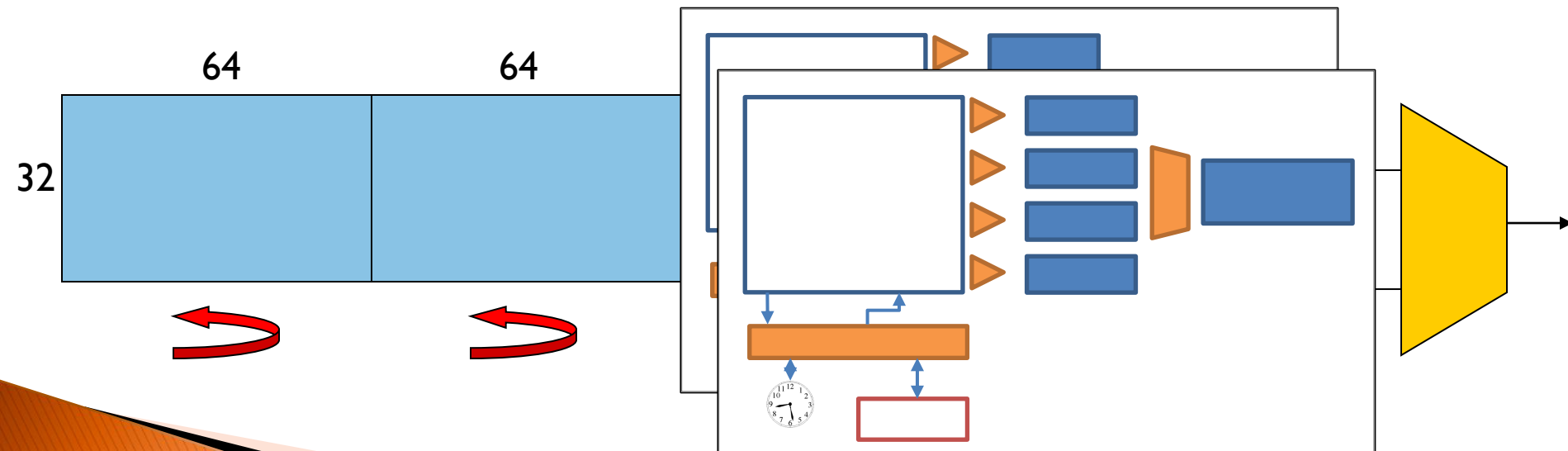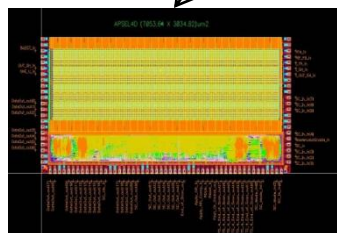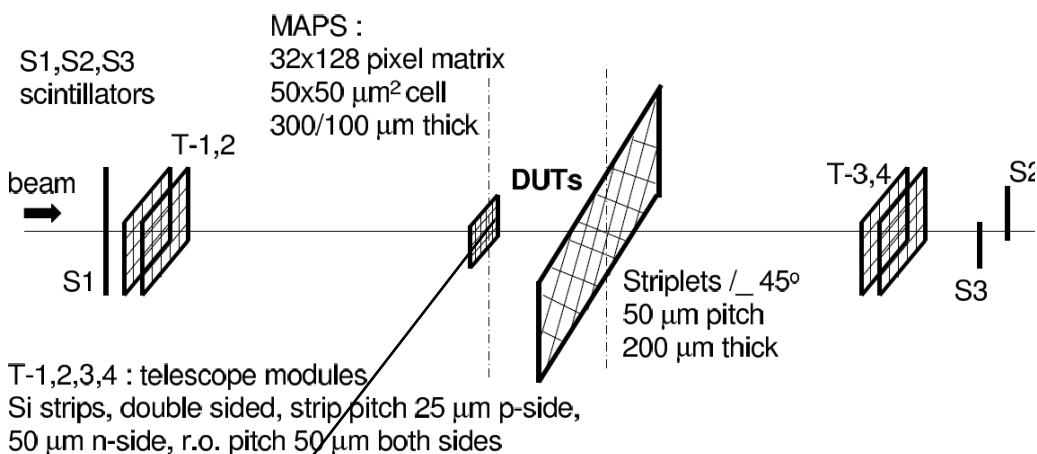
SuperPix0 layout – ST130nm
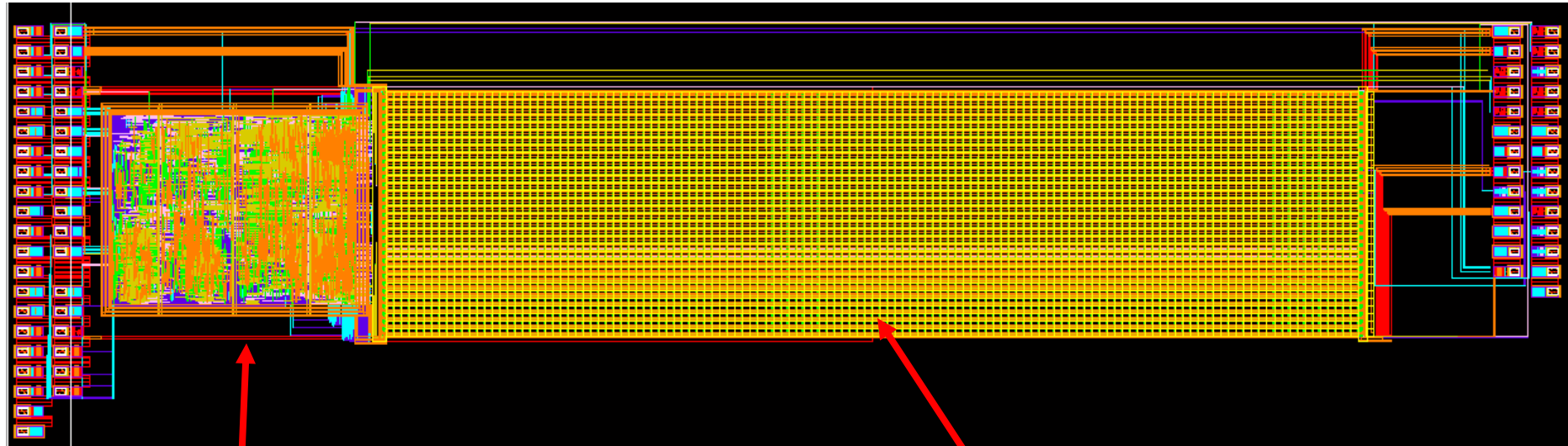
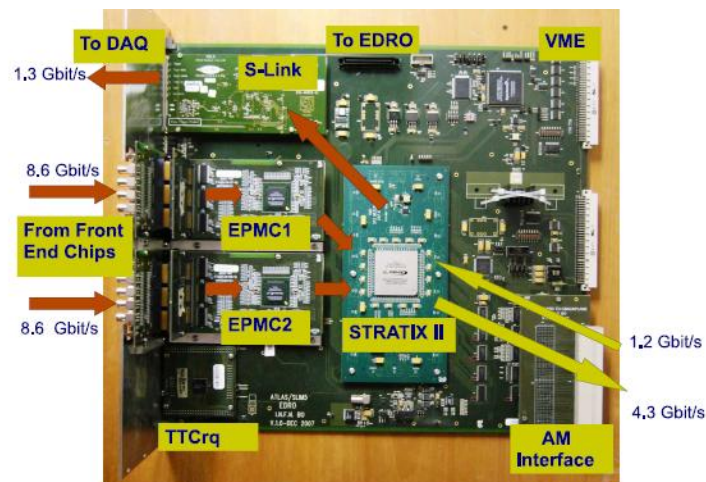Readout • TOT 58 636 logic cells
• Area < 2 mm²

Pixel matrix 128x32
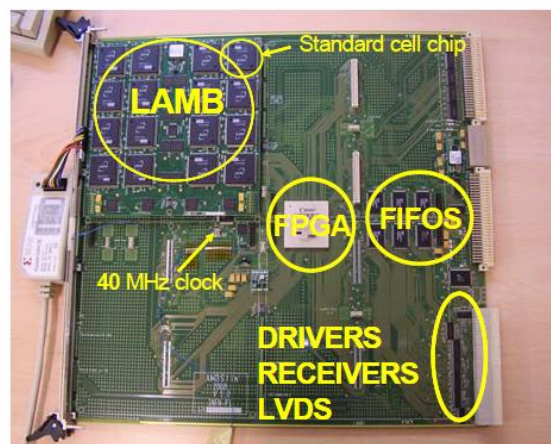Area ~ 10 mm²

Application on a DAQ chain

For the **SLIM5 collaboration** a similar readout architecture was implemented within a MAPS sensor chip. It has been tested with a silicon strip telescope and a powerful DAQ system during a test beam in 2008

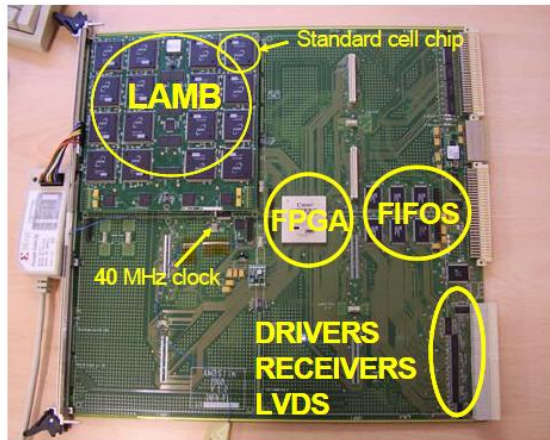DAQ board VME9U

APSEL4D

Associative Memory Board
For pattern trigger

Application on a DAQ chain

Associative Memory Board
For pattern trigger

Trigger on track pattern recognition

AM trigger latency < 1 us
Trigger Type:
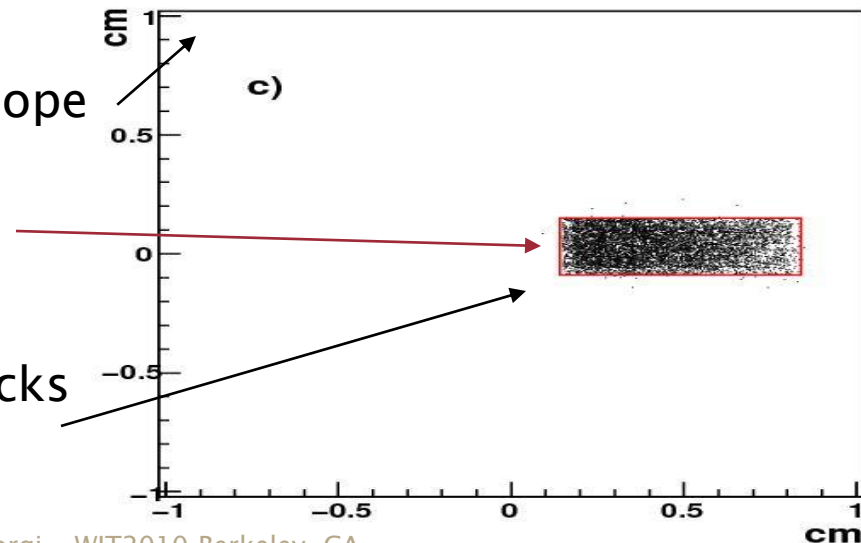• Hit molteplicity
• Track molteplicity
• Zone trigger

One given Surface in-between telescope

Trigger imposed on tracks crossing this
delimited area

Offline reconstructed tracks
on this surface

Conclusions

- Development under challenging target conditions
- Optimization of the architecture in several directions:
  - High speed: 100 Mhit/cm^2 rate, processed 50 Gpxl/s.
  - High efficiency: 98-99%.
  - Low bandwidth cost per chip: clusters optimization and time-wise scan halves down the bandwidth.
- Demonstrator submitted Sept. 2009 …awaiting for silicon.

Thanks for your attention

Filippo Giorgi
INFN Bologna (Italy)
giorgi@bo.infn.it

Backups

Study on Barrel optimal Depth:

B2

Barrel efficiency vs input rate

B rate/ A rate

Forbidden region
Mean input rate > ouput throughput

Barrel depth
- 2
- 4
- 8
- 16
- 32
- 64
- 128

Barrel inefficiencies due to fluctuations over the max throughput

Zone rate on Spars Input (Mzone/s)

A rate

Expected rate @**B2**: 8,2 MPxl/s

Expected rate @**B1**: 32,8 MPxl/s

Barrel clock 40 MHz

Study on Barrel optimal Depth:

A → [B2] → B

Barrel efficiency vs input rate

B rate/ A rate

Forbidden region
Mean input rate > ouput throughput

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- 4
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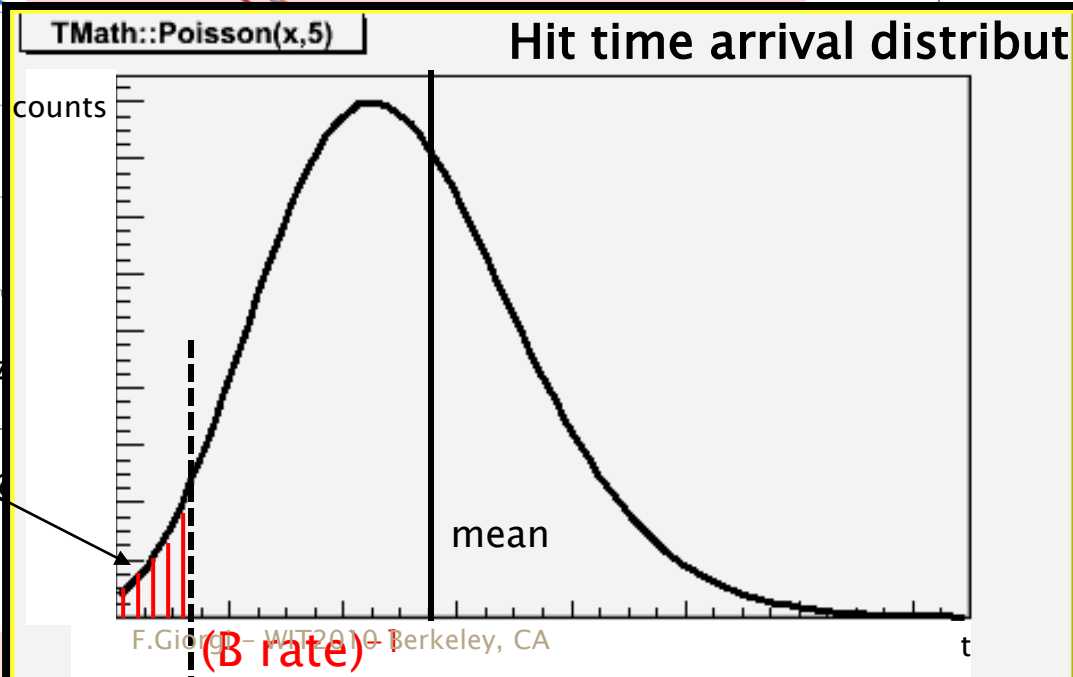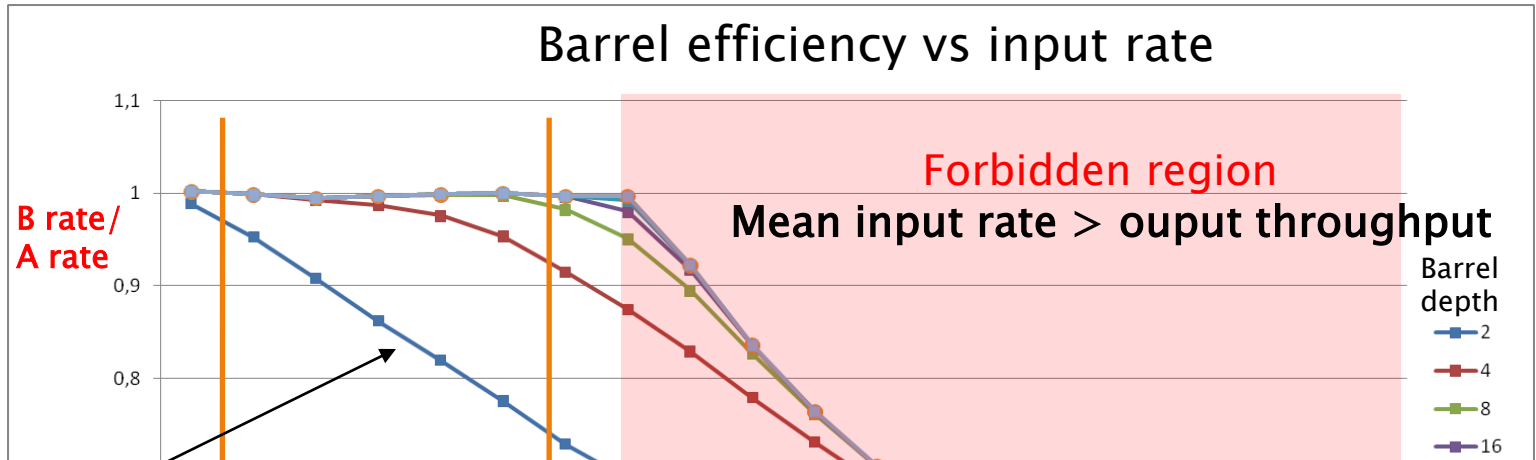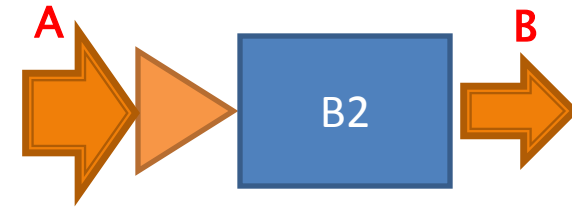
Barrel inefficiencies due to fluctuations over the max throughput

Expected rate @**B2**:
8,2 MPxl/s

Expected rate @
32,8 MPxl/s

Hit time arrival distributi

TMath::Poisson(x,5)

counts

mean

(B rate)

t

The Slow Control bus: I²C-like system

Hard Wired Addresses

001 010 011 100 101 110

slave slave slave slave slave slave

VDD

DAQ BUS master

SDA
SCL
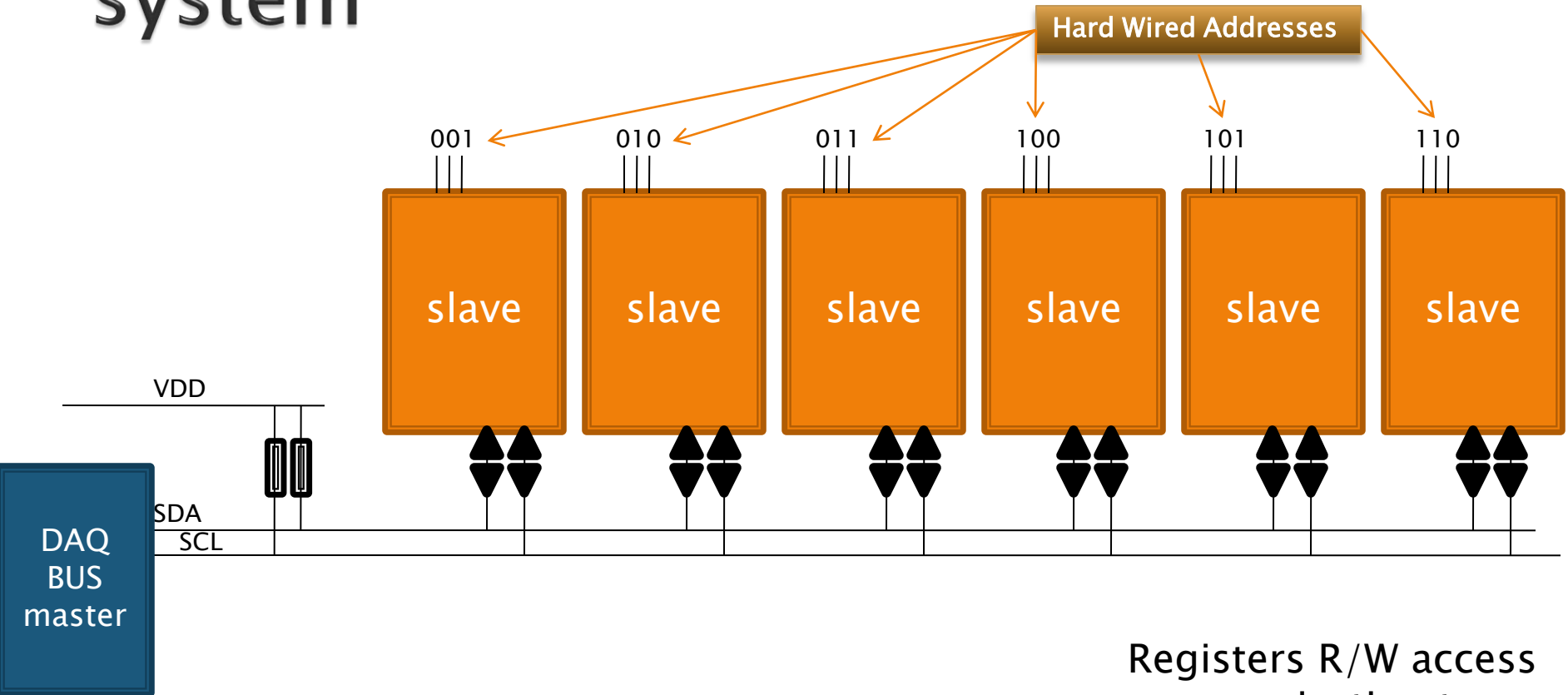
Registers R/W access communication type

I²C : two bidirectional open-drain lines.
• Serial Data (SDA)
• Serial Clock (SCL), pulled up with resistors.

Slow Control

- 1 Set of Read/Write registers
  - ◦ Chip settings
  - ◦ MP masks
- 1 set of Read Only registers
  - ◦ Acquisition flags
  - ◦ Rate counters
  - ◦ Error flags

Sub–matrix readout Efficiency table
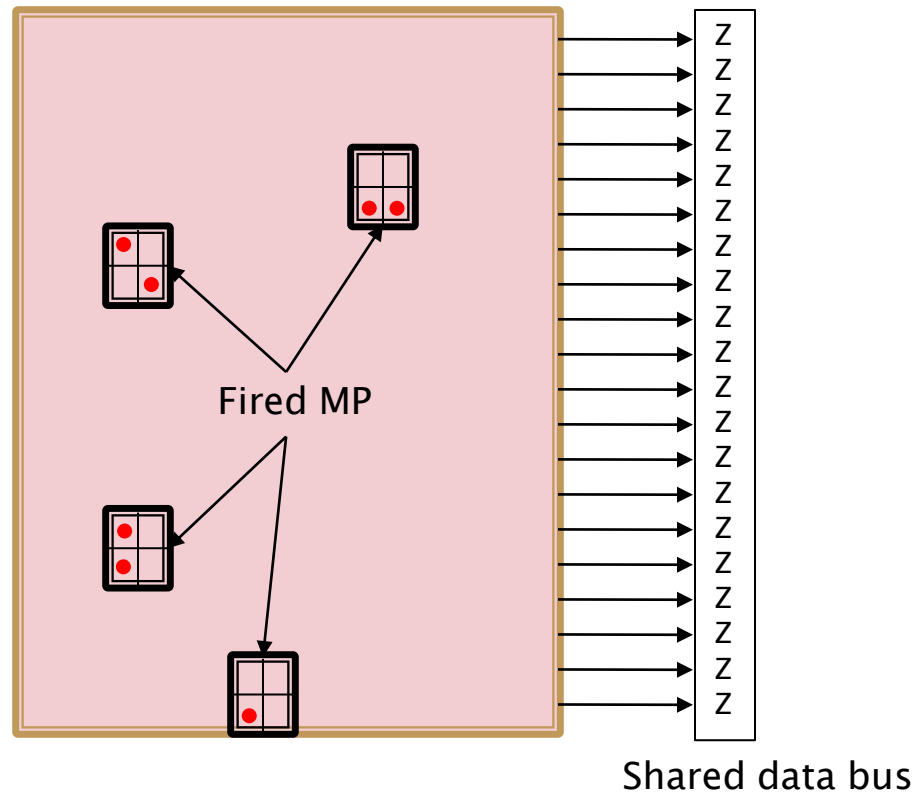
Hit rate 100 MHz/cm²

RN	sim DURATION (us)	RDclk (MHz)	BCO (us)	Mean Sweeping time (us)	global hit rate (MHz)	rate on area (MHz/mm2)	B2 depth	B1 depth	Scan buffer overflow	Already hit effi (%)	Frozen MP effi (%)	Overflow effi B2 (%)	Overflow effi B1 (%)
107	1	60	0,5	0,45	33,8	1.03	8	32	0	99,96	98,90	100	100
108	1	80	0,5	0,34	33,8	1.03	8	32	0	99,95	99,39	100	100
109	1	100	0,5	0,27	33,8	1.03	8	32	0	99,96	99,53	100	100
110	1	60	1	0,75	33,8	1.03	8	32	0	99,91	98,83	100	100
111	1	80	1	0,56	33,8	1.03	8	32	0	99,91	99,10	100	100
112	1	100	1	0,45	33,8	1.03	8	32	0	99,91	99,25	100	100
113	1	60	1,5	0,95	33,8	1.03	8	32	0	99,86	98,78	100	100
114	1	80	1,5	0,71	33,8	1.03	8	32	0	99,86	99,05	100	100
115	1	100	1,5	0,57	33,8	1.03	8	32	0	99,86	99,23	100	100
116	1	60	2	1,08	33,8	1.03	8	32	0	99,84	98,42	100	100
117	1	80	2	0,81	33,8	1.03	8	32	0	99,83	98,81	100	100
118	1	100	2	0,65	33,8	1.03	8	32	0	99,83	99,04	100	100

SIMULATIONS: the infrastructure

- ▸ Realistic VHDL model of a Sub-matrix for behavioral simulation.
  - ◦ 2D array of MP entities, each one with uniform random hit generation. User-defined hit rate.
  - ◦ NO pixel dead time taken into account. (pixel immediately reset after read)
- ▸ VHDL test bench
  - ◦ Integrated data integrity check.
  - ◦ Efficiencies evaluation.
  - ◦ File logs
    - • Simulation runs e-log (storing the whole parameter set for each simulation)
    - • Frozen hit log (once a MP gets frozen, the fired pixels within are stored in absolute x-y format)
    - • B2 Readout log (stores the hits read out from any of the B2 decoded in absolute x-y format)
    - • B1 Readout log (stores the hits read out from B1 decoded in absolute x-y format)
    - • Output log (stores the hit read out from the final output stage decoded in absolute x-y format)
- ▸ Hit controller program: a C++ tool that checks the correspondence between the frozen hit log and output log.
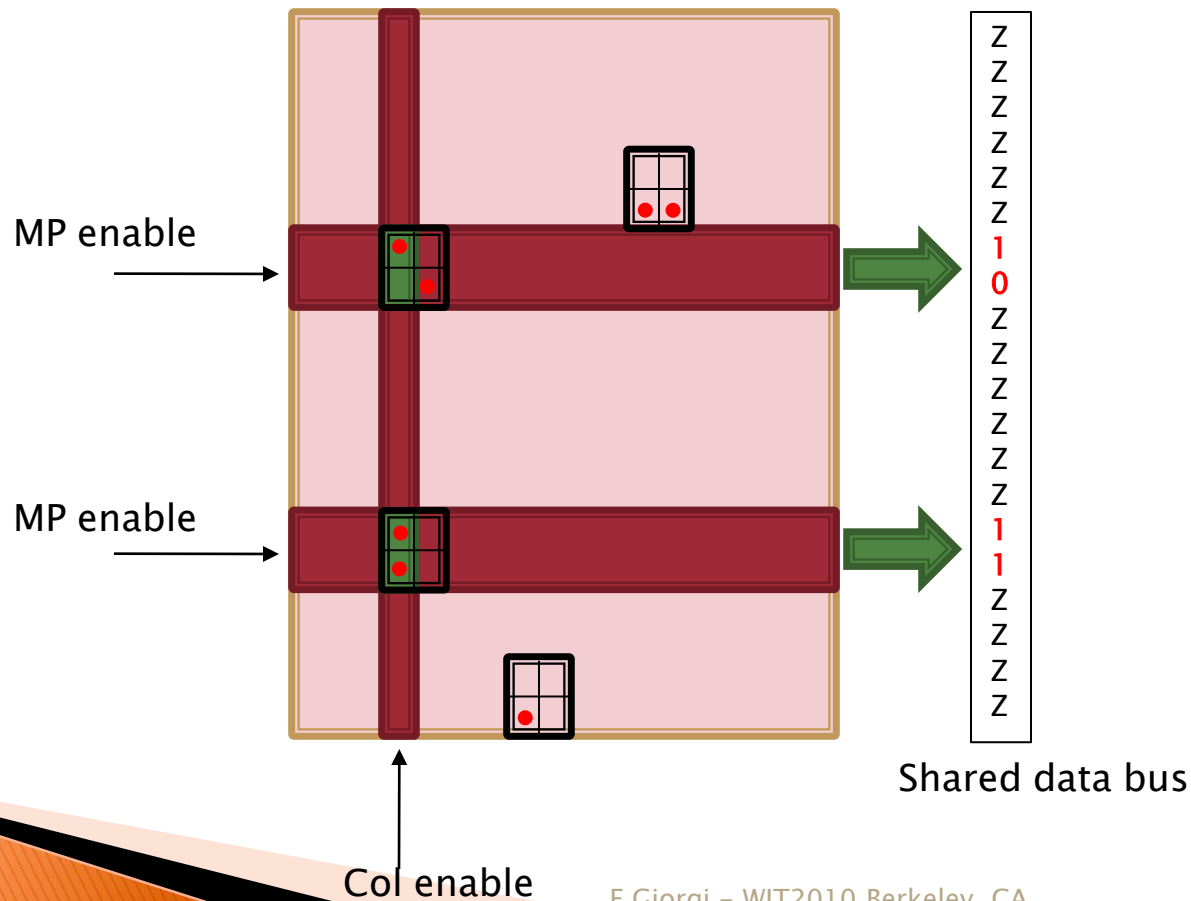
Matrix overview (2)

- Pixels grouped into **Macro Pixels:**
  - ◦ Minimum entities addressable by readout logic
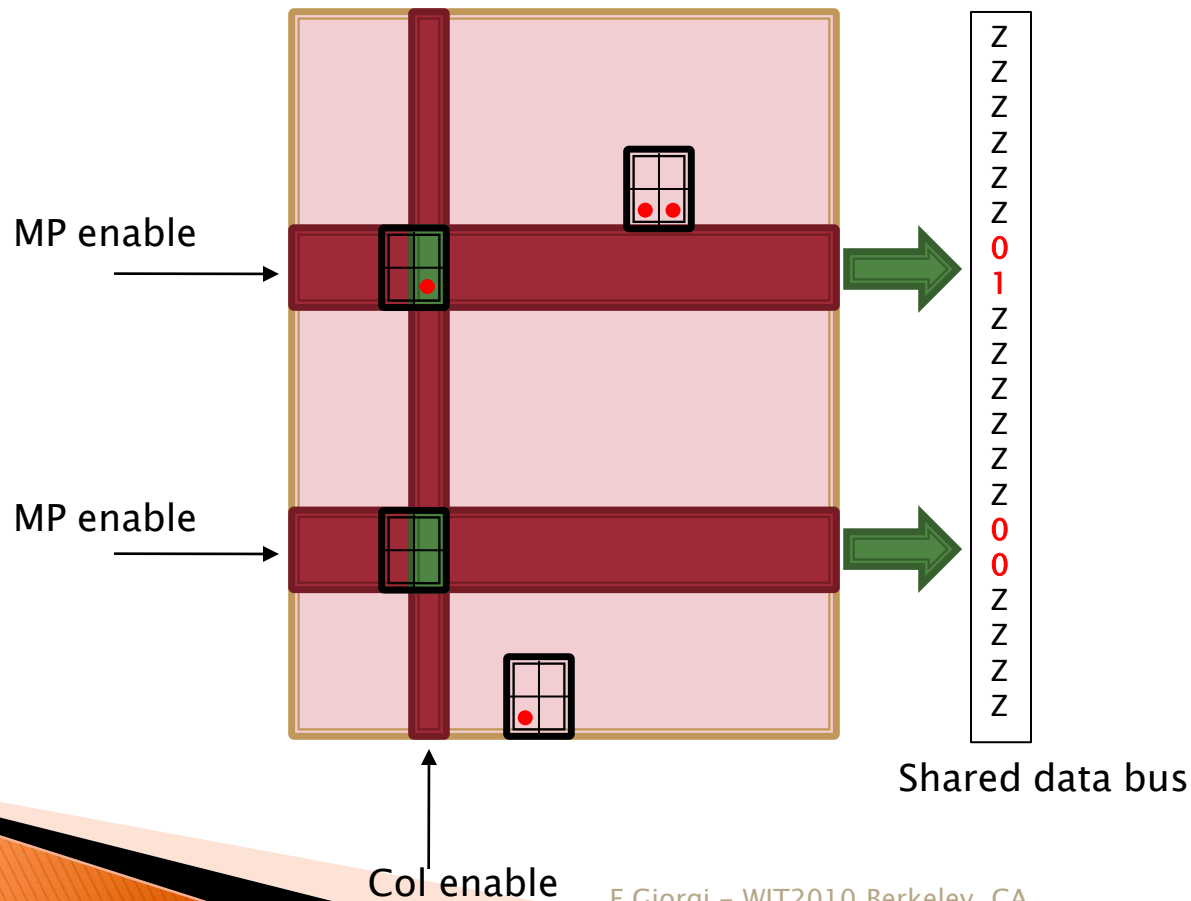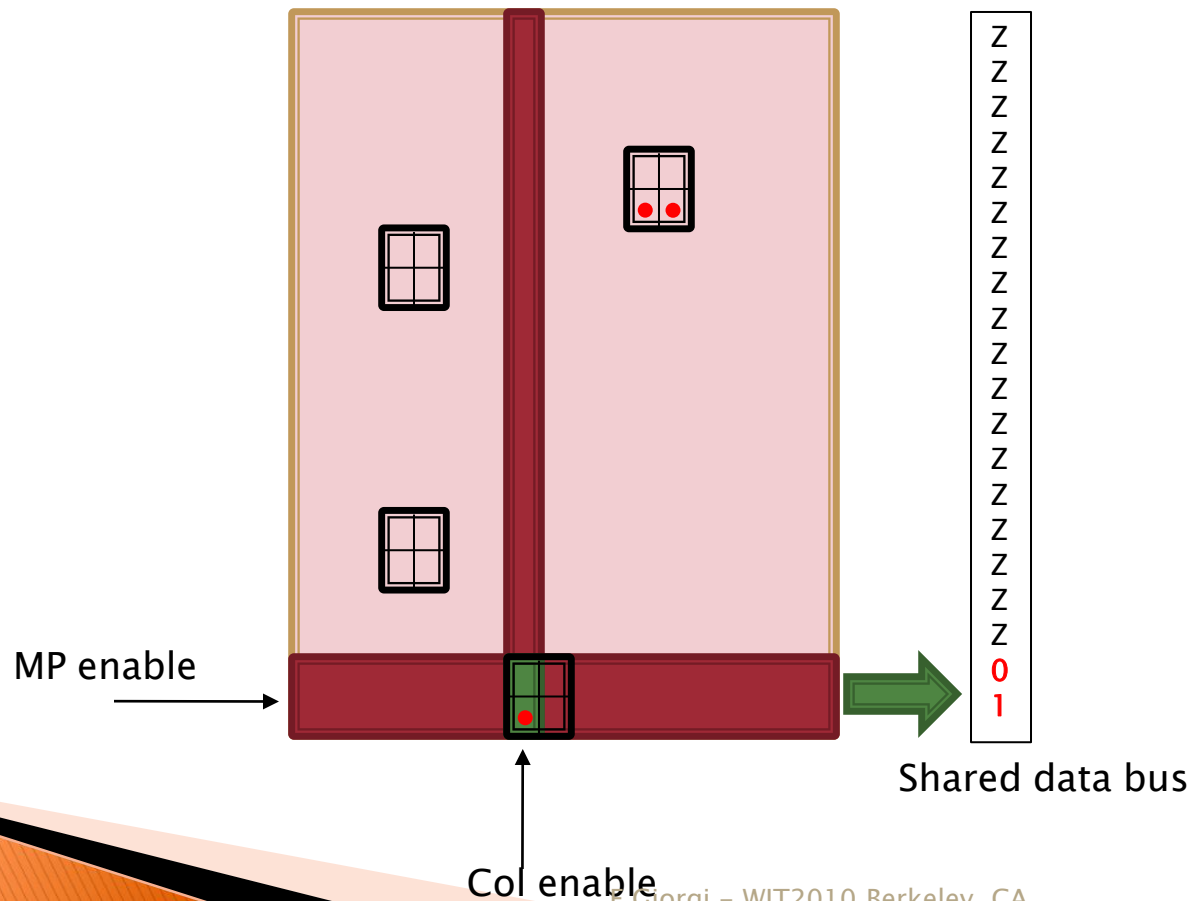 - ◦ Minimum entities for time tagging

Fired MP

Shared data bus

Matrix overview (2)

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  - ◦ Minimum entities for time tagging
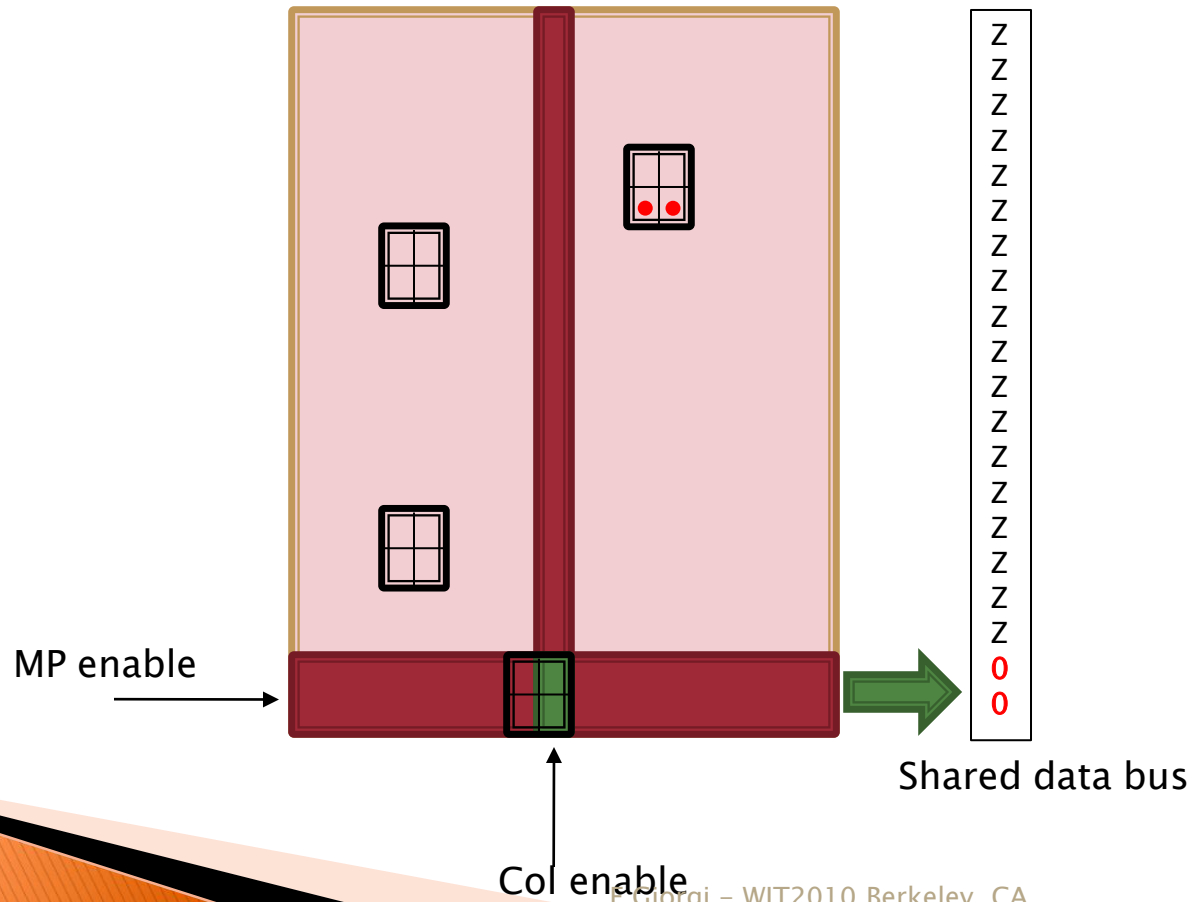

MP enable

MP enable

Col enable

Shared data bus

Matrix overview (2)

- Pixels grouped into **Macro Pixels:**
  - Minimum entities addressable by readout logic
  - Minimum entities for time tagging

MP enable

MP enable

Col enable

Shared data bus

Z
Z
Z
Z
Z
Z
Z
0
1
Z
Z
Z
Z
Z
Z
Z
0
0
Z
Z
Z
Z
Z

Matrix overview (2)

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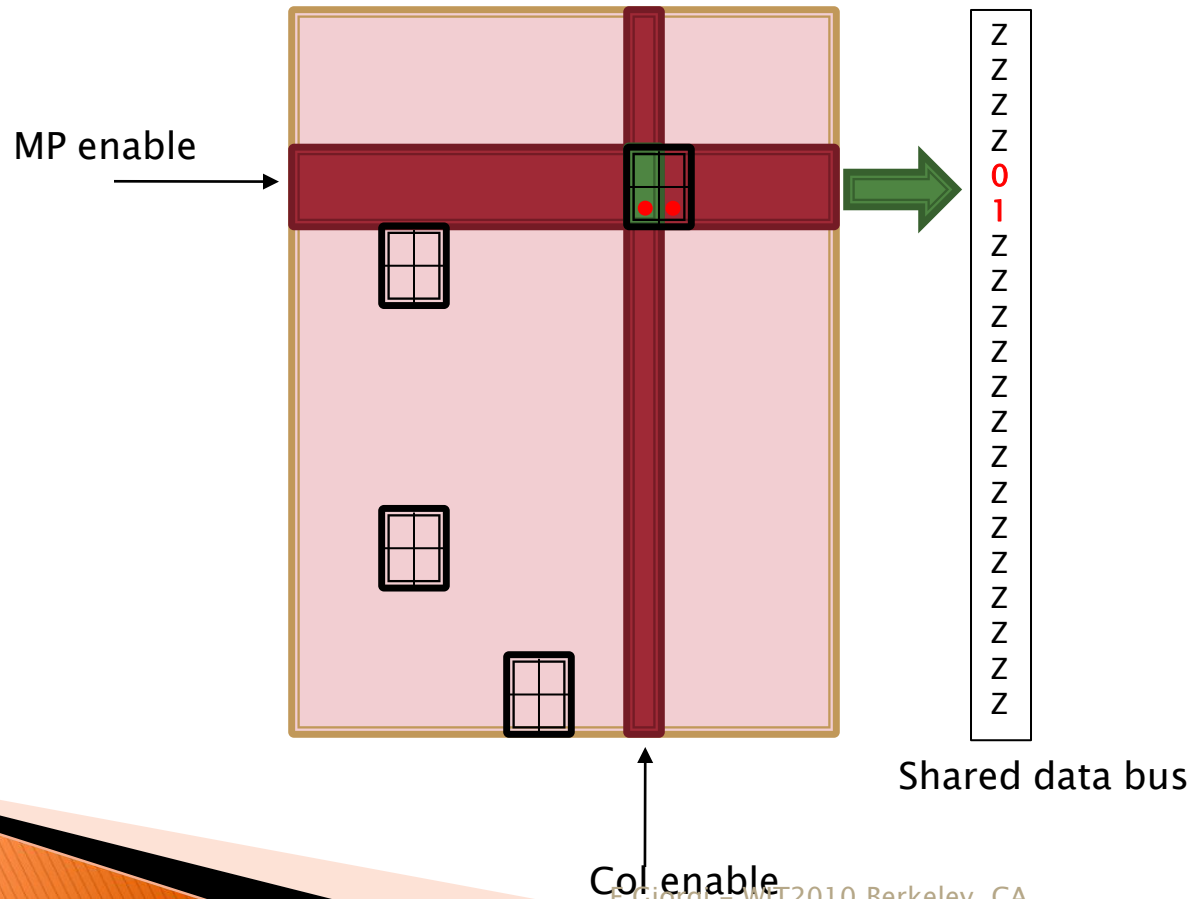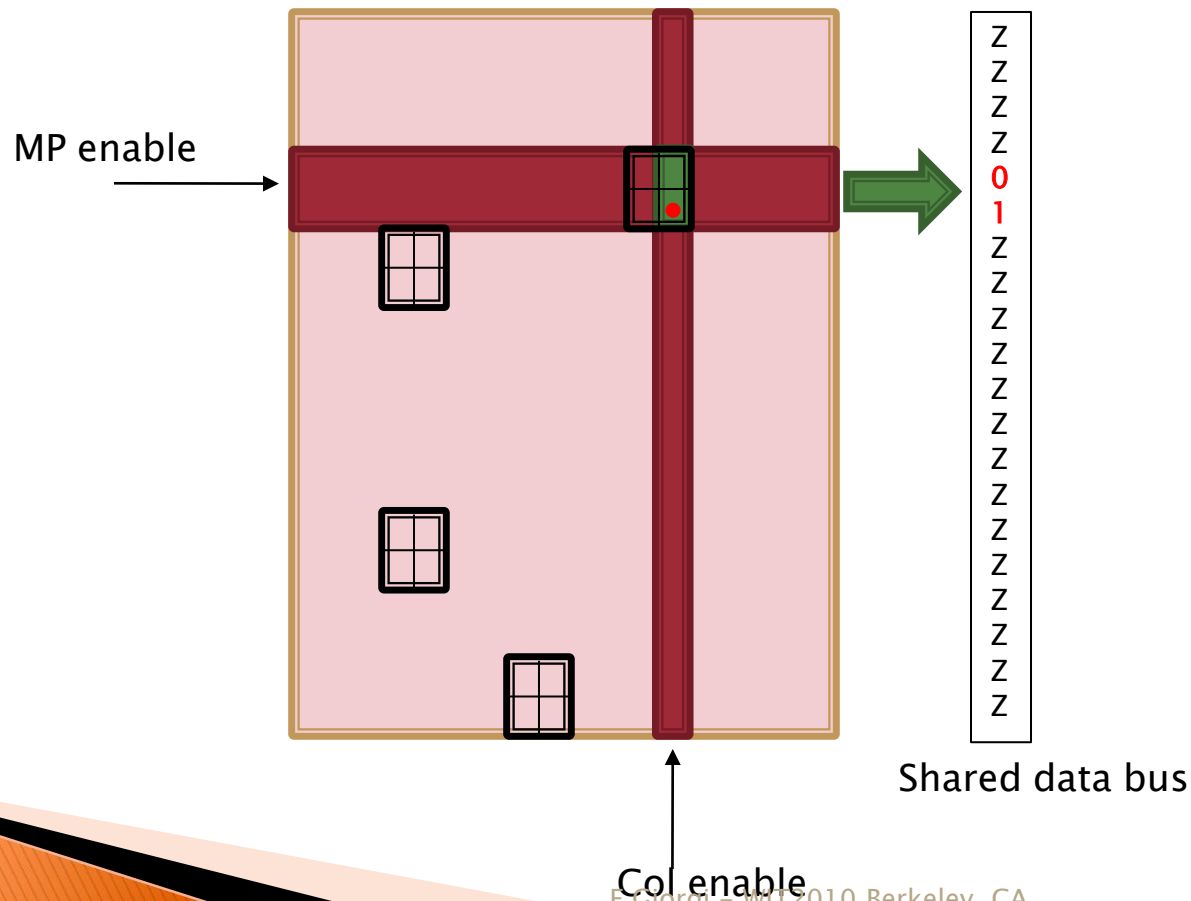

MP enable

Col enable

Shared data bus

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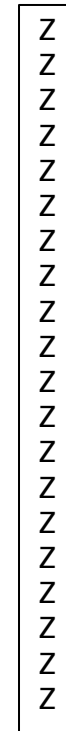

MP enable

Col enable

Shared data bus

Matrix overview (2)

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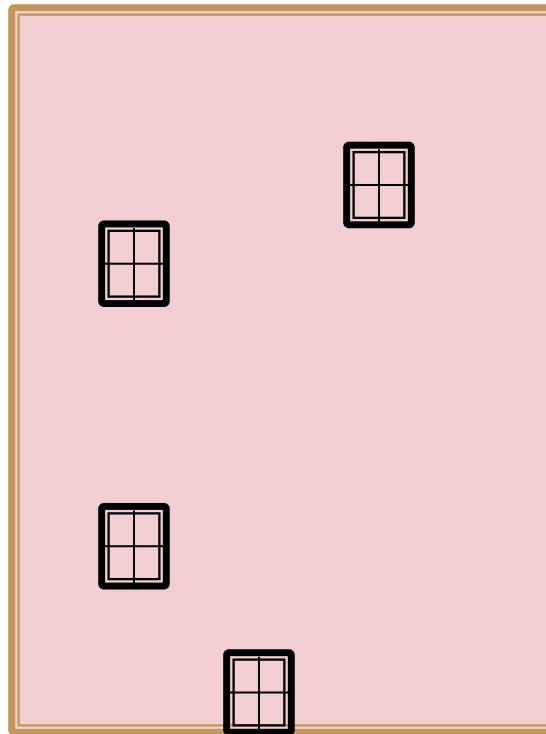

MP enable

Col enable

Shared data bus

Matrix overview (2)

▸ Pixels grouped into **Macro Pixels:**
  ◦ Minimum entities addressable by readout logic
  ◦ Minimum entities for time tagging

Shared data bus

Components synthesis

Components	Flip Flop registers	Logic gates
B2	~140	~1400
B1	~1000	~6700
Concentrator	~230	~1000
Concentrator out	~120	~370
I2C interface	~130	~600
Mask register	~520	~2300
Scan buffer	~4700	~9600
Register file	~1000	~2700
Sparsifier	~160	~1000
Sweeper	~7200	~16200