
System Concepts for Doublet Tracking Layers

Presented by Carl Haber

Lawrence Berkeley National Lab

with M.Garcia-Sciveres, M.Gilchriese, B.Heinemann, T.Mueller,
and many colleagues in the international ATLAS silicon strip
stave upgrade community

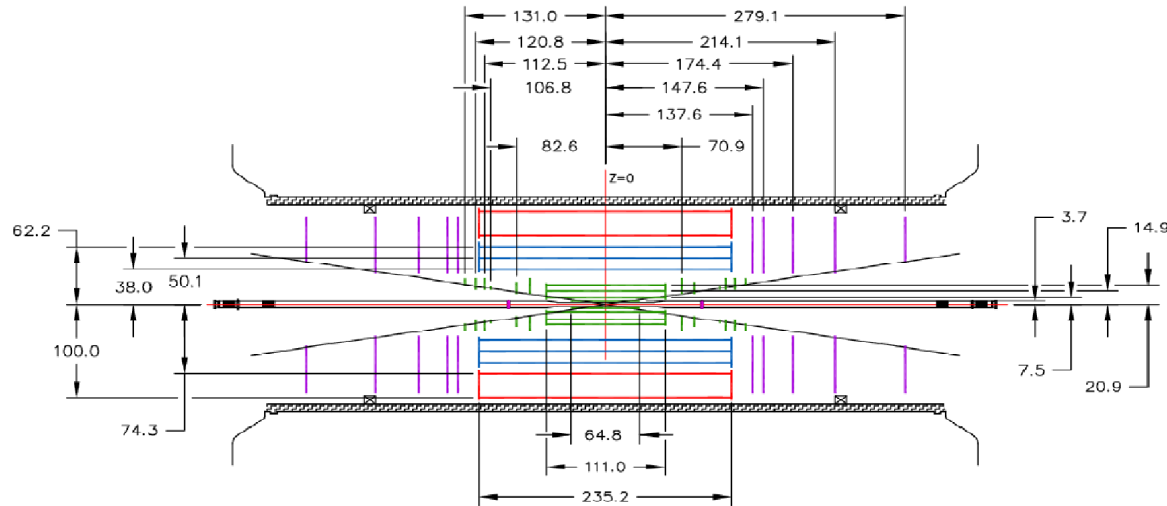
Outline

- Introduction
- Layout
- The present stave design and features
- Assumptions/Issues
- Trigger rate study
- A trigger stave concept and implications

Introduction

- Over the past 4-5 years ATLAS has carried out an R&D program to develop a tracker for the super-LHC
- Many critical aspects and technologies have been addressed – layout, mechanics, mass, cooling, sensors, electronics, DAQ, assembly
- The tracker is designed around two-sided integrated multi-modular “stave” and “petal” elements.
- A stave or a petal is a natural doublet structure and could also be a basis for a local trigger
- Here we consider the implications of, and for, this design, on a local doublet based tracker trigger

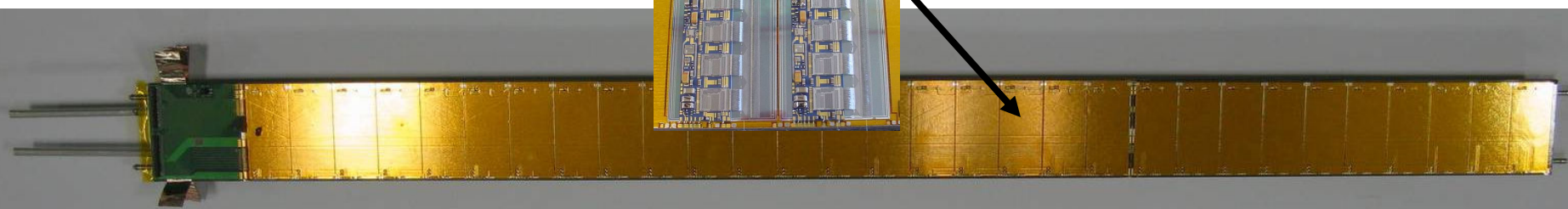
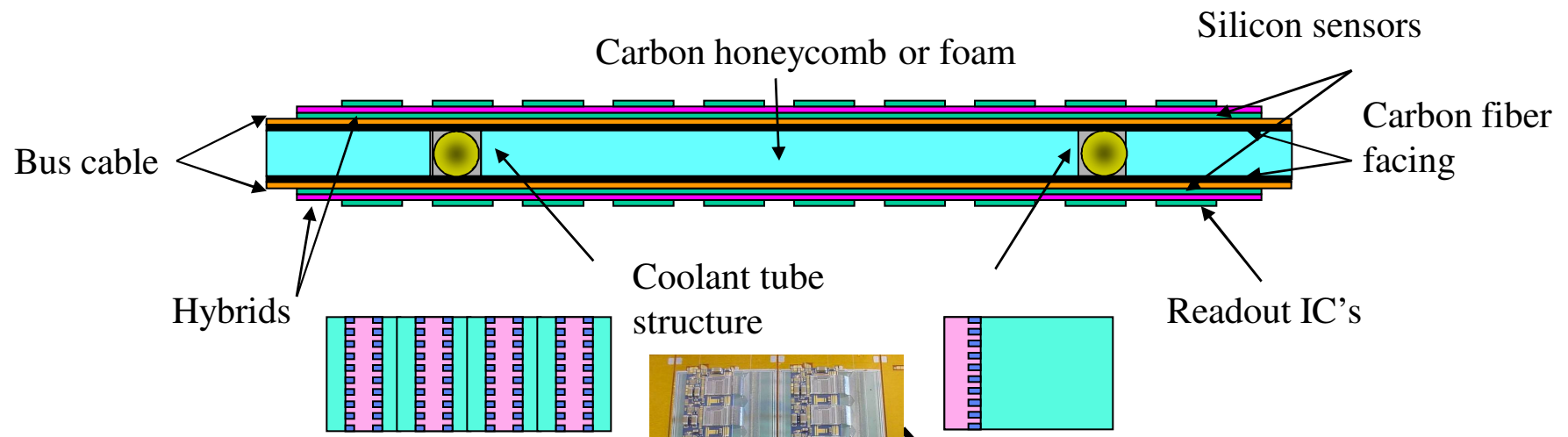
Current s-LHC Tracker Layout



- 5 double sided barrel layers
 - Inner layers: 3 of 2.5 cm = short strips
 - Outer layers 2 of 10 cm = long strips
- 5 double sided disk layers
- Basic substructure is a “stave” or “petal” being a highly integrated electrical/mechanical/thermal element holding many “modules”

Stave Concept

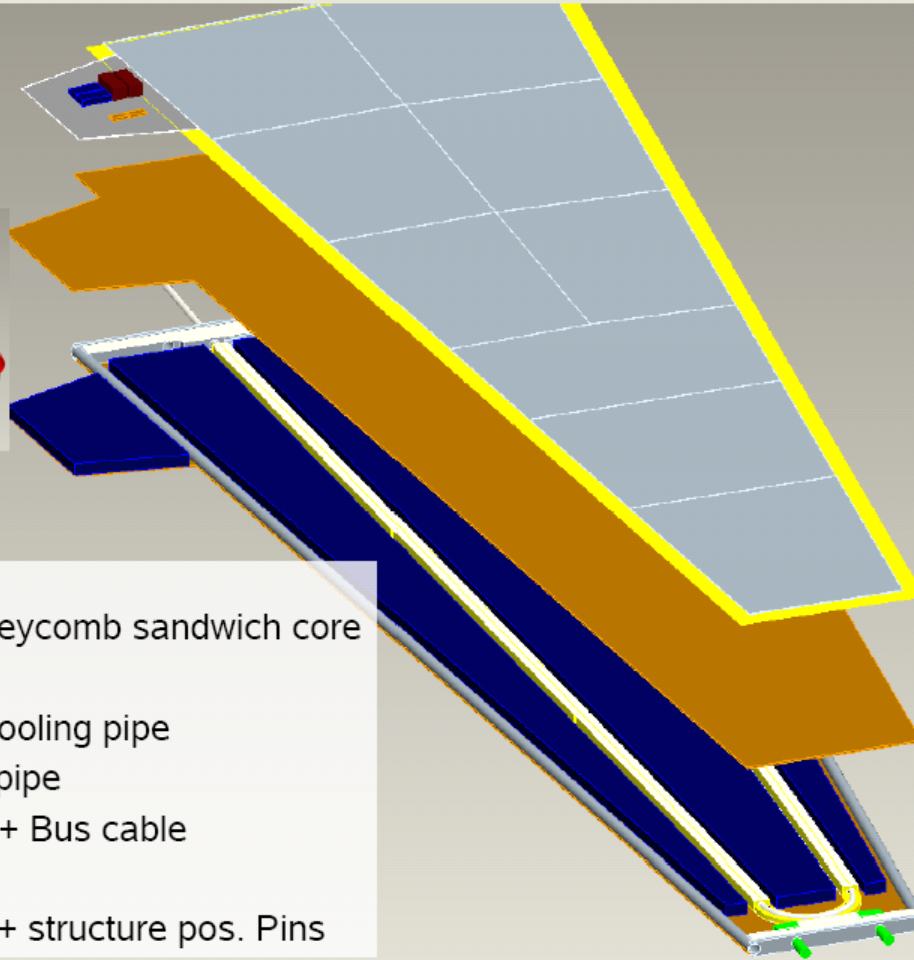
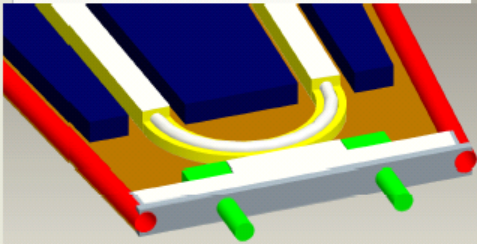
- Approximate dimensions
 - Short- (~2.5 cm), Long-strips (~10 cm): length 1.2 m, width ~ 11 cm
 - Thickness ~ 3-5 mm
- Laminate of core, electrical bus, sensors, hybrids, chips
- Mass 2.26 (1.73)% X0 (34% core, 66% electrical+sensors)



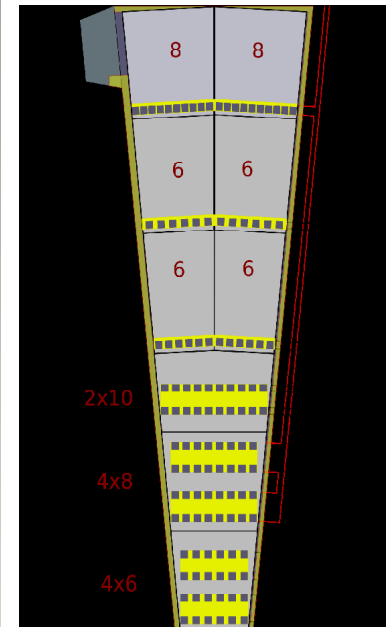
Forward Petals

The petal concept

- ✓ Follows quite closely the barrel stave concept



- ✓ 2 Carbon Facings + Honeycomb sandwich core
- ✓ CF tubes on sides
- ✓ Independent SS - CO₂ cooling pipe
- ✓ POCOFoam around SS pipe
- ✓ Independent e- services + Bus cable
- ✓ Control card on side
- ✓ Top-bottom Al closeouts + structure pos. Pins



ATUW 2008, NIKHEF

Carlos Lacasta

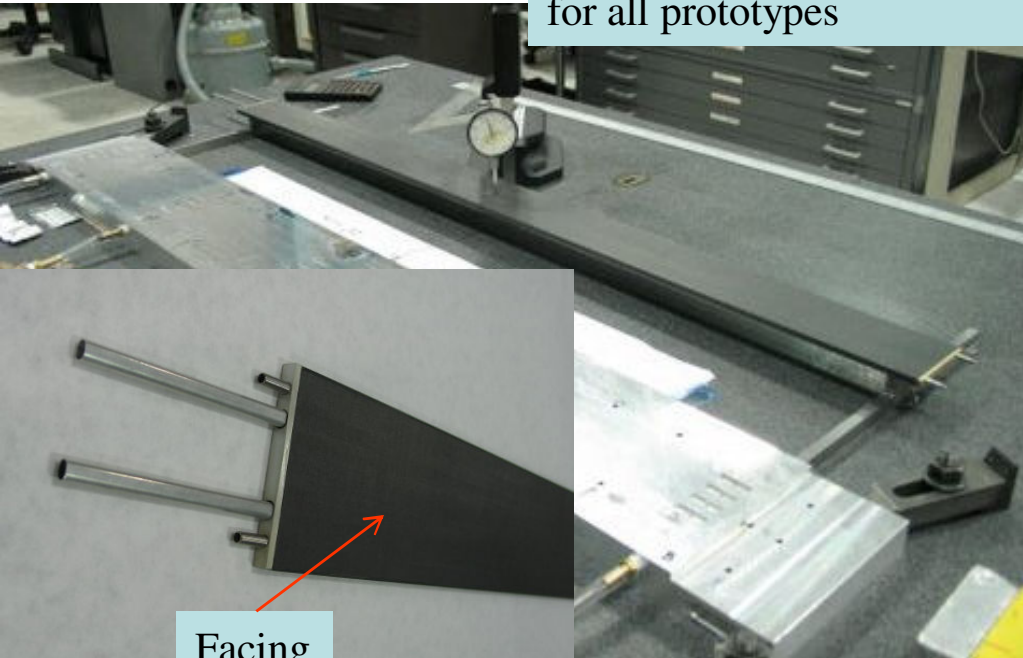
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Elements of Stave/Petal Technology

- Low mass thermo-mechanical cores
 - Assembly and materials
 - Measurement
 - Simulation
- Embedded electrical services
- Distributed multi-drop LVDS transmission
- Alternate powering, control and protection
- Low mass, surface attached hybrids
- Fine pitch interconnections
- Multichannel Parallel DAQ and test systems

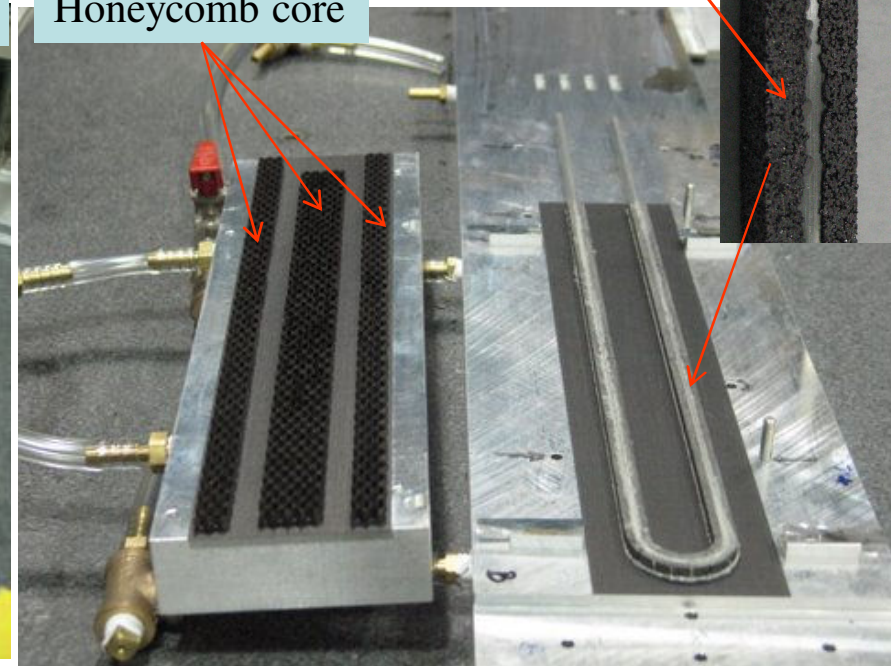
Core Construction

Honeycomb ~ 5 mm thick
for all prototypes

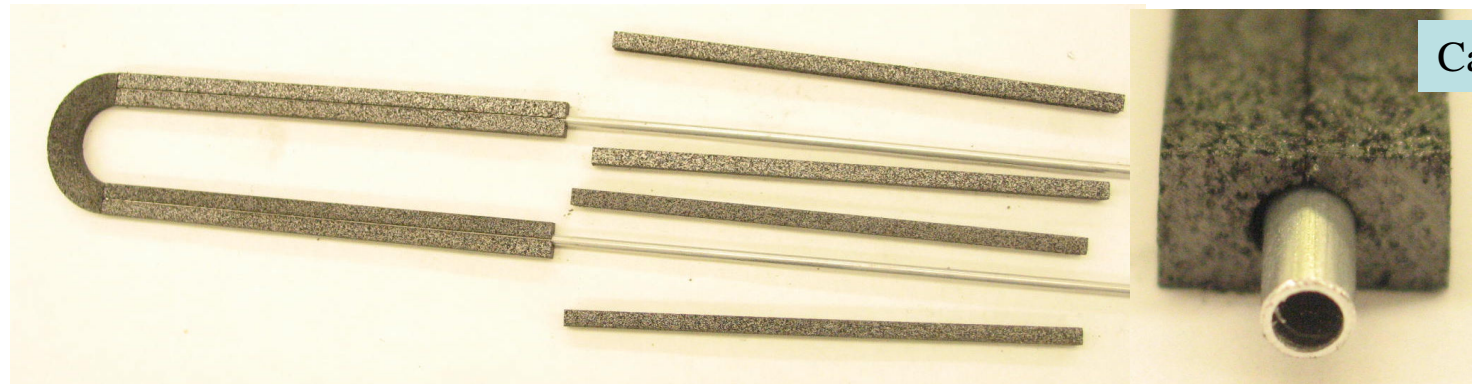


Facing

Honeycomb core

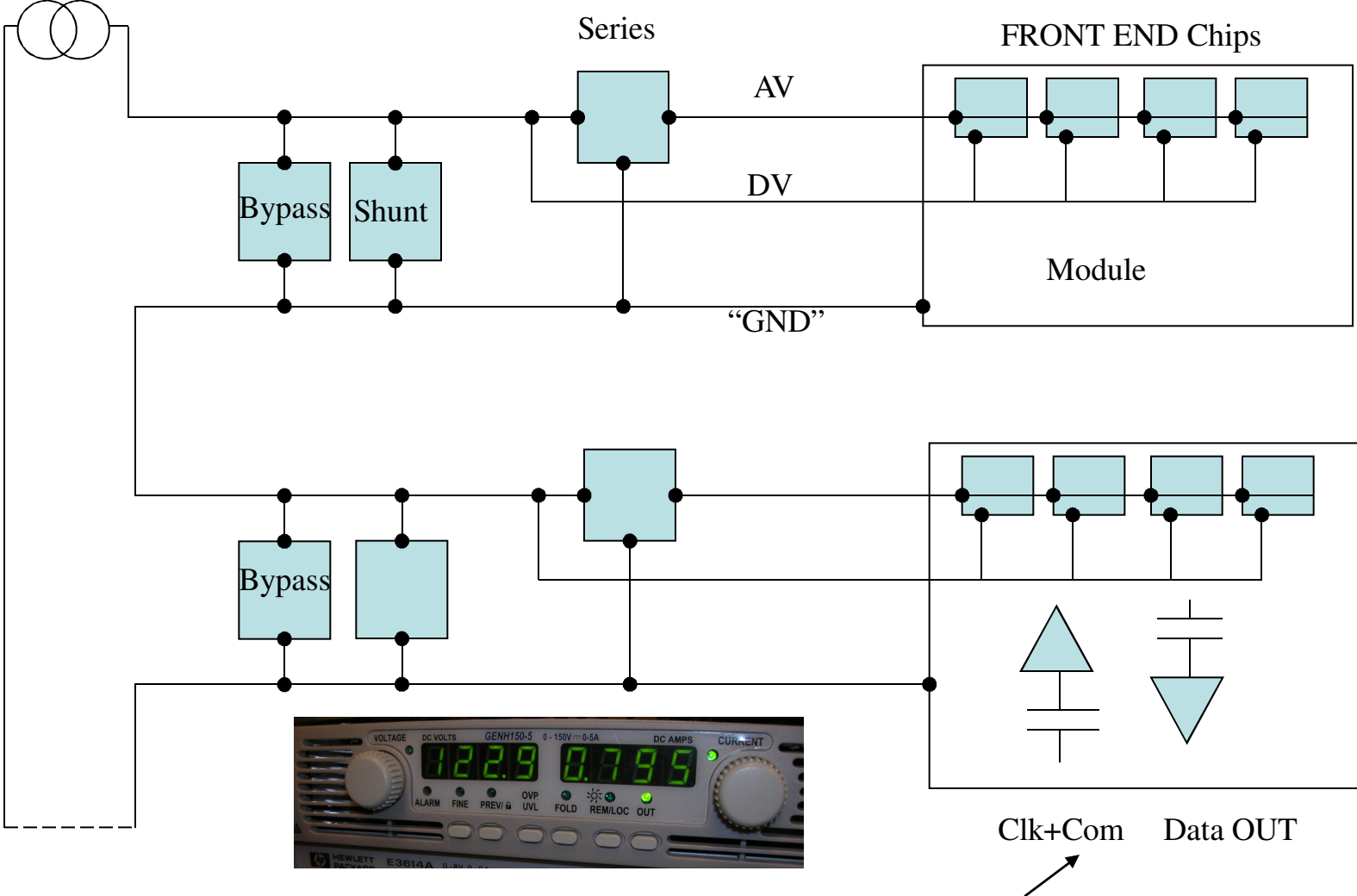


Carbon foam



Carbon foam

Serial Powering



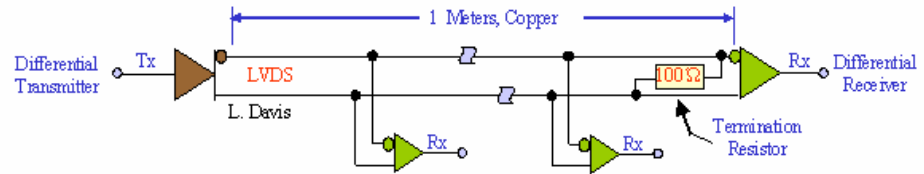
Requires AC coupled data and TTC



Embedded Bus Cables

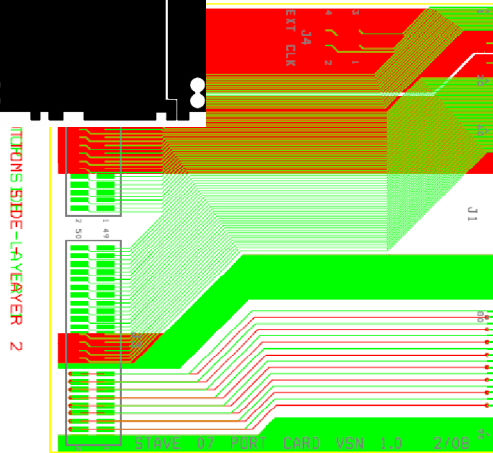


Al shield



Data readout: 1/hybrid

Clock & Command lines



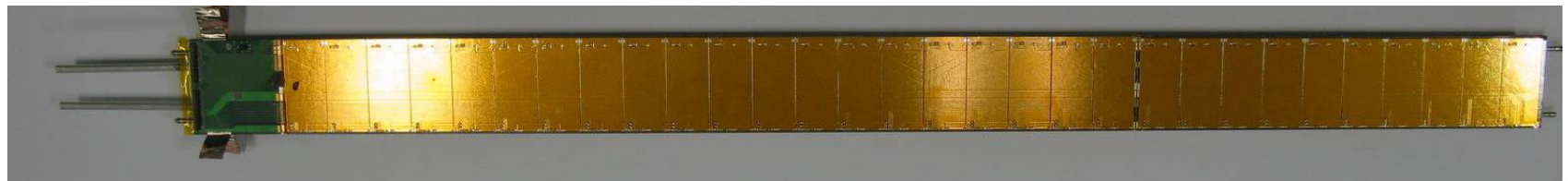
End of Stave Card



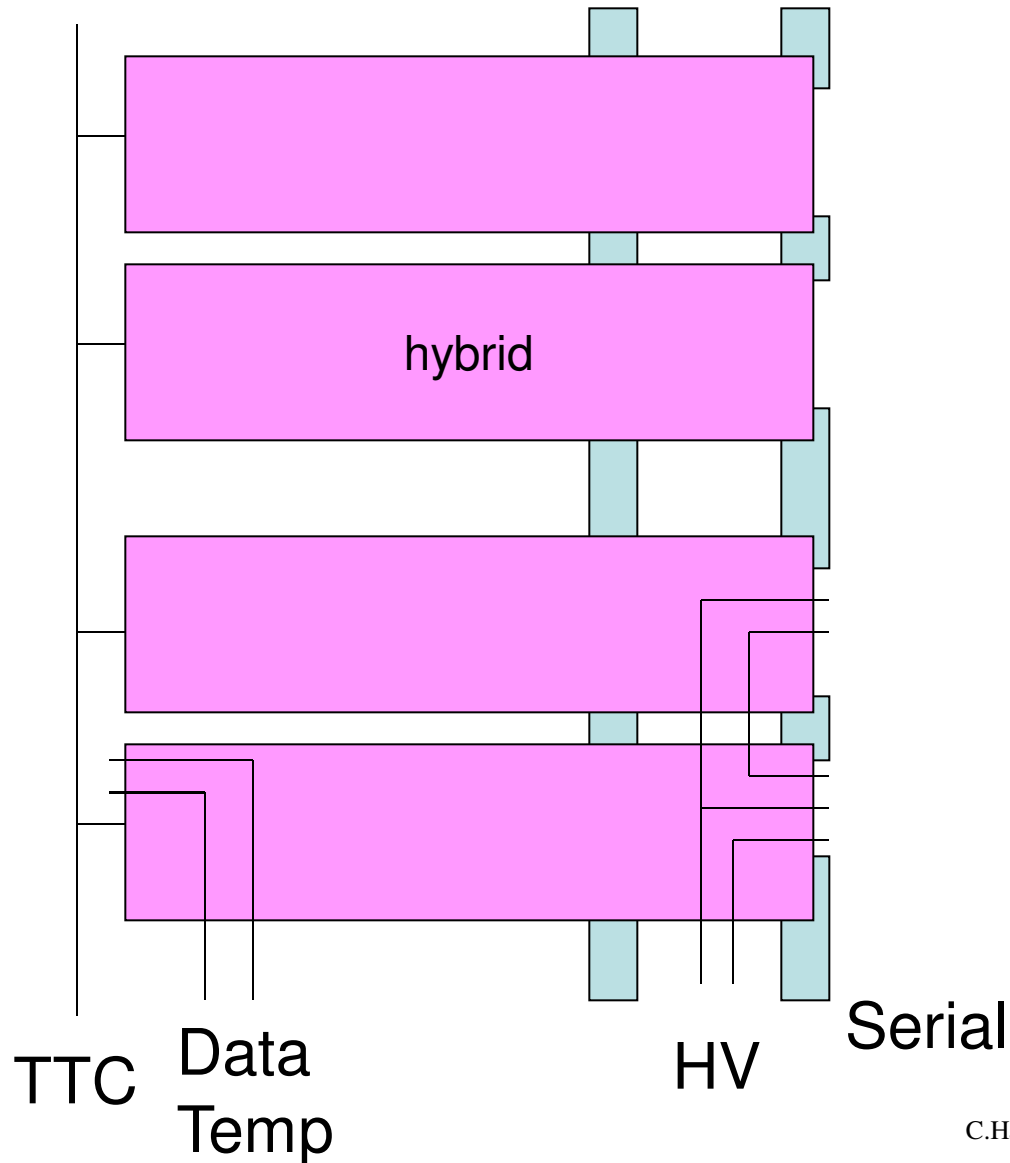
Serial current return

Serial current link

HV distribution

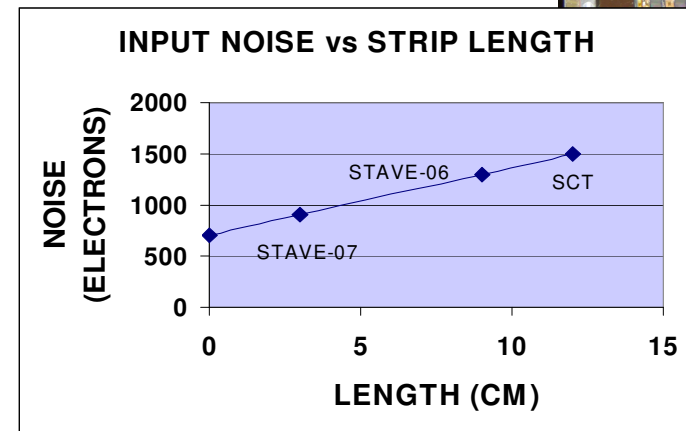
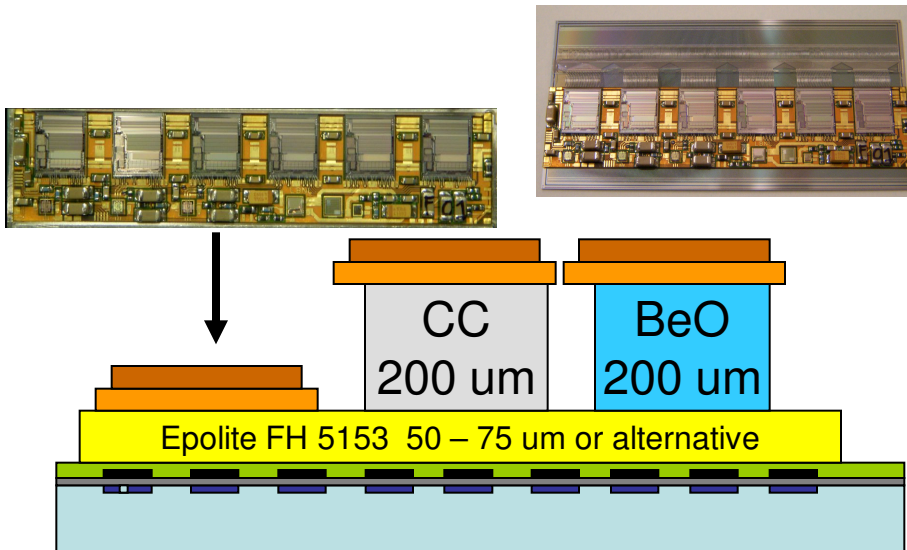
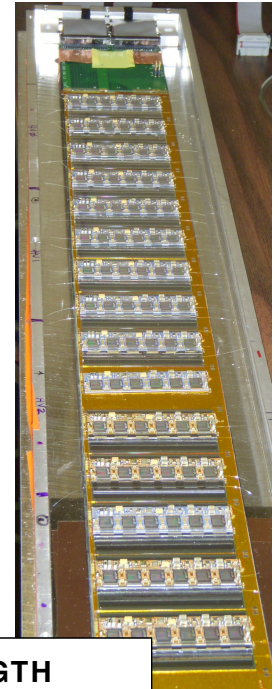
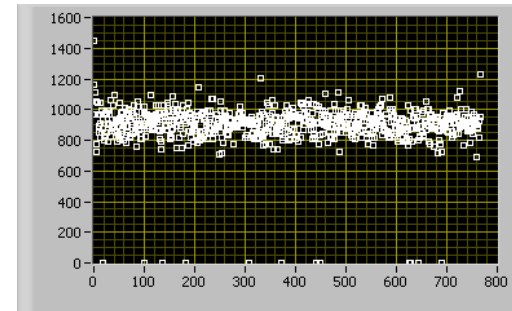
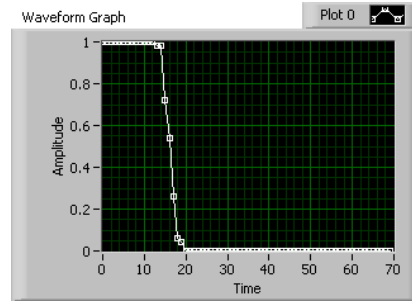


Wiring Geometry



Tests of Staves and Modules

- Electrical performance studies
 - Noise
 - Grounding, bias, and shielding
 - Signal propagation
- Module is serially powered, with AC coupled data and control
- Good noise and interference performance observed on stave
- Tested with a range of substrates, thicknesses, directly glued to sensor



Assumption and Issues

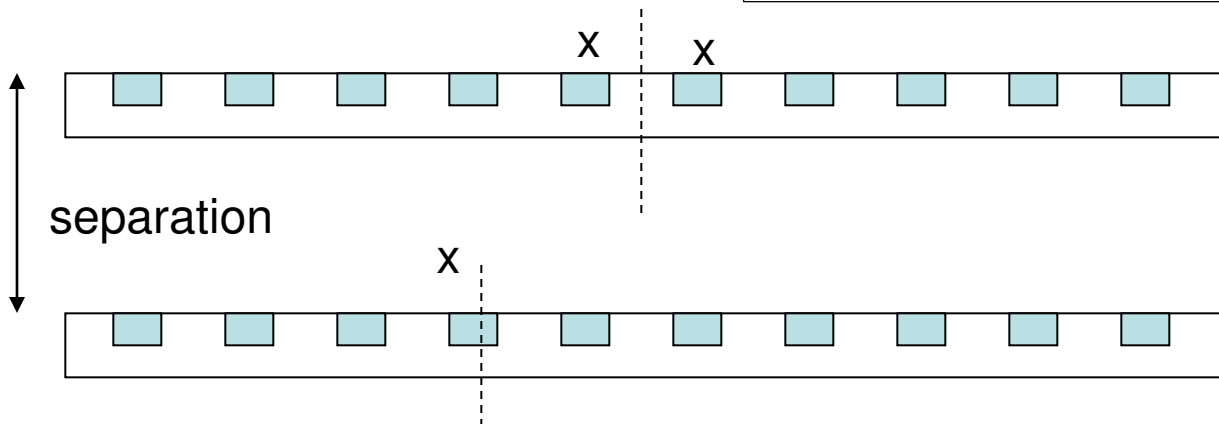
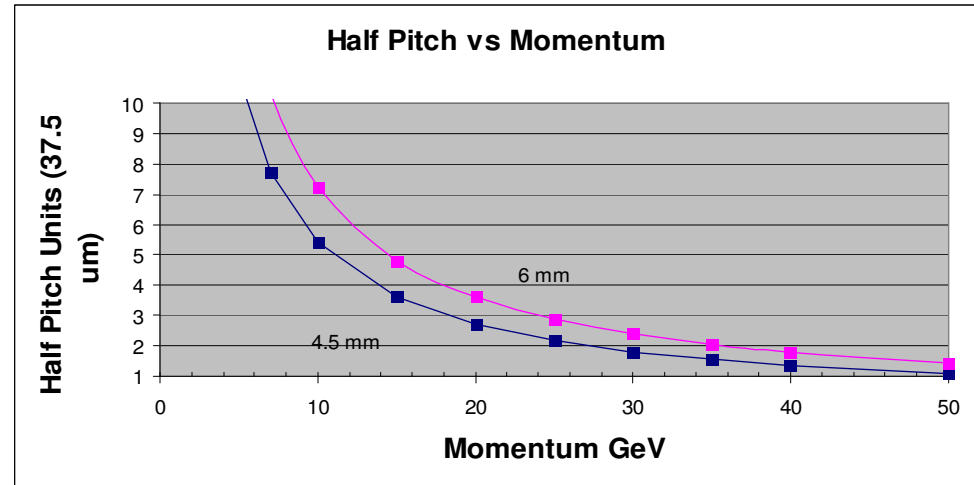
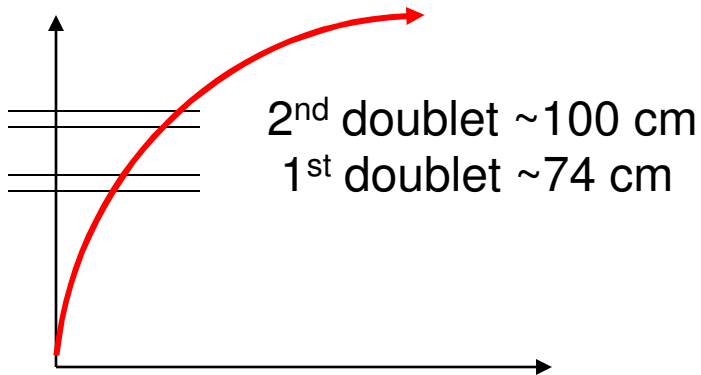
- Focus here is on doublet silicon strip tracking layers at large radius (70-100 cm) with local correlation circuits.
- Assume “long” strips (5-10 cm) with ~few mm radial separation
- Without a trigger system we currently have:
 - A minimal mass design
 - Each of 5 stave layers with axial/stereo sensors
 - 2.5/10 cm Z granularity well matched to the expected sLHC occupancy and the bandwidth of a practical frontend/data transmission system
 - A design meeting thermal requirements with direct cooling of the sensors.
 - Embedded digital data paths without undue interference and coupling.
 - Practical alternative powering designs (serial and DC/DC) which significantly reduce services
- What is the impact of a local doublet trigger and what can we retain?

Implications

- Is the 10 cm strip geometry sufficient?
- Is the trigger rate, real/fakes manageable?
- What is the impact on the readout bandwidth?
- Can we afford to lose axial/stereo layers in favor of axial/axial layers?
- How much mass is added?
- Are the interconnections practical?
- What are the electrical implications of sending fast hit data around for correlation?
- What is the effect on cooling and thermal performance?

Basic Concept

Simple calculation at 100 cm

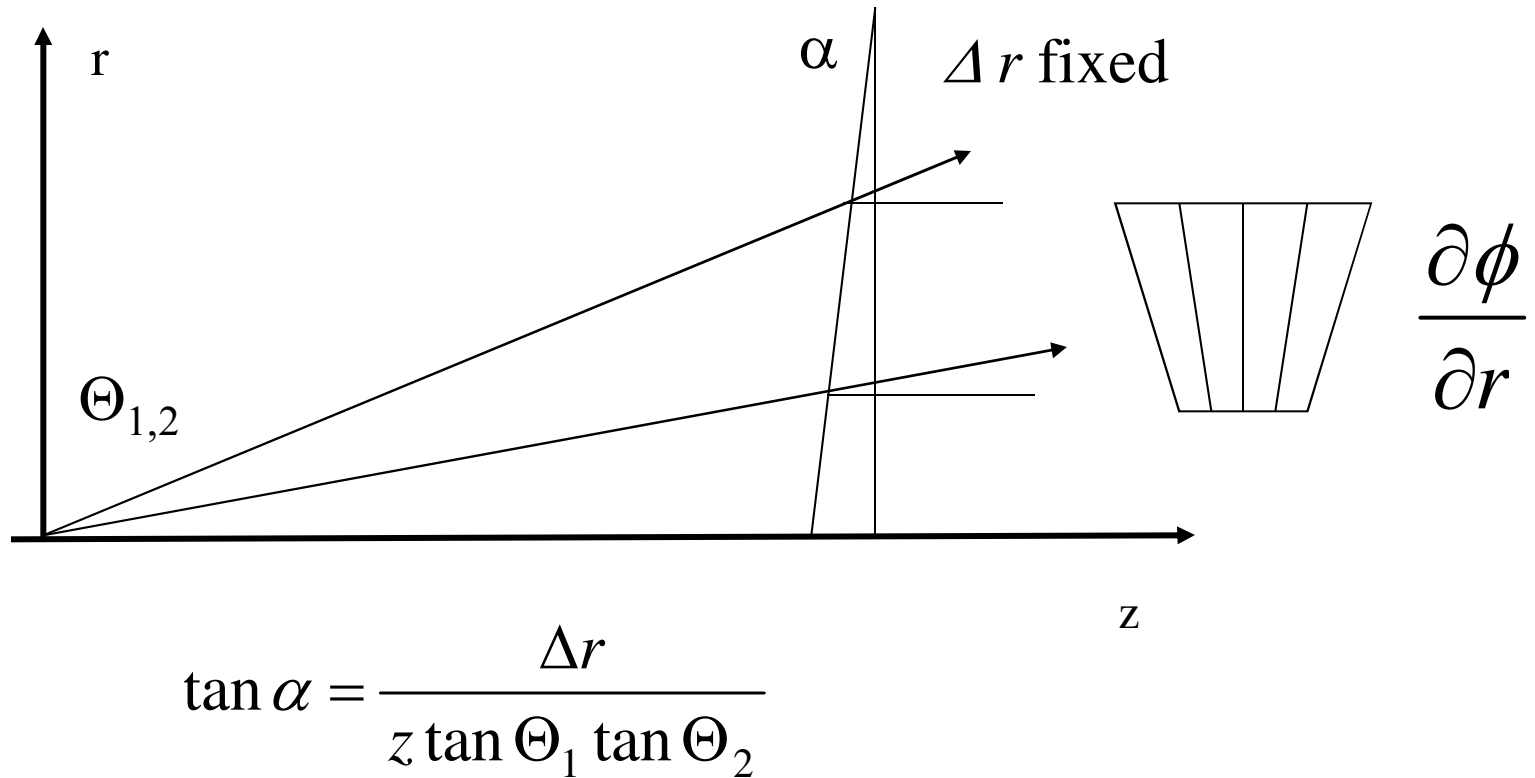


In a binary scheme the natural binning unit will be a half-pitch

Allow 1 or 2 strip clusters

For reasonable pitches, sensor separations, and momenta find ~2-5 bins
Local module output could be 3 bits : 7 bins + 1 sign

Petals Configured as Trigger Doublets



Description of Simulated Layout

- sLHC outer barrel modules
- L4 = 100 cm, L3 = 74.3cm
- 10 x 10 cm module
- 4.5 mm radial separation within module
- 75 micron pitch
- Not tilted
- Material = present SCT (over estimate)
 - Case 1: all material is before layer
 - Case 2: all material is within layer
- Single particle samples, 1 GeV π, γ, n and 20 GeV μ

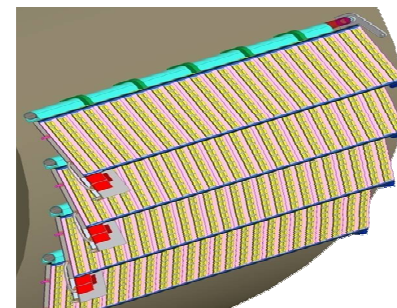
Simulation Results

- Ran 10K single particles/type through a GEANT4 simulation
- Layout is a mix of the present SCT material (mass) with an sLHC layout
- Trigger Hits are defined as doublets with a ≤ 2 strip window, 1-2 strip cluster
- Raw Hits are defined as all hits (=200 for efficient charged, no interactions)

	Trigger Hits per 100 particles	Trigger Hits per 100 particles	Raw Hits per 100 particles
	Material in front	Material within	Material within
1 GeV γ	1.44	0.71	75
1 GeV π	1.16	0.71	214
1 GeV n	0.09	0.05	117
20 GeV μ	-	89	217

Simulation Results

- Want to be efficient for stiff charged tracks: OK
- Keep material out from in front of layer
- Normal data is read out at 100 KHz
- Trigger data is read out at 40 MHz
- Want the data rate from triggers (real and background (min-bias)) to be of same order as the normal data rate
- Find this to be ~ 2 : so twice as much trigger background as real (100 KHz) L1 triggered data
 - Need to run proper min-bias samples
 - Need to vary layout (separation, trigger criteria, material...)

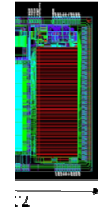
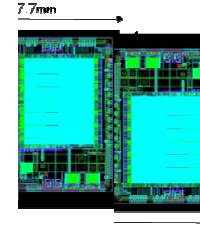
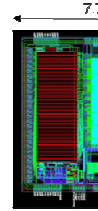
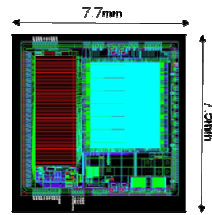


$$400 \times \frac{(TRate(1 GeV \pi) + TRate(1 GeV \gamma))}{(Raw(\pi) + Raw(\gamma))} \approx 400 \times 0.005 \approx 2$$

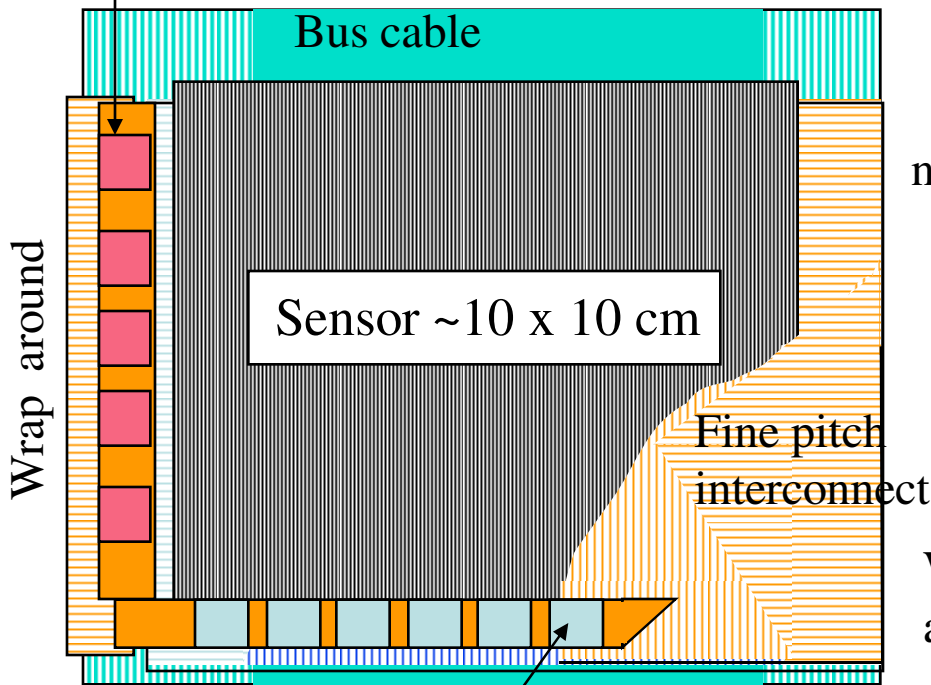
Technical Concept

Split the readout chip and use embedded fine pitch interconnection

ABCn
Binary readout



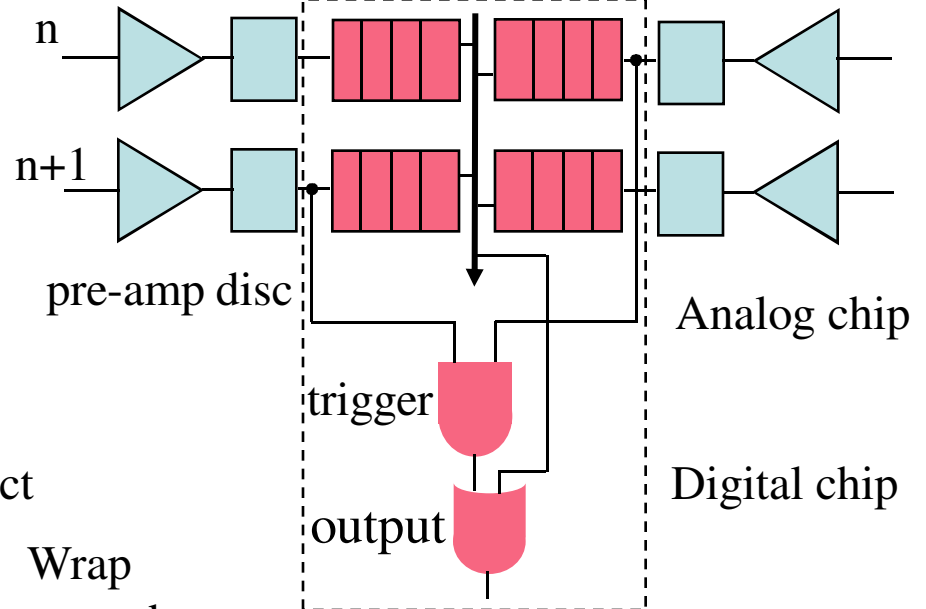
Digital chip on hybrid x5



top

pipeline

bottom



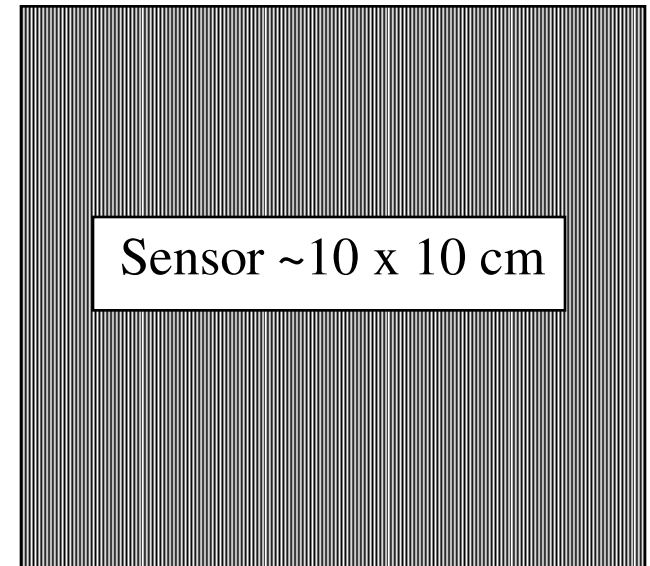
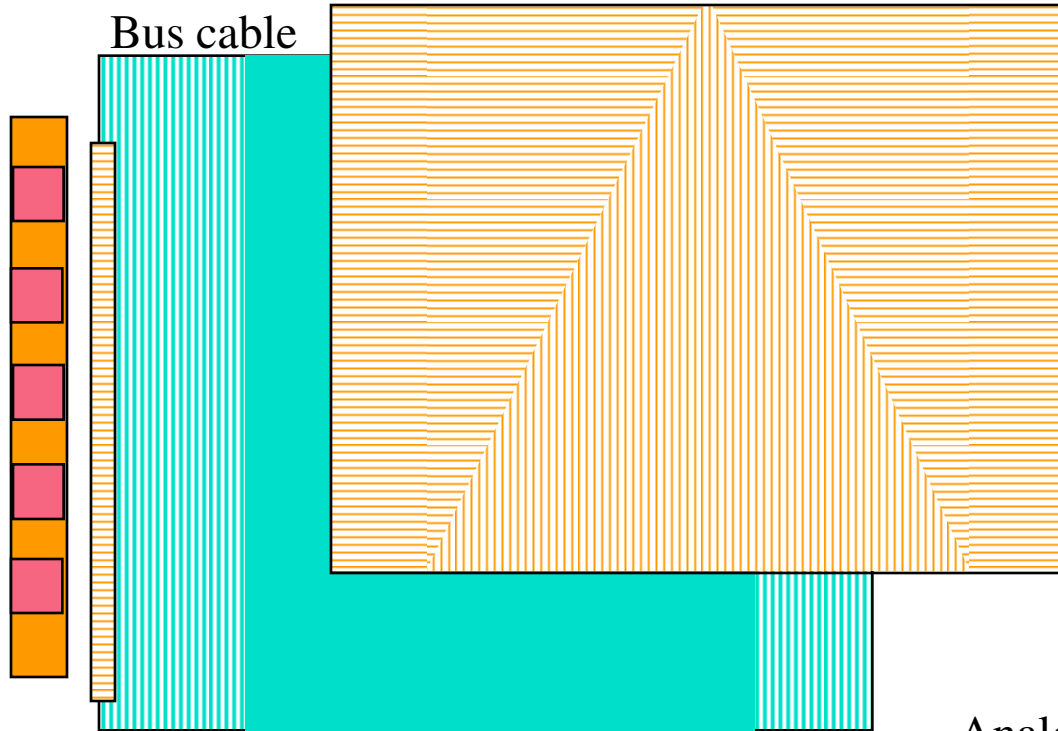
Wrap around

Analog chip on hybrid x10

Technical Concept

Digital chip on hybrid

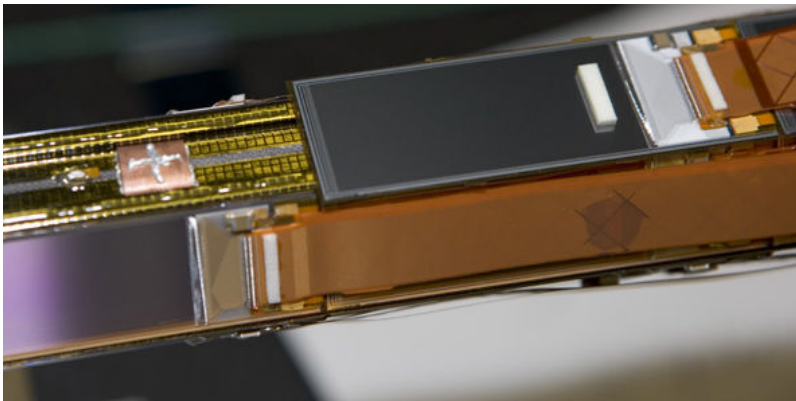
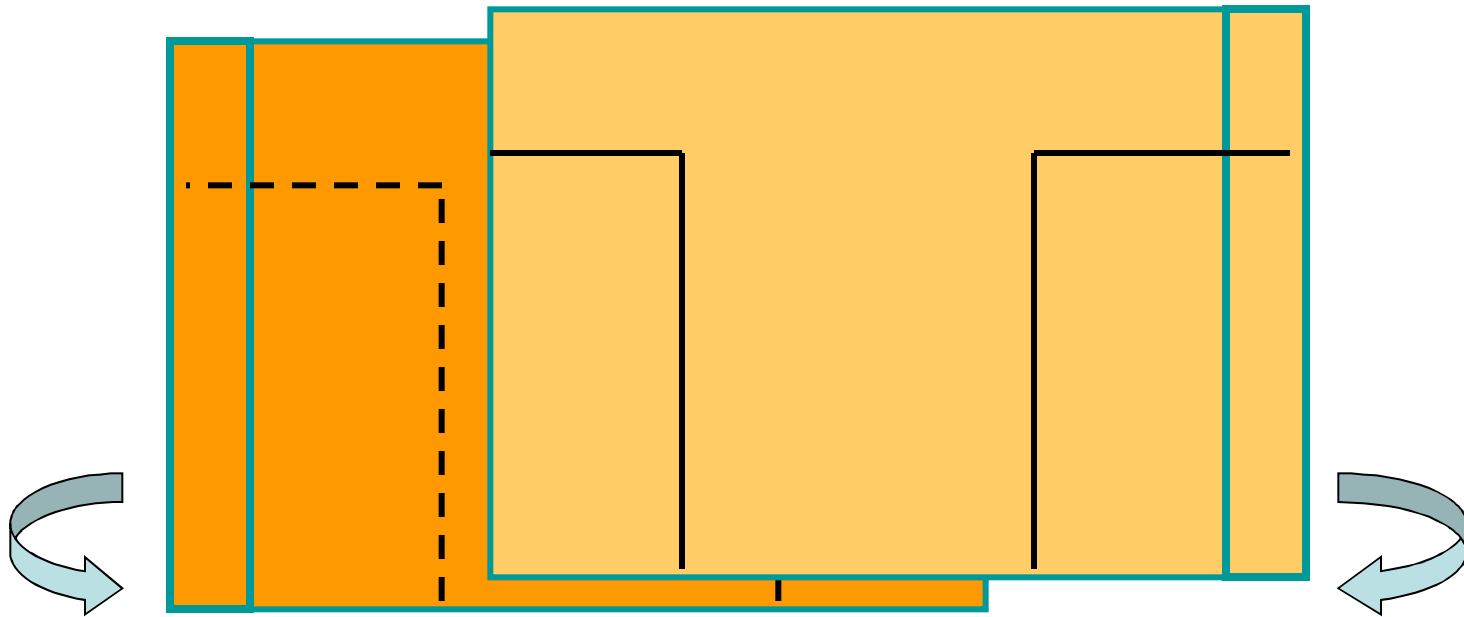
Fine pitch
interconnect



Analog chip on hybrid



Structure of Interconnect/Wrap-around

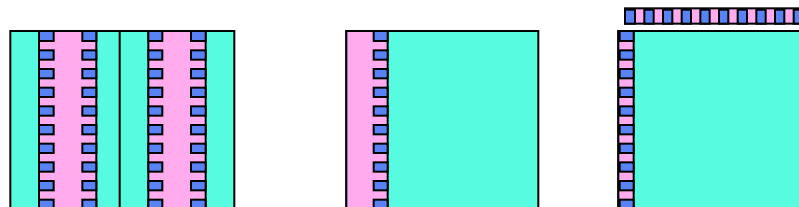


Fine pitch interconnect method used for D0 Layer0, CDF Layer00 projects, and BaBar

Impact

- Consider effect of additional chips and interconnect material on the stave
- Compare to material estimates studied earlier as part of ongoing stave R&D
 - Effect of trigger components is not large
- Of potentially more concern are thermal and electrical interference
- Impact of axial/axial vs axial/stereo not yet known

Stave	Flex SS	Flex LS	Flex LS + Trig
Core	0.73	0.73	0.73
Module	1.49	0.96	1.07
Glue	0.04	0.04	0.04
Total %Xo	2.26	1.73	1.84

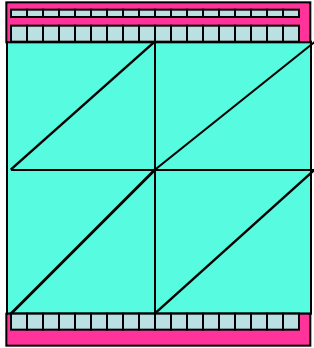


Conclusions

- Stave/petal element is a natural basis for local doublet trigger
- Electrical/interconnect concept is a small perturbation on existing mechanical design
- Additional mass is not significant, keep mass within or behind
- Need to study electrical interference aspects
- Implications for data rates and bandwidth need more detailed and realistic simulation but do not yet appear severe
- Overall optimization of tracker needs consideration

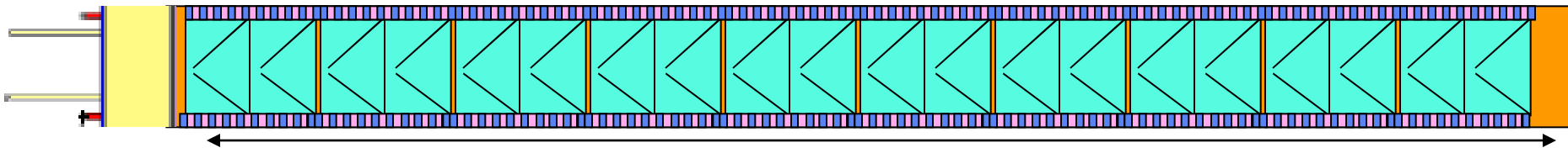
Extra Slides

Short Strip Concept for a Trigger Stave

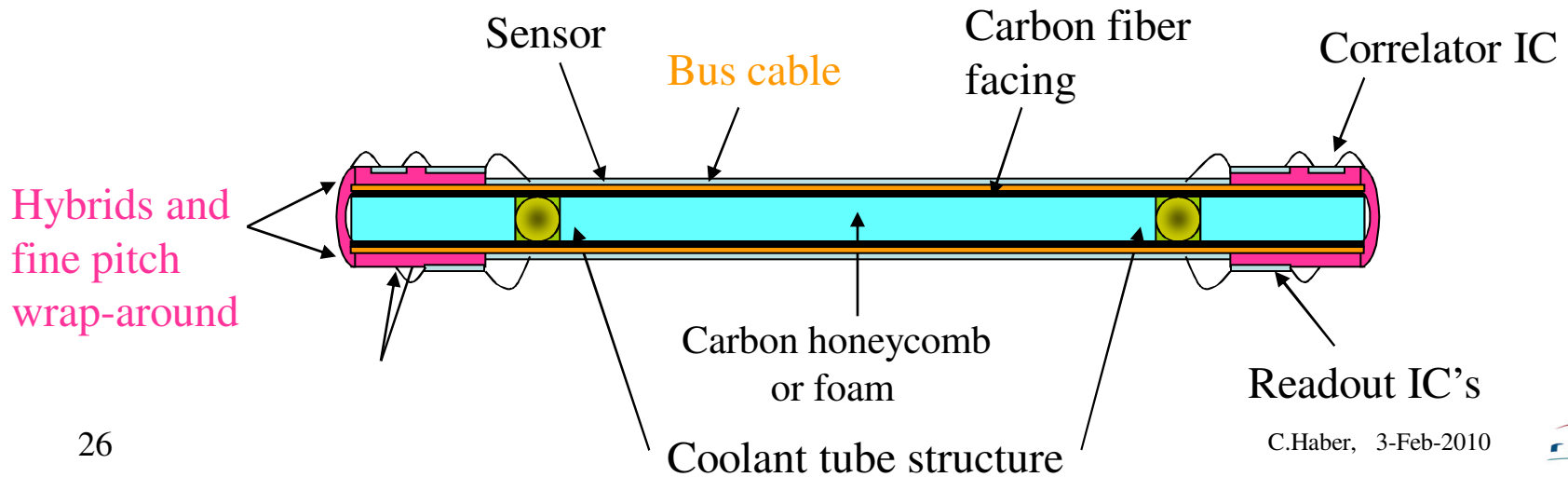


Double metal sensor module

Idea is to read out strips from both edges using double metal layer
A correlator chip looks at hit patterns from both sides.



~ 1.2 meter



Background Variation with Strip Cut

