Wireless transfer of L1 track trigger data in ATLAS ID

R. Brenner (with help from S. Cheng and H. Kratz, Microwave Technology Group, Signals and Systems, Uppsala University)

1/(20)

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Extremely High Frequency technology

- Motivation for wireless data transfer in the track trigger
- Simple idea

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- Initial tests
- A more sophisticated idea
- Key technology development
- Conclusions

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The present tracker readout architecture is not optimal for trigger... a fundamental difference



Physics events are triggerd in Rol that are conical regions radial from the interaction point in Φ and η

Wireless transfer with millimeter wave:

Small and low mass components of materials already used in our trackers

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- Low power
- Low cost
- High band width

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Off detector

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> Transfer L1 data from the cryostat wall to Content Addressable Memories (CAM) or Associative Memories (AM) for fast pattern recognition located in ATLAS cavern

Ex. patterns for a geometry with three layers

- 80 μm pitch and reconstruction down to 1GeV pT: 70 Gpatterns
- 320 μm pitch and reconstruction down to 10 GeV pT: 500 Mpatterns

Simulation by Sebastian Schmitt (Univ. Heidelberg)

... not easy either





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Fakes vs. resources



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The result shows it is almost impossible to send signals through a silicon module

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A more sophisticated design

- Take advantage from the fact that signals do not penetrate silicon sensors in the design of the wireless network because of no interference between layers
- Invent a new way to transfer L1 signals and at the same time reduce number of fakes.
- Use separate antennas for reception and transmission to avoid the screening problem





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Reduction of fakes with correlation





Doublets

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Triplets

- Correlation between two layers or three.
 - Use only the axial strips on modules
 - Accept hits only in pT window >8GeV (2-3mm on next layer)
- Correlation between two sides of an axial-axial module

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- Each module has to share data with 4-6 modules on the ne layer
- Directive antenna technology important to get high gain (low power) and reduce interferences
- Perhaps a fully integrated scheme with chip-to-chip data transfer between layers (which would require chips on different layers facing each other.

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Key technology development

- Integration of trigger in frontend ASIC and on detector module -> 130nm process leaves plenty of space for trigger on the ABCDnext
- Integration of wireless data transfer on module or FE chip using 3D assembly techniques
- Development of correlation logic and optimal data formatting



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2.75mm

2 5mm

- Surface integrated waveguides (SIW) in kapton
 - MEMS antennas in silicon

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60 GHz

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Berkeley Wireless Research Center (C. Marcu et al.), A 90nm CMOS Low-Power 60GHz Transceiver with Integrated Baseband Circuitry, prsented at ISSCC 2009

New version in 65 nm CMOS in process at ST Microelectronics





DOWNCONVERTER

QUAD

PRBS

CHECKER

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Integrated slot array antenna

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