



Development of Interconnect Technologies for HEP Applications

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WIT2010, LBNL, Feb 4, 2010**

The Need for Development

The last round of detectors typically had at most one layer of bump bonds and an array or two of wire bonds. There were yield issues but the needs were mostly met. The situation in the next decade will be different:

1. Complex multi-layer attachments
2. Internal flex cable busses running between detector sub-units.
3. Wide variety in pad pitch, array size and mechanical strength.

Solutions exist for most of the assemblies being considered ...

... but, **are they available to you for your prototyping needs?**

1. Vendors are not willing to take on small custom jobs. Or they demand large \$\$.
2. It is difficult to work closely with vendors and solve problems because they protect their proprietary processes.
3. Long turn around time slows down progress.

Interconnect Technology at UC Davis

We acquired a flip-chip bump-bonder in 1993 as part of the DOE Infrastructure Program. This machine was used for bump bonding CMS forward pixel prototypes among other projects.

Since then we have started exploring other new techniques for interconnection of electronics and detectors/cables.

A recent DOE ARRA grant has encouraged us to enhance our capabilities and develop a wider spectrum of technologies.

In this talk, we describe two R&D projects as examples of diverse needs and also discuss some generic development.

Si/W ECal R&D Collaboration

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J. Jaros, T. Nelson
SLAC

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S. Adloff, F. Cadoux, J. Jacquemier, Y. Karyotakis
LAPP Annecy

Si-W: An Imaging Calorimeter



High Degree of Segmentation

- 3D general pattern recognition capability
- PFA: particle separation in jets
- ID of specific objects/decays: e.g. tau
- Tracking (charged and neutrals)

Si-W Calorimeter Concept

Baseline configuration:

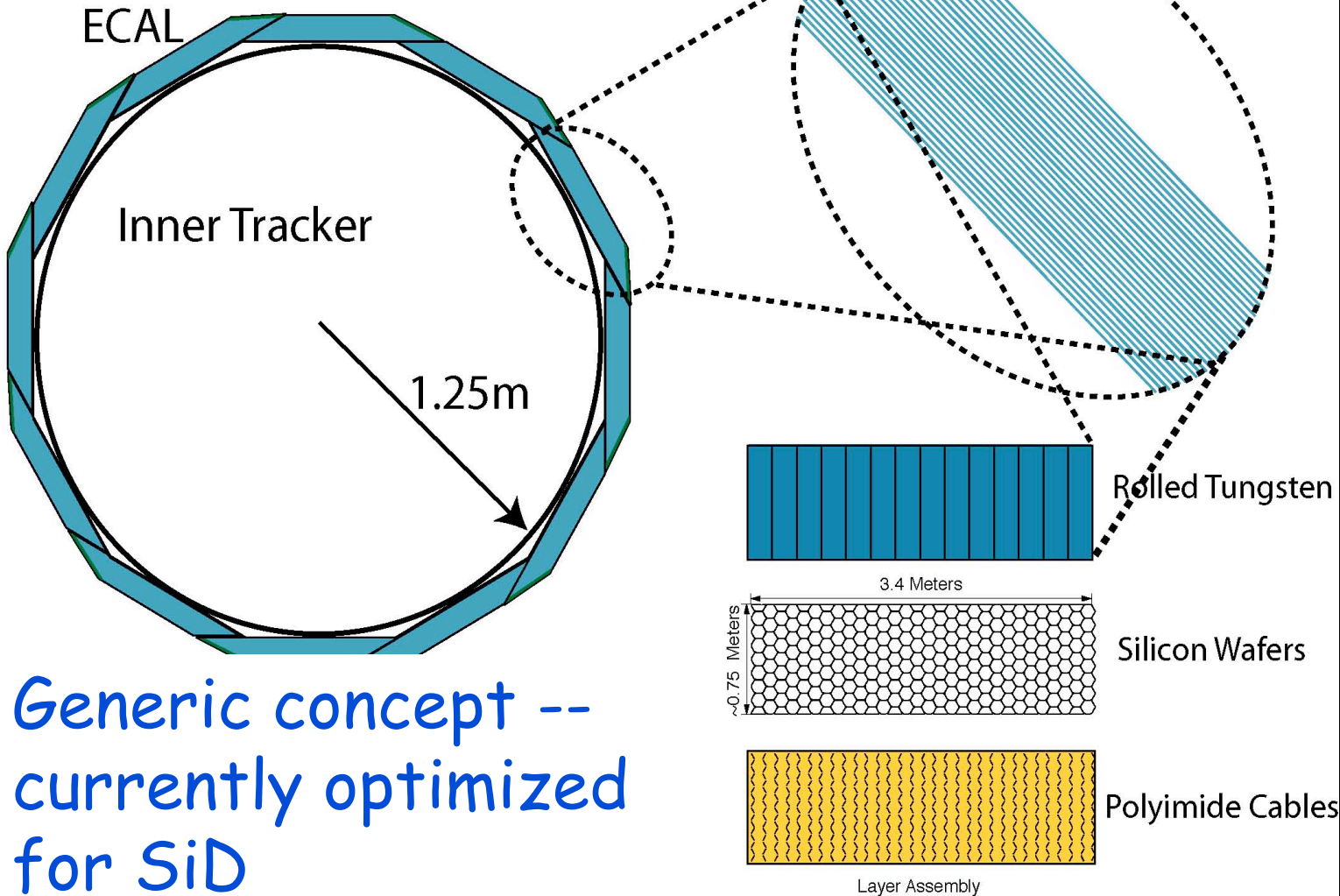
- transverse seg.: 13 mm^2 pixels

- longitudinal seg:

$$(20 \times 5/7 X_0) + (10 \times 10/7 X_0)$$

$$\Rightarrow 17\%/\text{sqrt}(E)$$

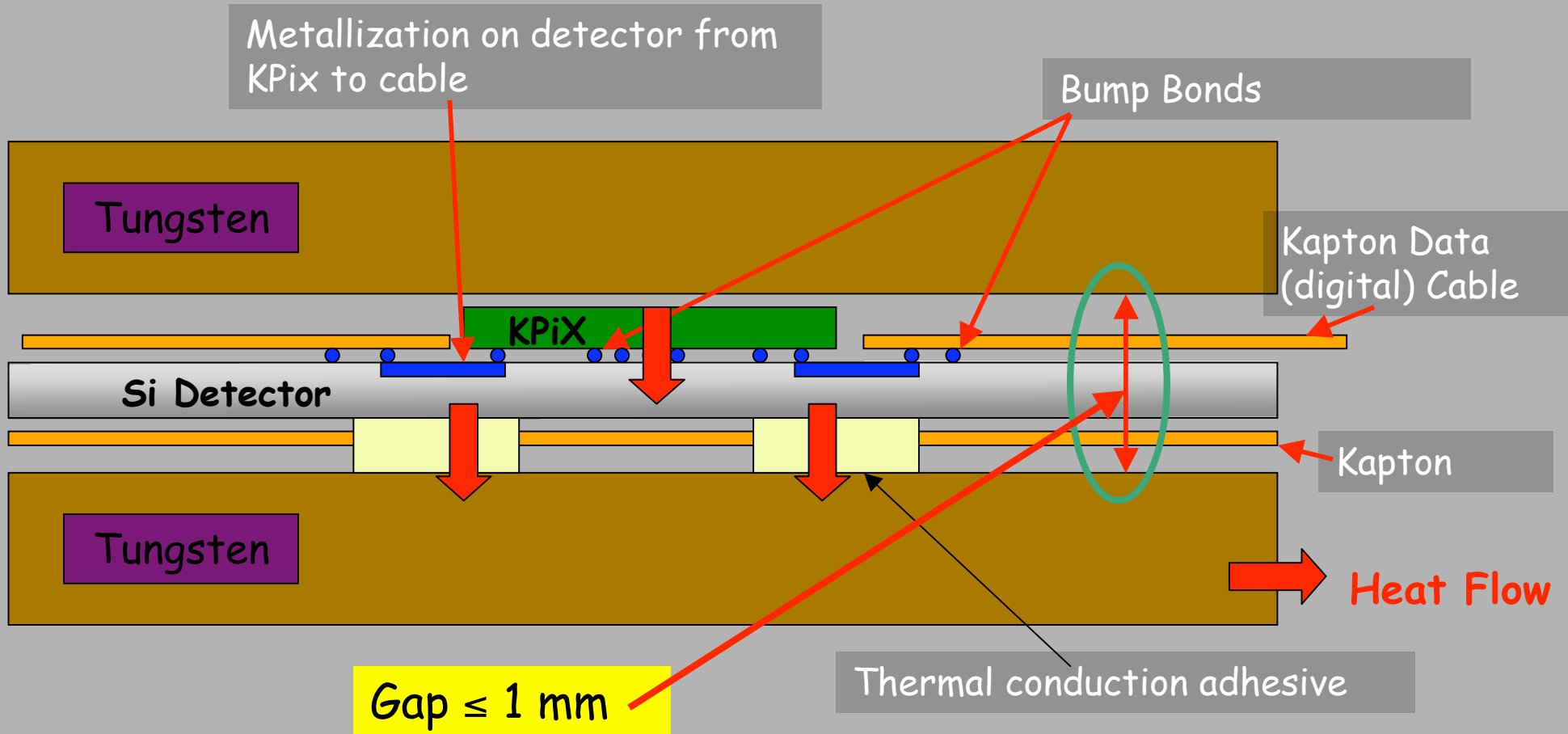
Si-W Calorimeter Concept



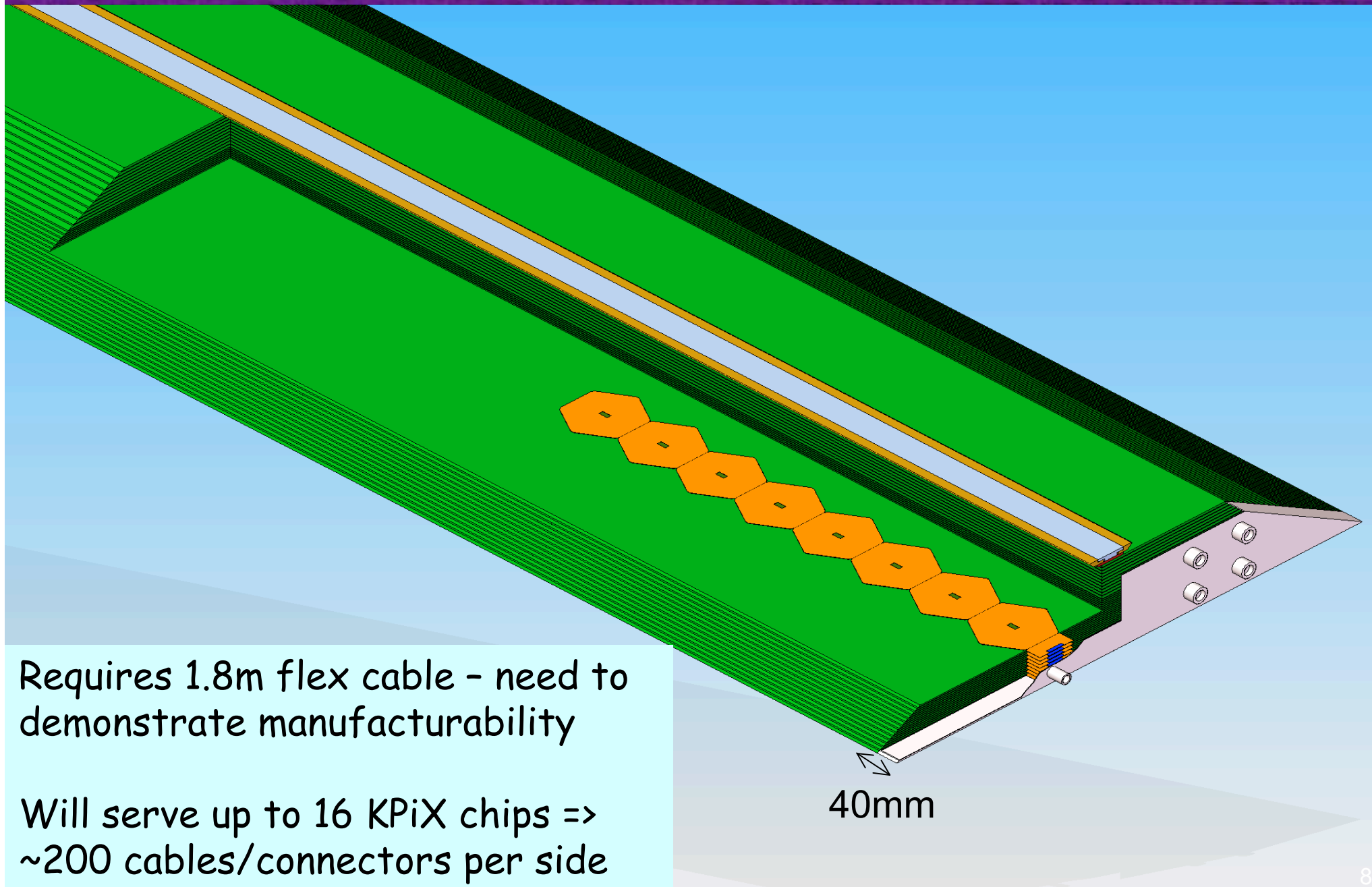
Generic concept --
currently optimized
for SiD

• 1 mm readout gaps \Rightarrow 13 mm effective Moliere radius

Readout gap cross section (schematic)



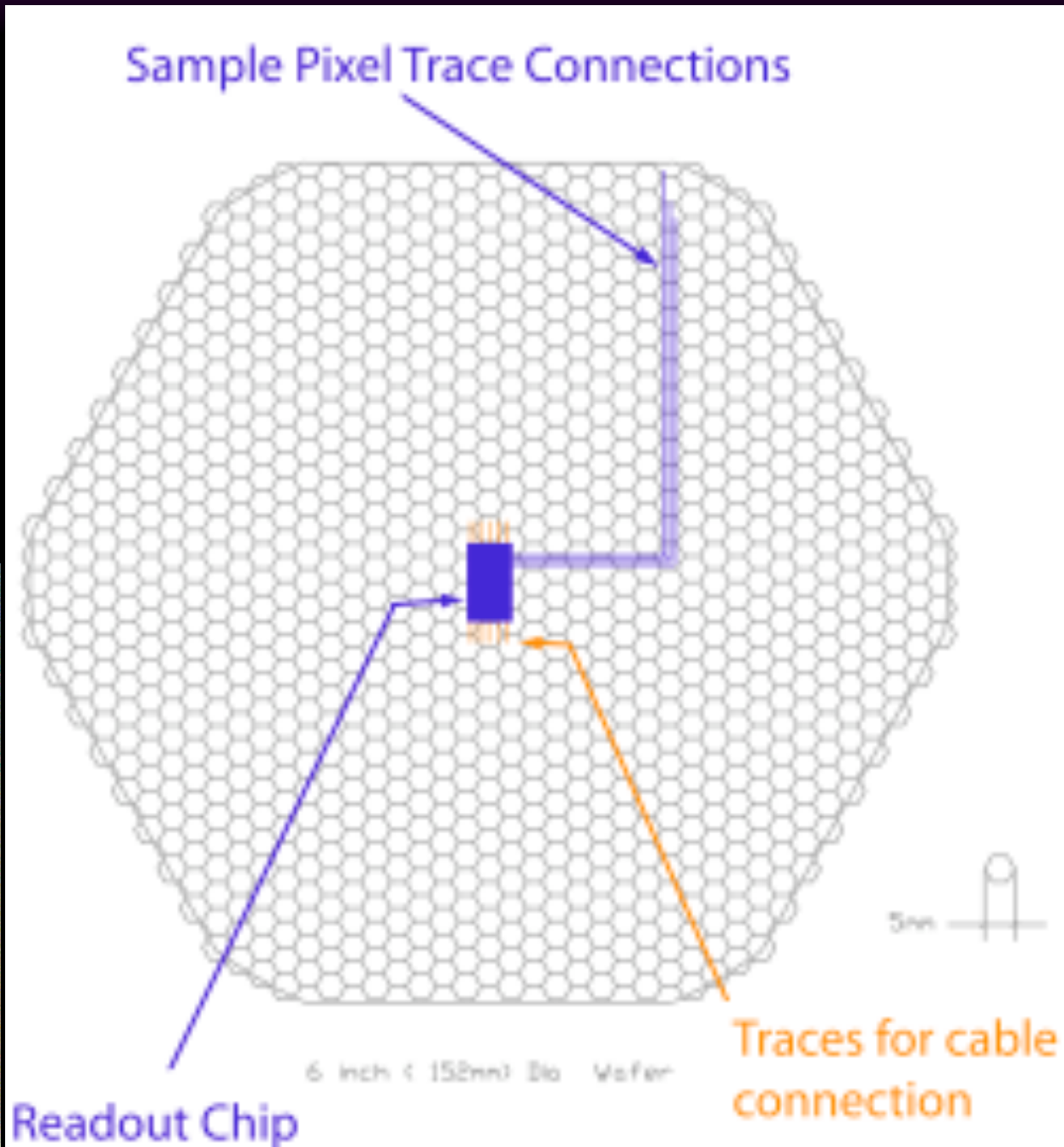
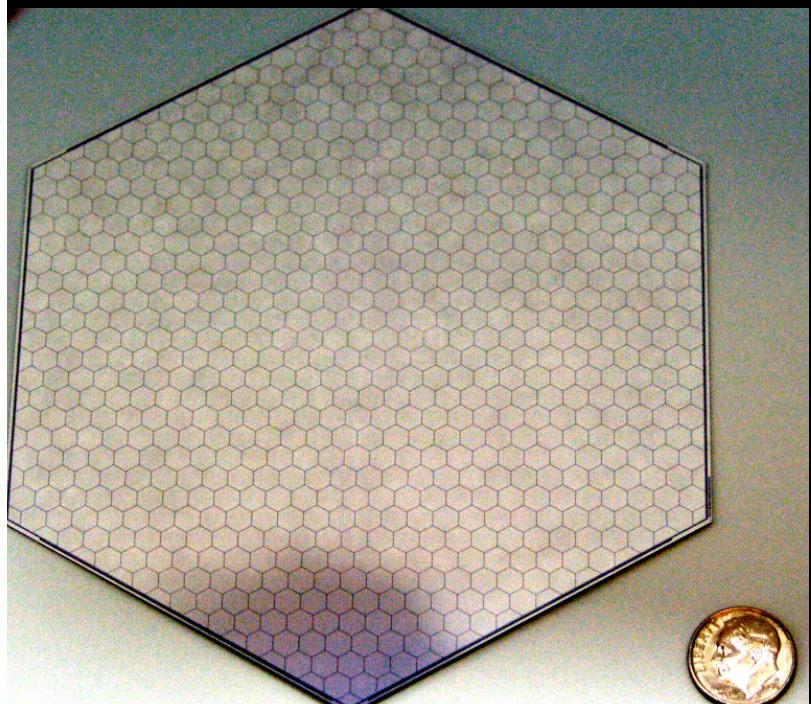
Module Design



Si Detector

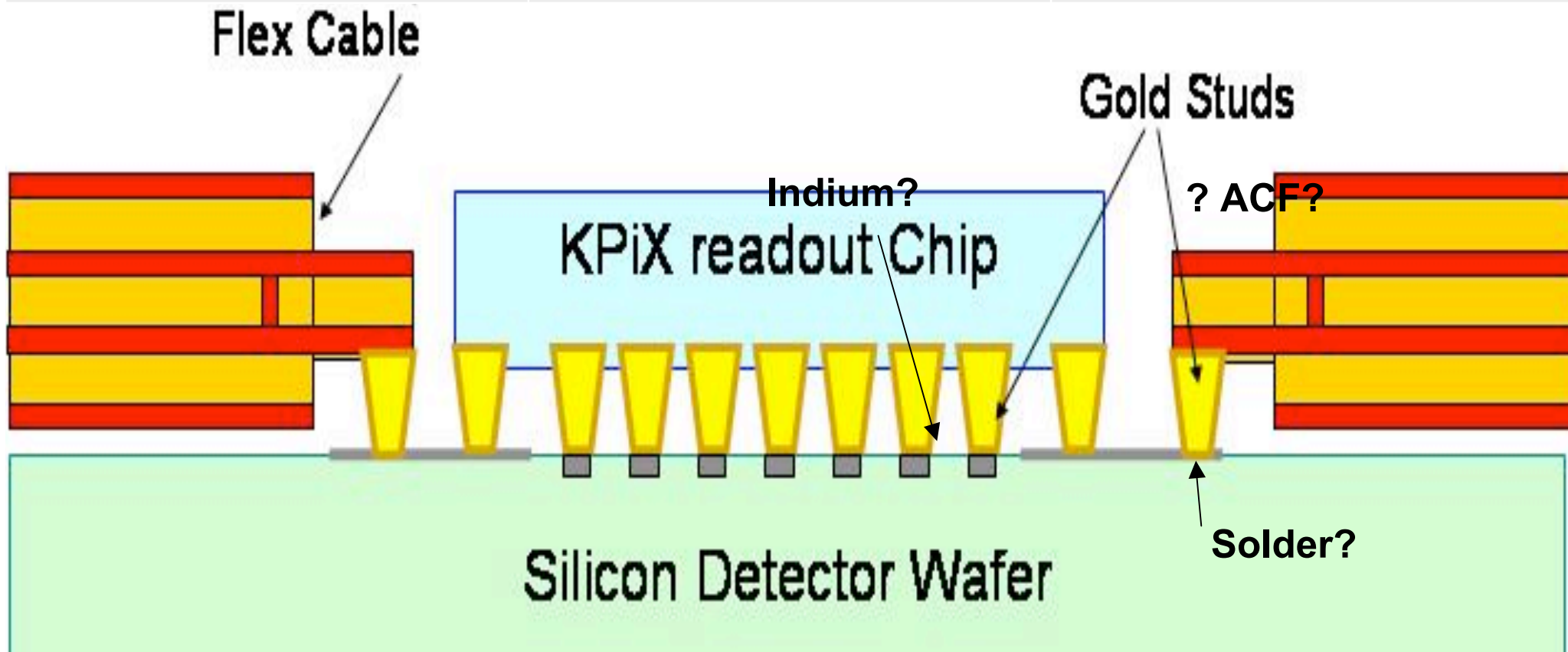
Wafer

- 6 inch wafer
- 1024 13 mm^2 pixels
- Hamamatsu Prototype (ver2) sensors in hand (40 wafers)



Interconnect issues: Technologies being considered

	Prototyping	Production
KPiX to Sensor	Gold Stud Bonding	Indium/Solder Bump Bonding
Flex Cable to Sensor	Solder Balls Conducting Epoxy ACF	ACF?



Track Trigger for CMS @ SLHC

J.P. Chou, U. Heintz, M. Narain, M. Segala, N. Vlamis, *Brown University*

M. Mannelli, *CERN*

J. Alexander, J. Dobbins, L. Fields, T. Lutz, N. Rider, A. Ryd, J. Thom
Cornell University

M. Chertok, R. Erbacher, B. Holbrook, R. Lander, J. Thompson, M. Tripathi
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W.E. Cooper, M. Demarteau, G. Deptuch, J. Hoff, M. Johnson, R. Lipton, T. Miao, L.
Spiegel, S. Tkaczyk, M. Trimpl, R. Yarema, Z. Ye, T. Zimmerman, *Fermilab*

A. Chandra, J. Ellison. *University of California, Riverside*

R. Demina, R. Flight, Y. Gotra, S. Korjenevsky, *University of Rochester*

J. Incandela, *University of California, Santa Barbara*

M. Weinberger, *Texas A&M University*

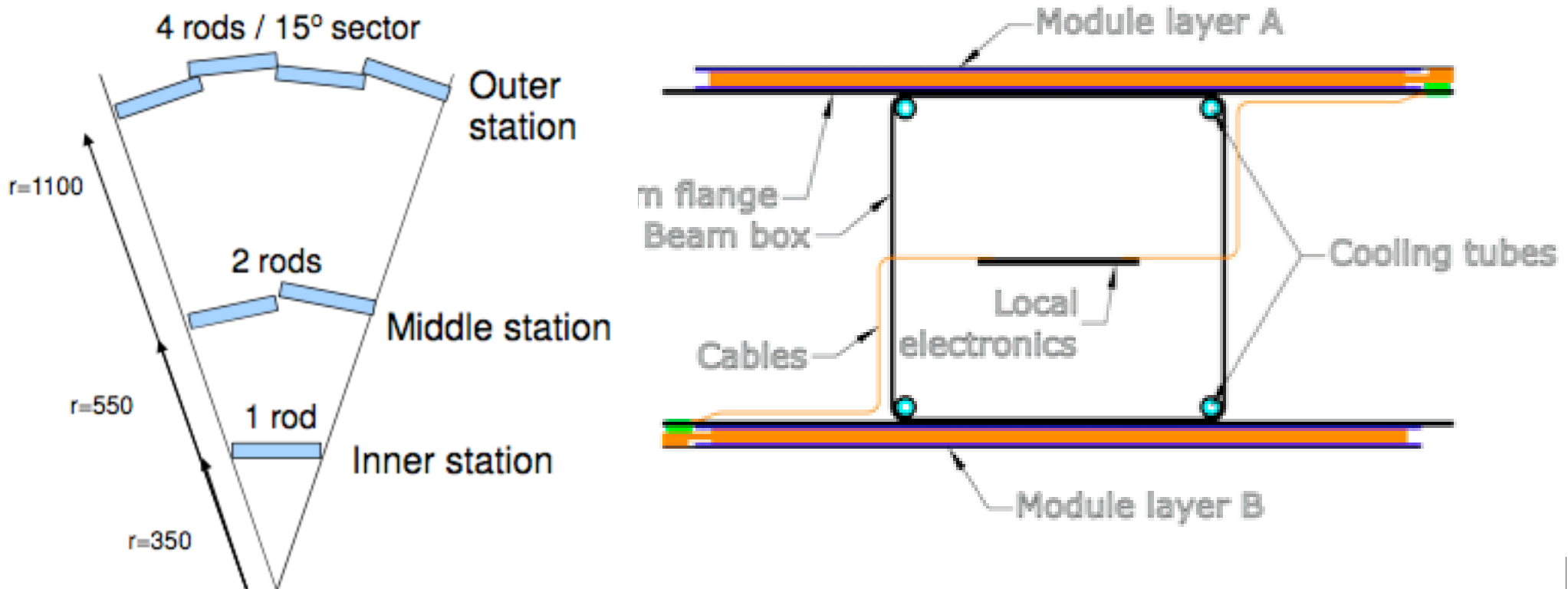
E. Brownson, P. Sheldon, *Vanderbilt University*

SLHC Track Trigger Concept

Sector based approach to track finding. P_T cut applied at 0th level.

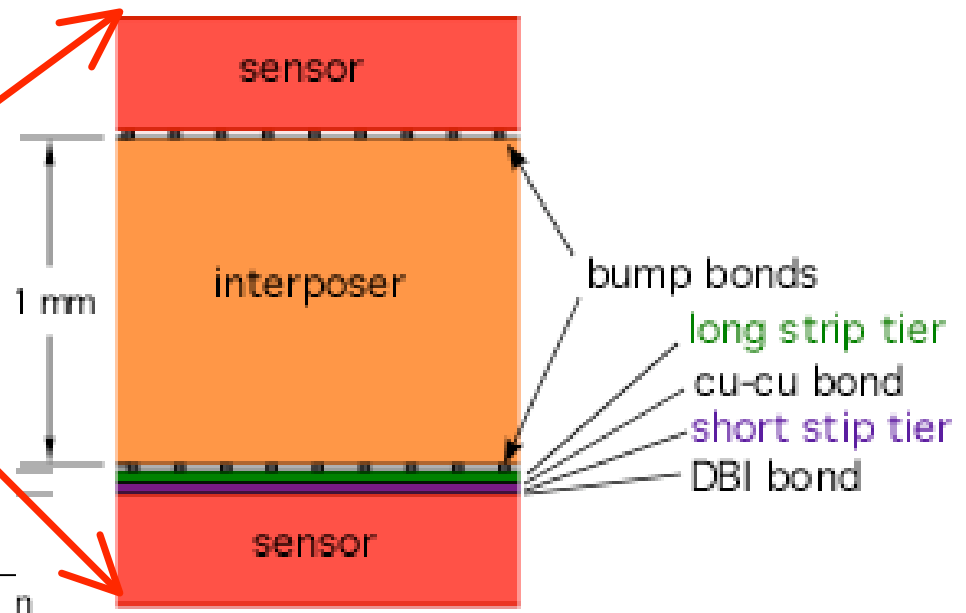
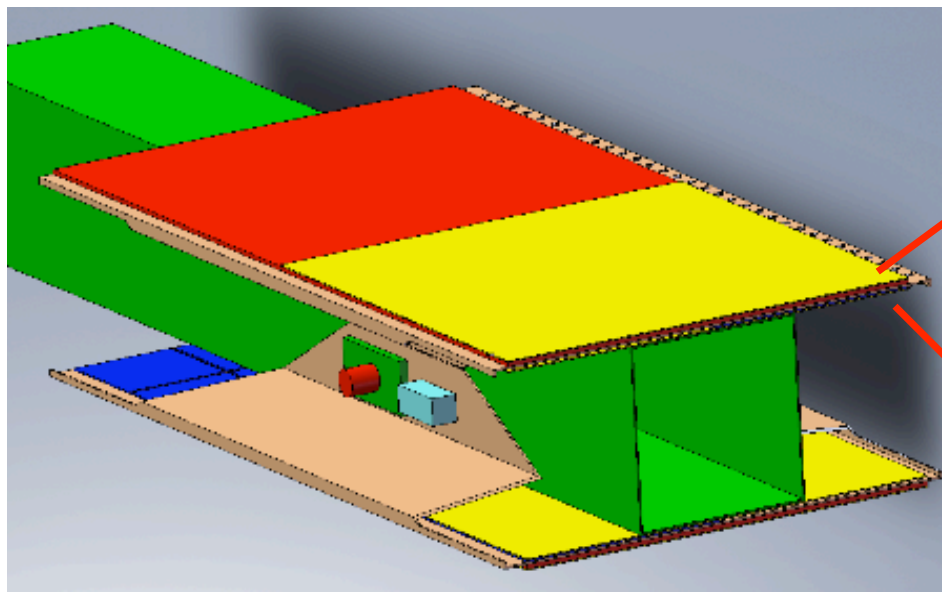
15 degree sectors with 3 layers of double stacks each.

See talks by Manelli, Lipton, Cooper, Alexander, Heintz.



Double Stack Interconnects

	Prototyping	Production
Interposer to Sensor Interposer to 3-D chip	Gold Stud Bonding	Indium/Solder Bump Bonding
Flex Cable Attachment	Wire Bonding Solder Balls Conducting Epoxy ACF	?



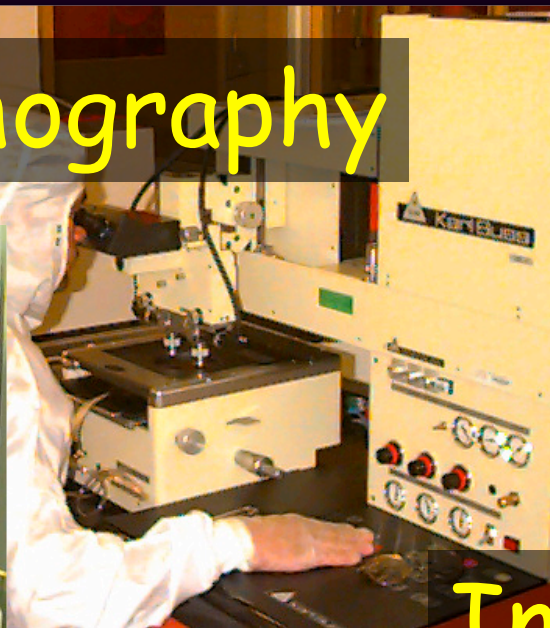
Areas of R&D in Interconnect Technology

- Single die photolithography for Indium
- Under bump metallization studies
- Smart flex cables
- Conductive epoxy evaluations
- Gold Stud attachment
- Anisotropic Conducting Film attachment
- Flip-chip bonding

Processing at UC Davis

Photolithography

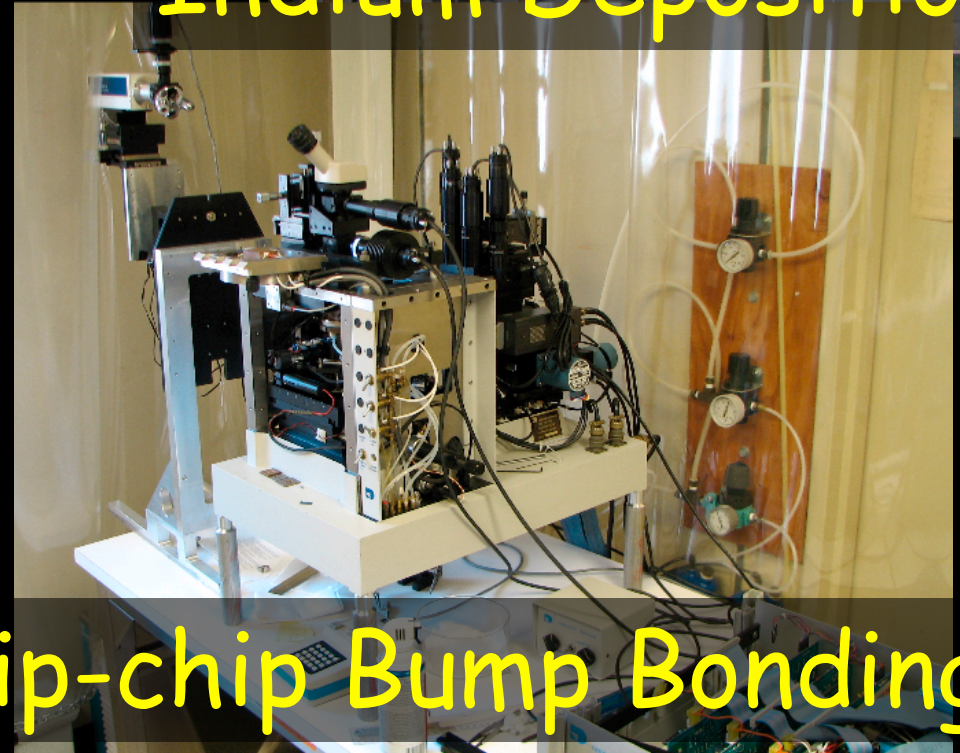
Ti/W Sputter



Indium Deposition



Gold Studs



Flip-chip Bump Bonding

Indium Bump Bonding

Wafer level Indium Bump Bonding is a mature/commercial technology. Best option for small bumps (<10 μm).

However, prototypes involve single die photolithography.

We are developing processes involving:

- a) silicone films and
- b) EDM machined cavities.

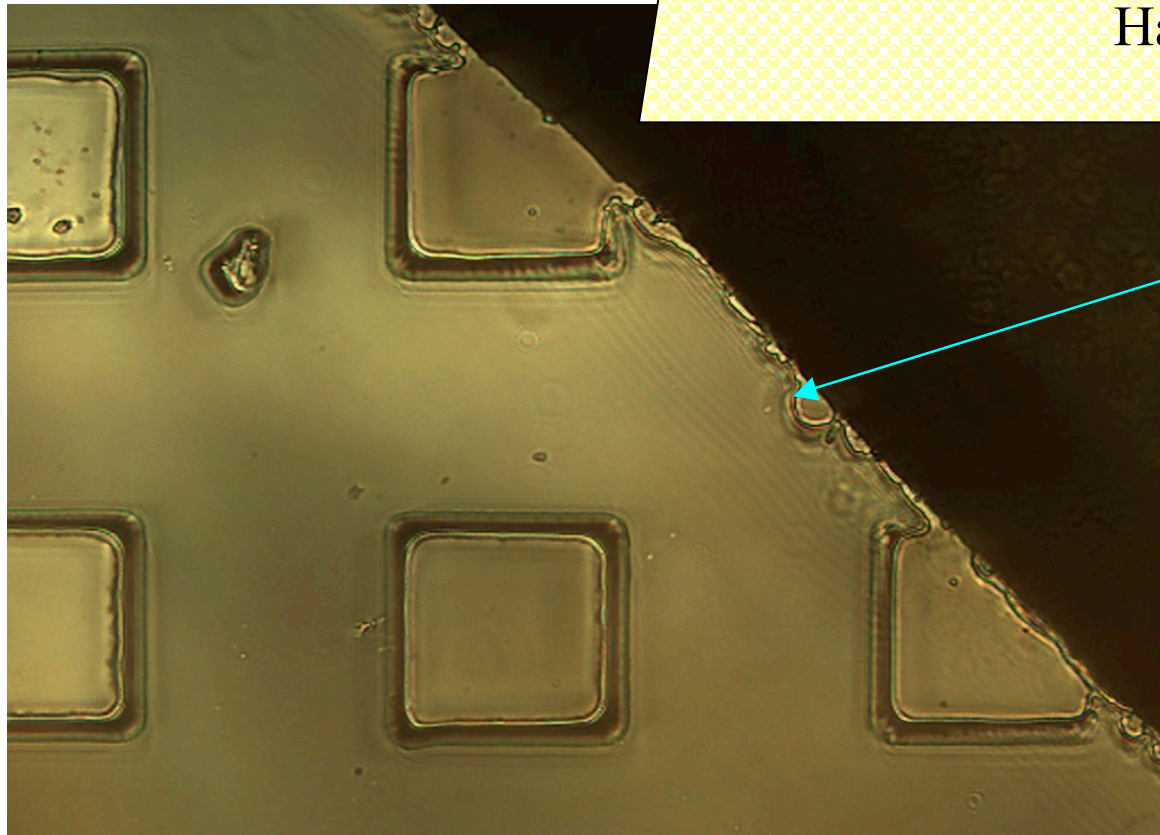
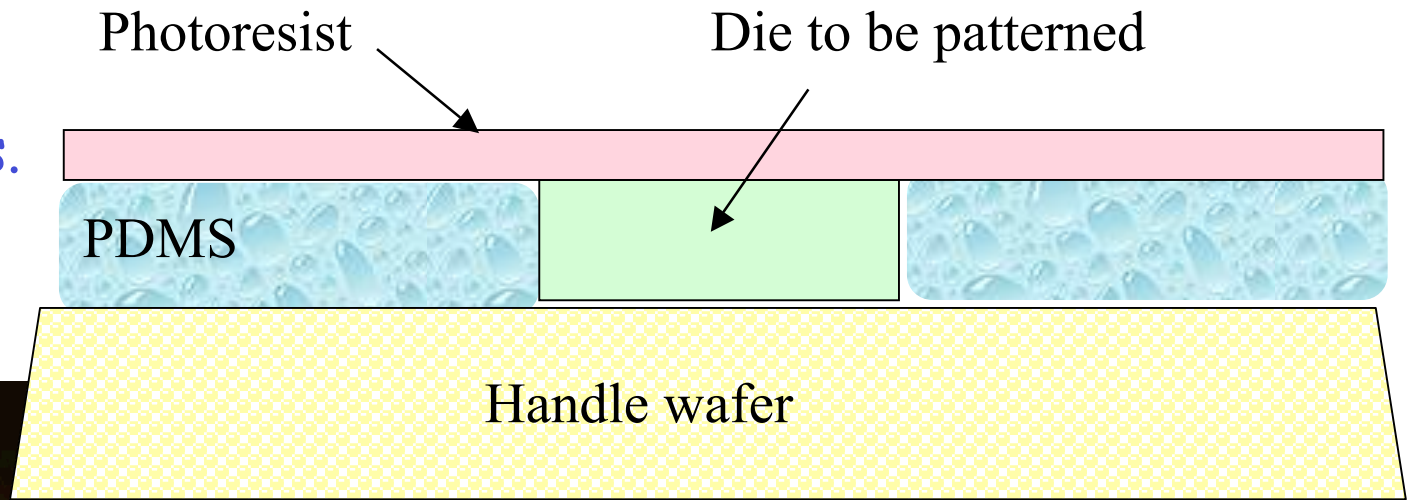
Spinning resist on a single die typically results in an edge-bead that prevents Good mask contact.



Polydimethylsiloxane (PDMS)

This technique can handle very small chips.

Work in Progress.



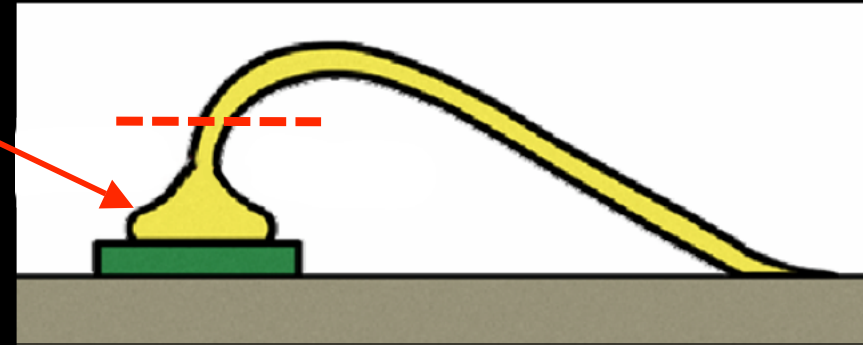
No significant edge-bead formed.

Gold Stud Bump Bonding

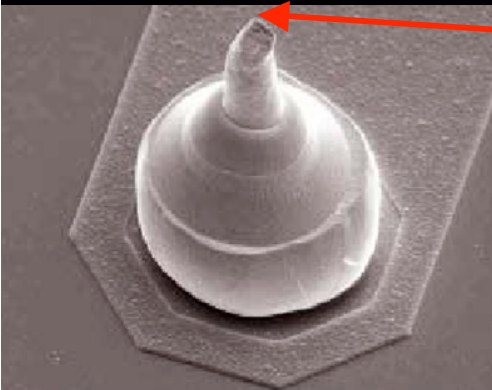
- An attractive option for prototyping because no photolithography is required for forming studs. Minimum bump size typically ~ 50 μm .
- However, the opposite chip requires surface treatment if it has typical aluminum pads.
- Not a problem for Si-W (opposite "chip" is a large wafer) or CMS 3D Track Trigger (interposer is custom made with Au).
- Au-Au bonding is possible, but so far the attempts have been for large bond pads (>100 μm).

Gold Stud Formation

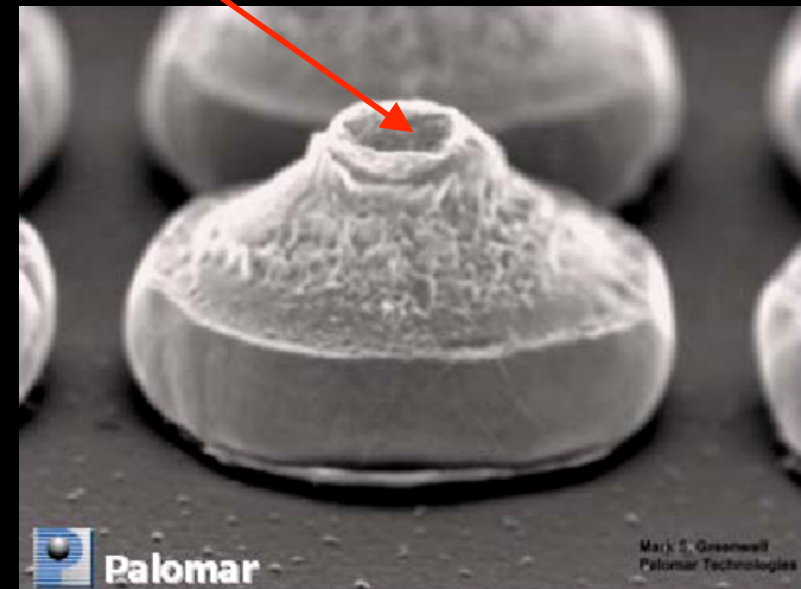
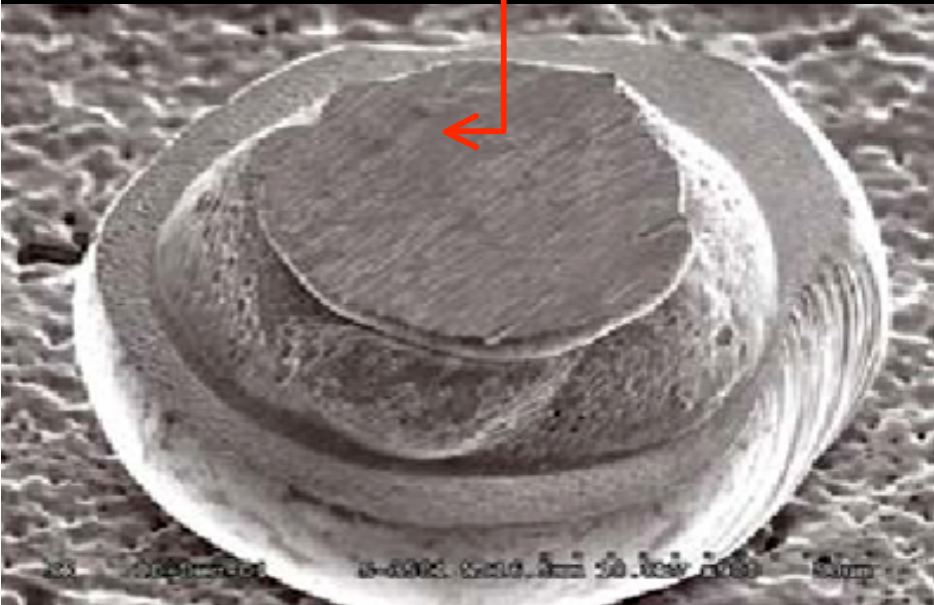
Step 1: A $\sim 25 \mu\text{m}$ gold wire is bonded to the pad.



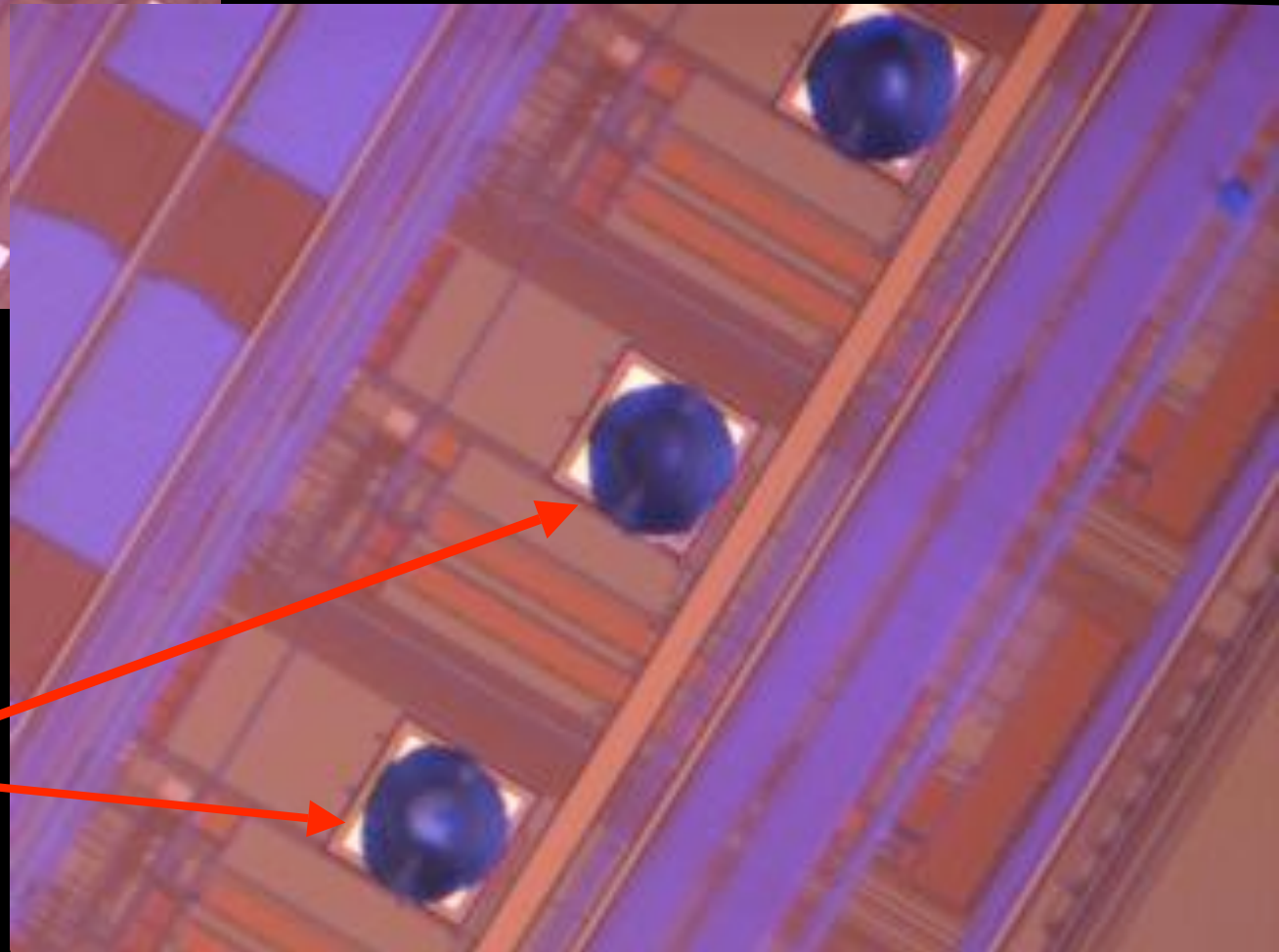
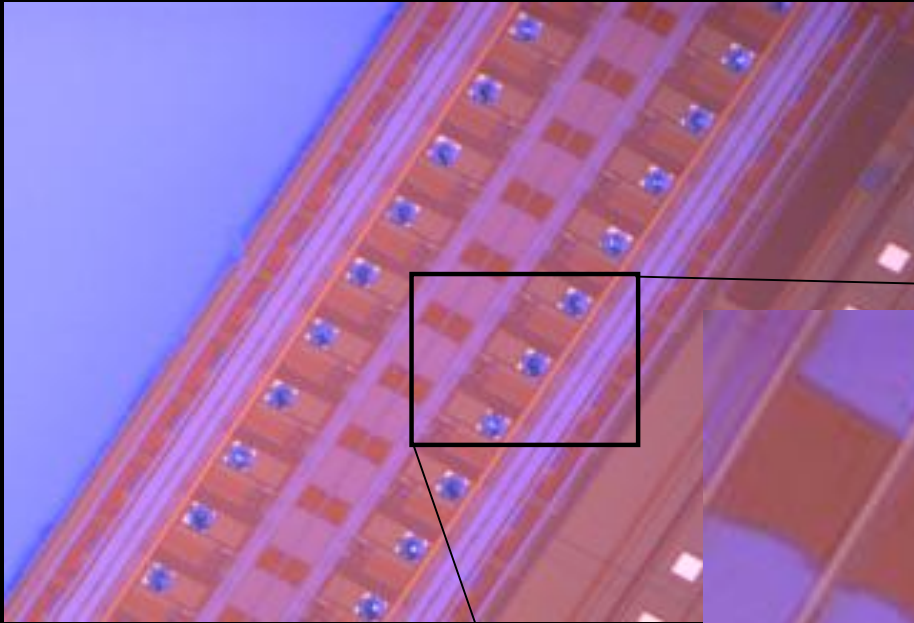
Step 2: The wire is snapped off.



Step 3: The stud is "coined" (flattened) to provide a better shape. Alternately, the wire is pushed back into the ball after snapping. The result is a matted surface.

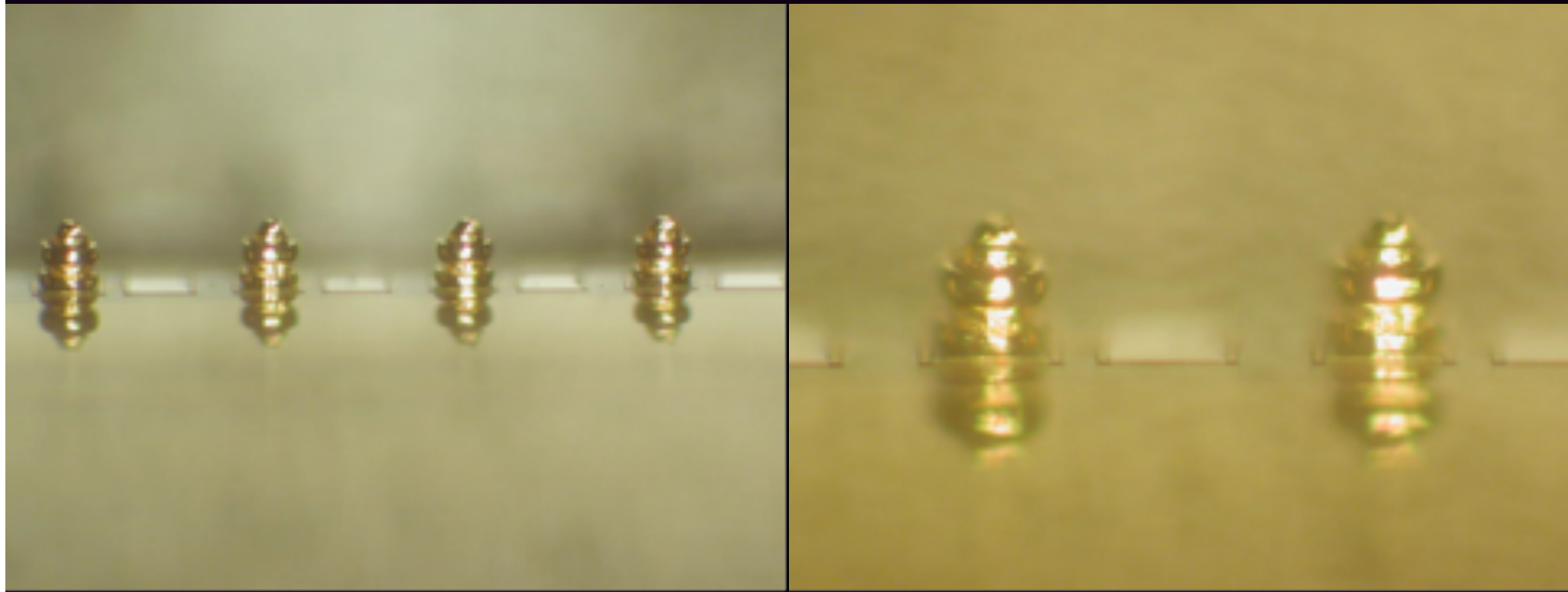


KPiX with Gold Studs



Studs are well-formed and centered on the $70 \times 70 \mu\text{m}$ pads.

Double Studs on test wafers



	<u>ball diameter - um</u>	<u>ball height - um</u>	<u>shear strength - grams</u>
count	10	10	10
average	58.4	66.0	21.0
stdev	1.0	.76	1.1

Gold Stud Attachment

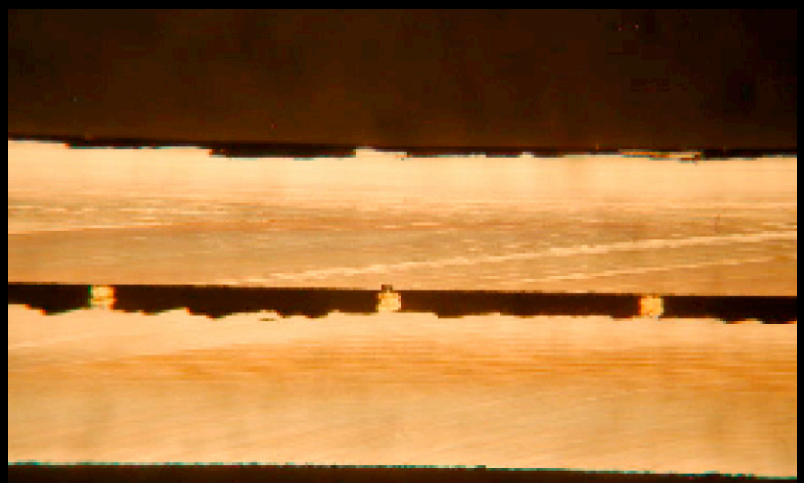
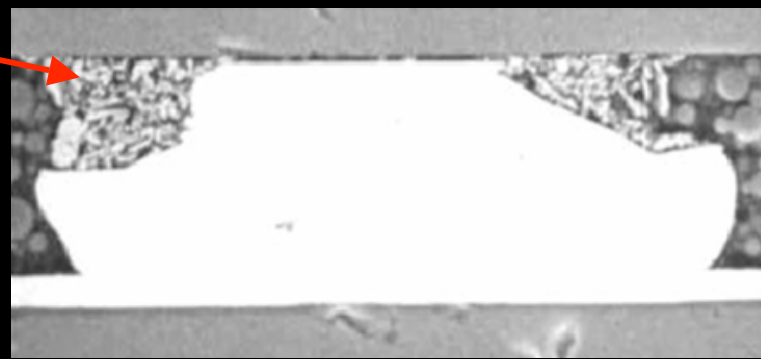
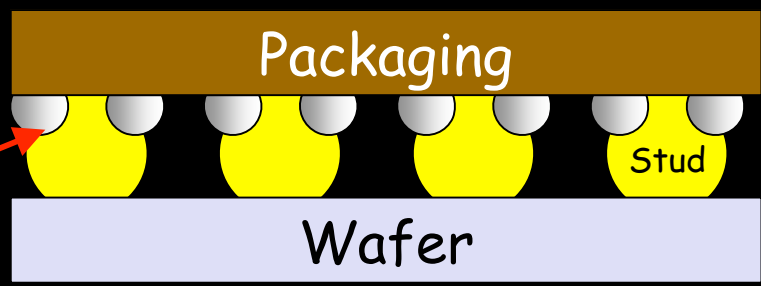
Three possibilities:

1. Conducting Silver Epoxy. High degree of bump height uniformity required. No limit on number of bumps. Low temp and pressure. Good success for large pads (>100 um). Work in progress for 50 um pads.
2. Thermo-compression. Typically, high temp and pressure: 300-350C and 150-200g/bump. Machine limit ~100-200 kg => Limits total number of bumps.
3. Thermosonic. Lower temp and pressure: 150C and 75g/bump. Limit on total number of bumps because of the limit on total deliverable ultrasonic power without breaking the chip.

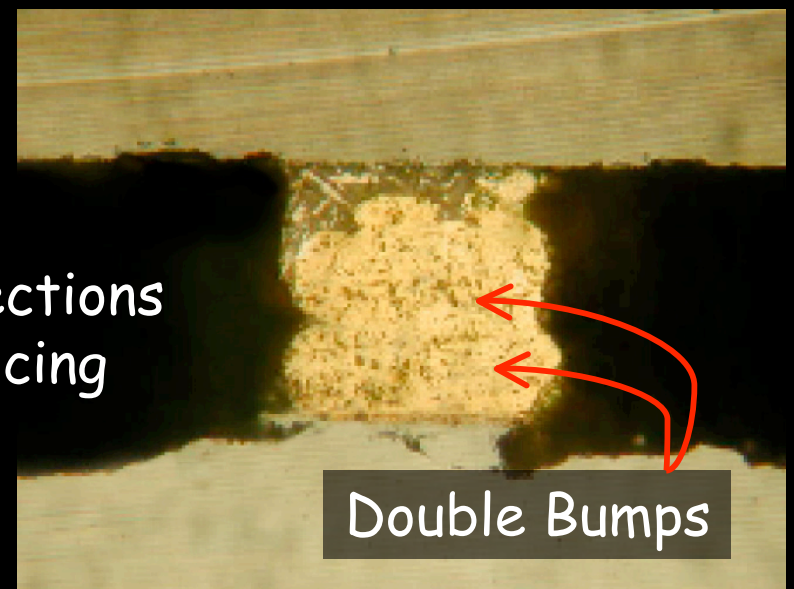
Adhesive Attachment

The tips of the studs are dipped into a conductive epoxy.
(Alternately, epoxy "dots" can be dispensed on the opposite wafer).

After a flip-chip alignment, the chips are compressed.



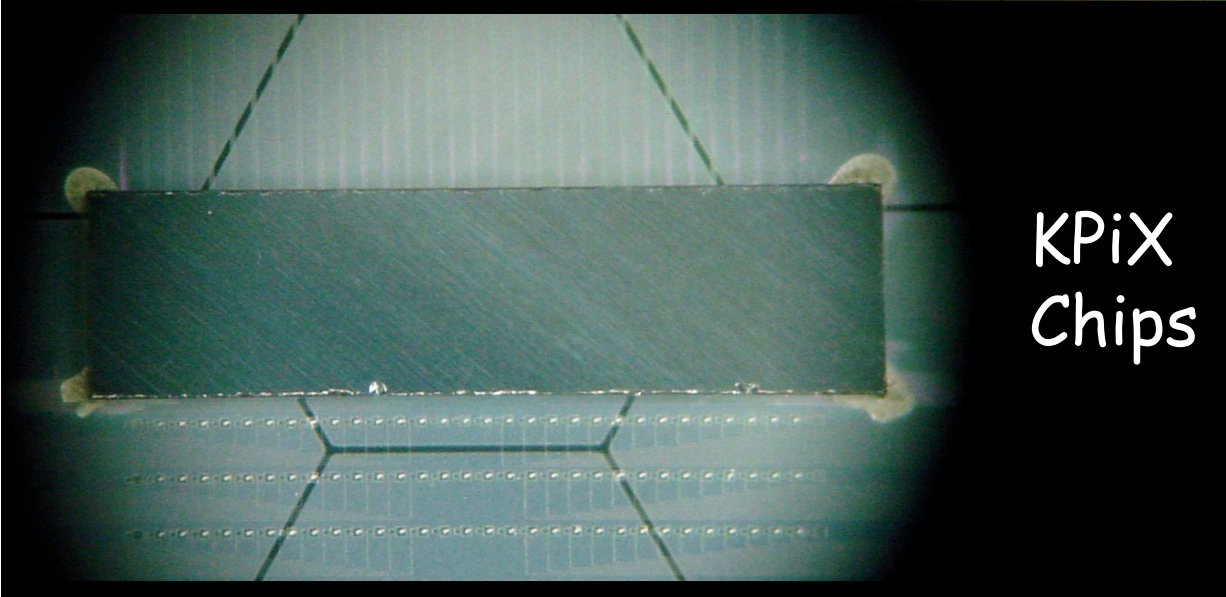
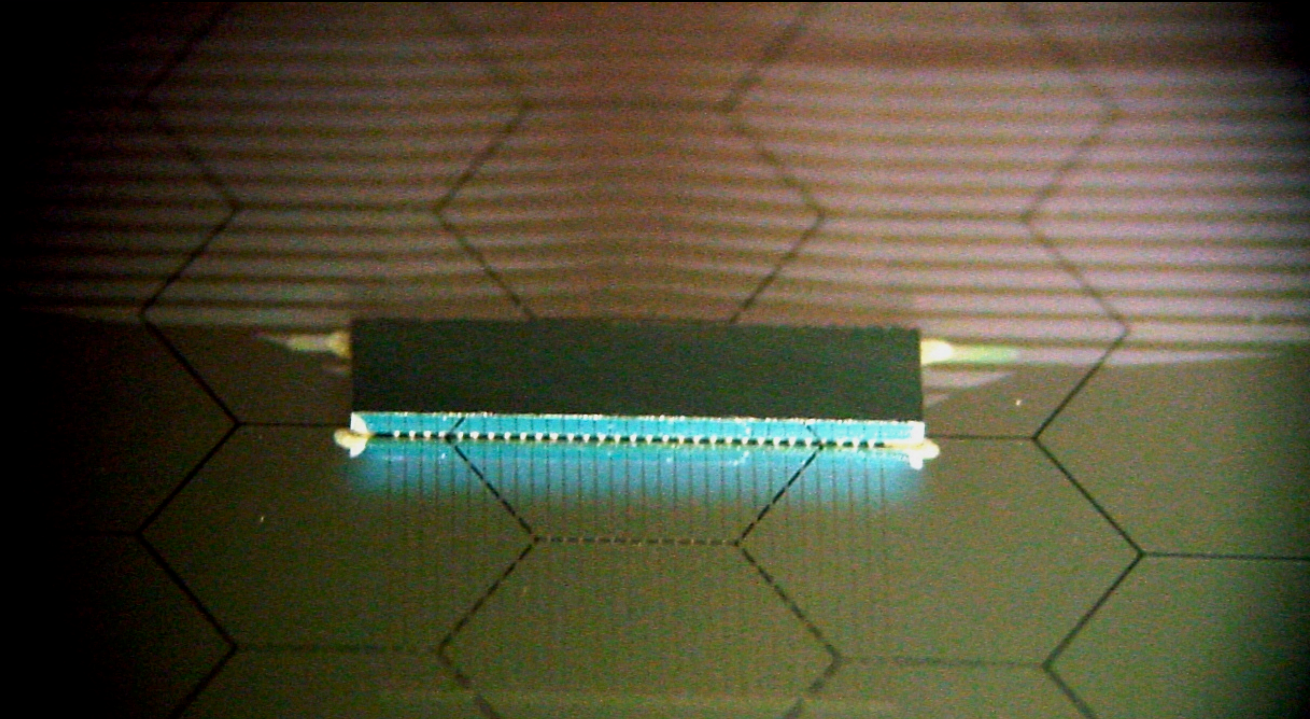
Cross sections after slicing



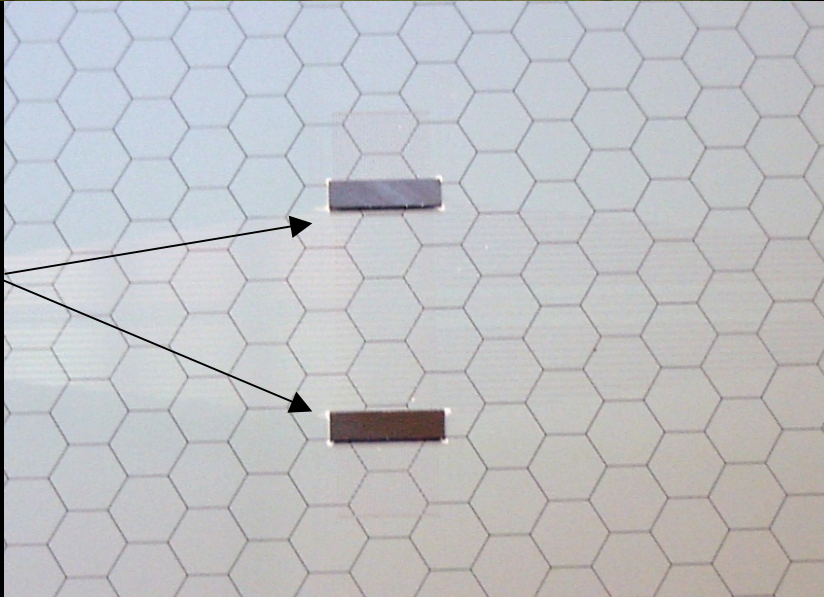
Double Bumps

Bump Bonding KPiX to Hamamatsu

Epoxy attachment is mechanically sound but yields high resistance per bump.

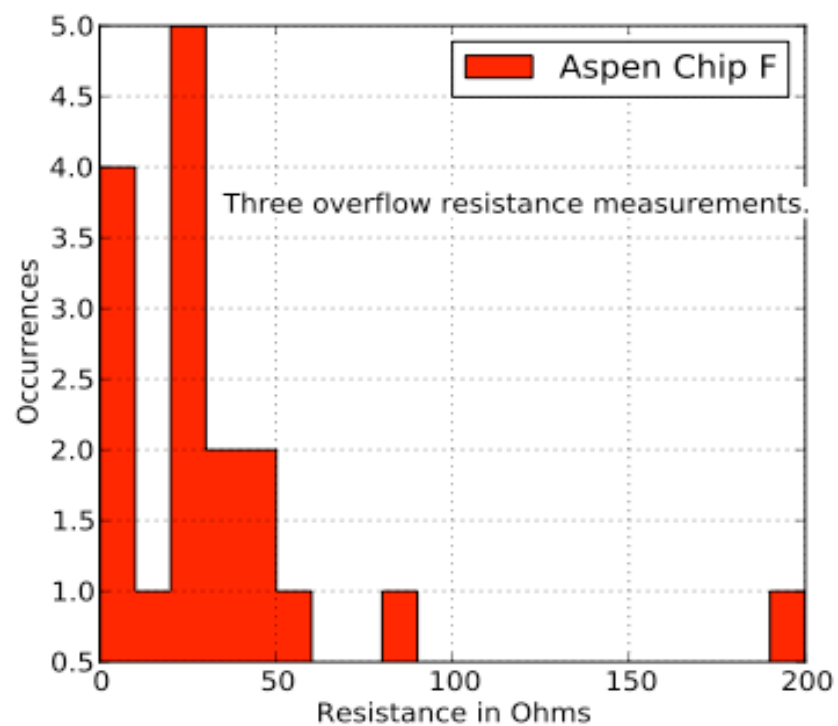
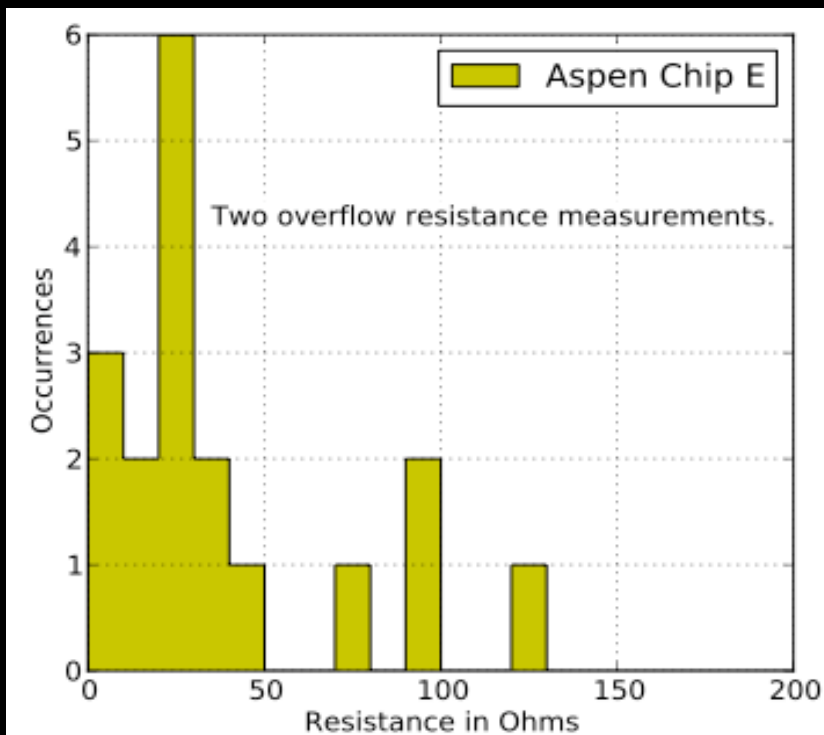


KPiX
Chips



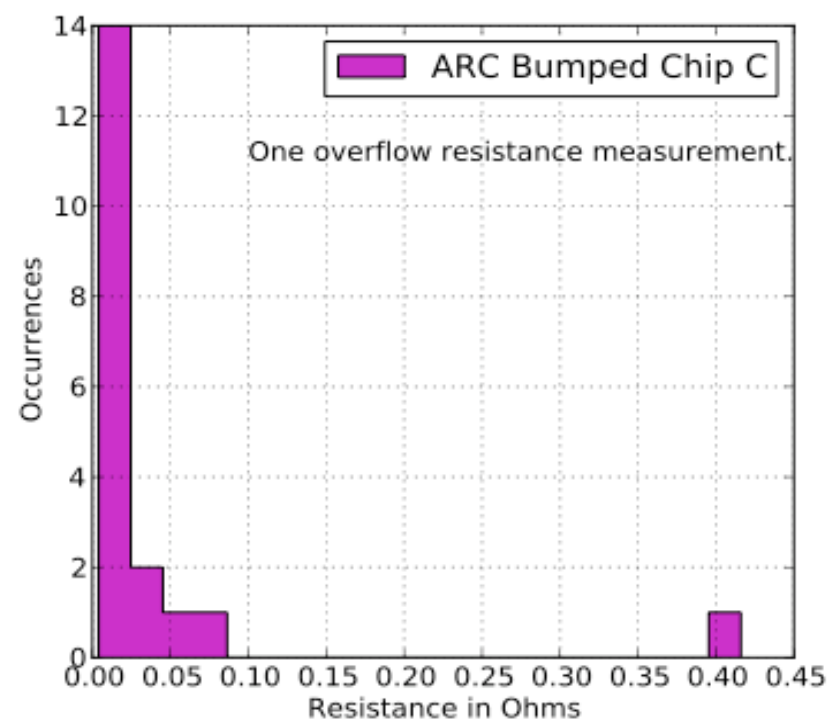
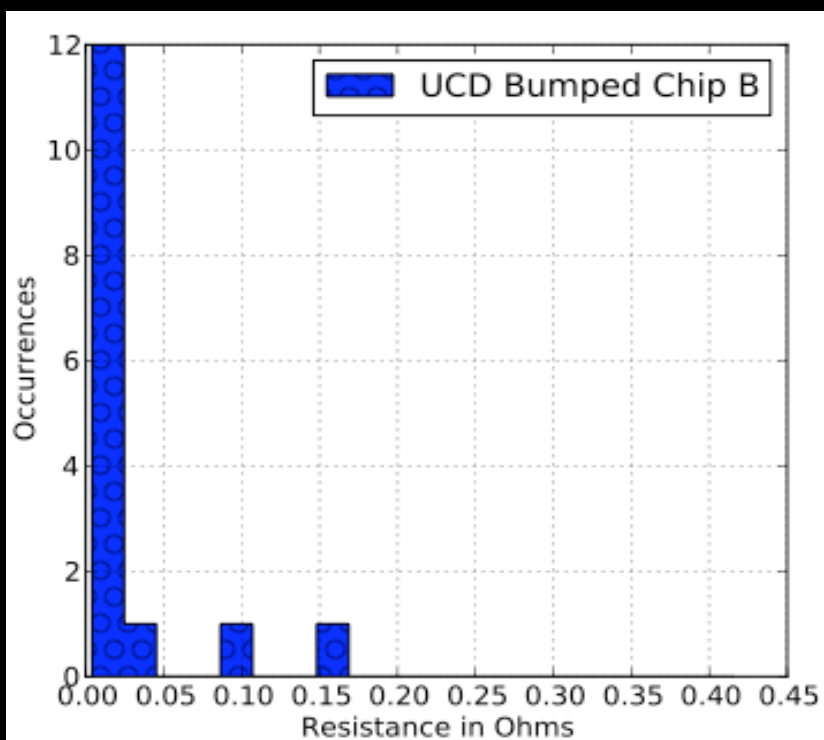
Au-Epoxy

High R!



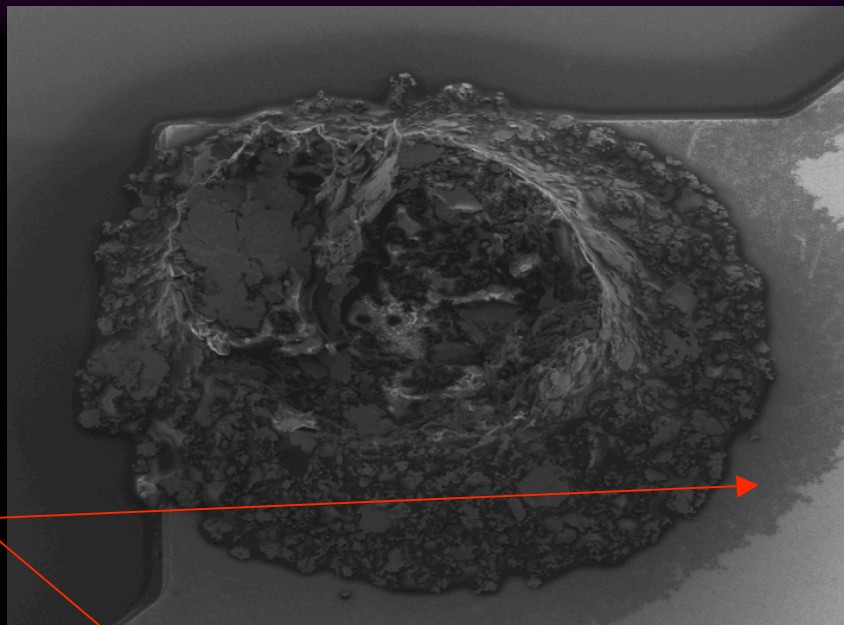
Au Thermo-Compression

Low R.

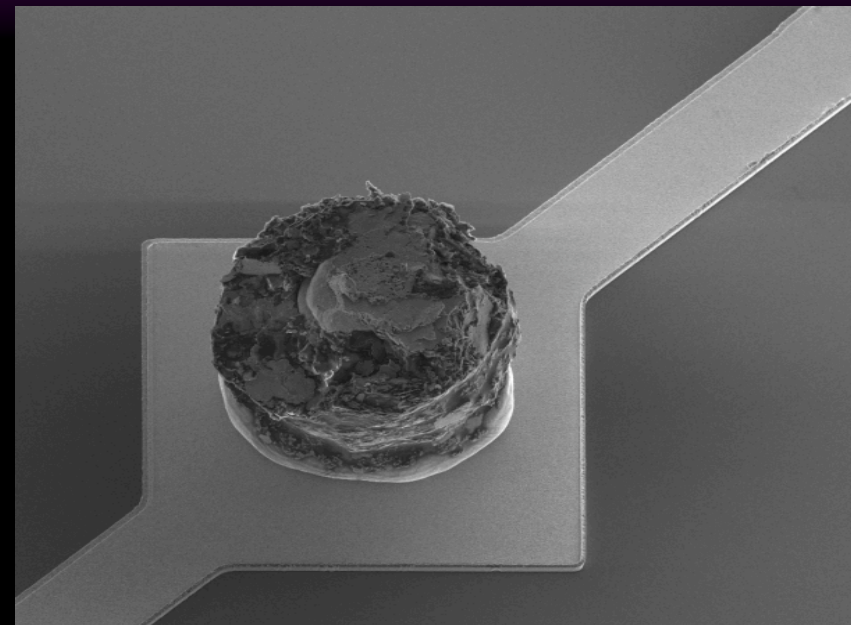


Bleed-out suspected for poor AU-epoxy contact

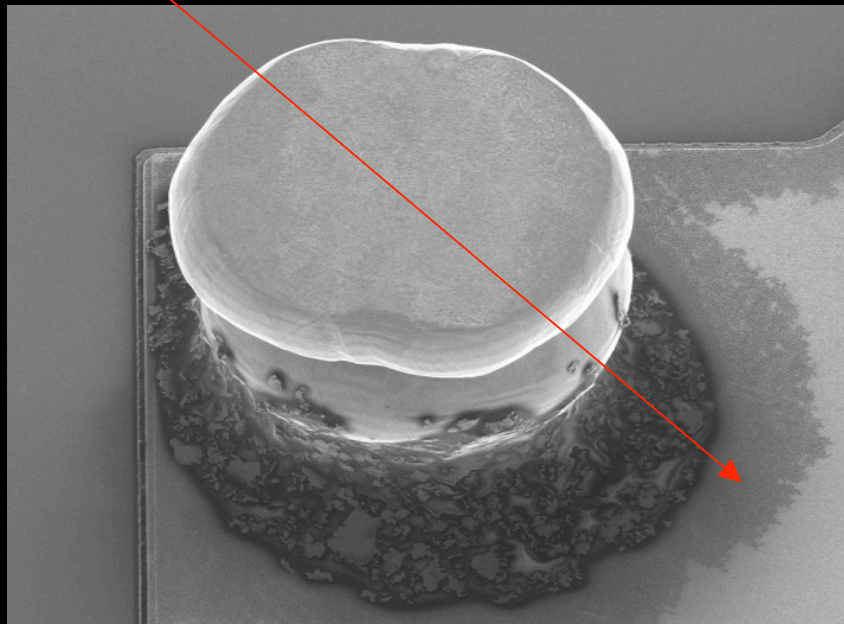
Bleed-out



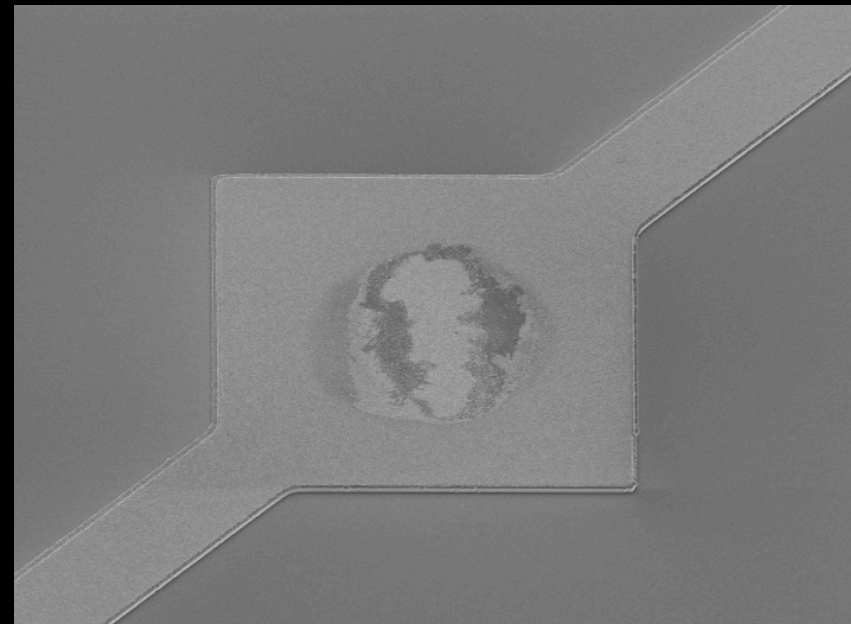
11/6/2009	Lens Mode	WD	HFV	HV	mag	spot	20 μm
12:15:15 PM	Field-Free	9.4 mm	136 μm	5.00 kV	2 187 x	2.0	Nova NanoSEM



11/6/2009	Lens Mode	WD	HFV	HV	mag	spot	30 μm
12:52:07 PM	Field-Free	6.6 mm	195 μm	5.00 kV	1 530 x	2.0	Nova NanoSEM

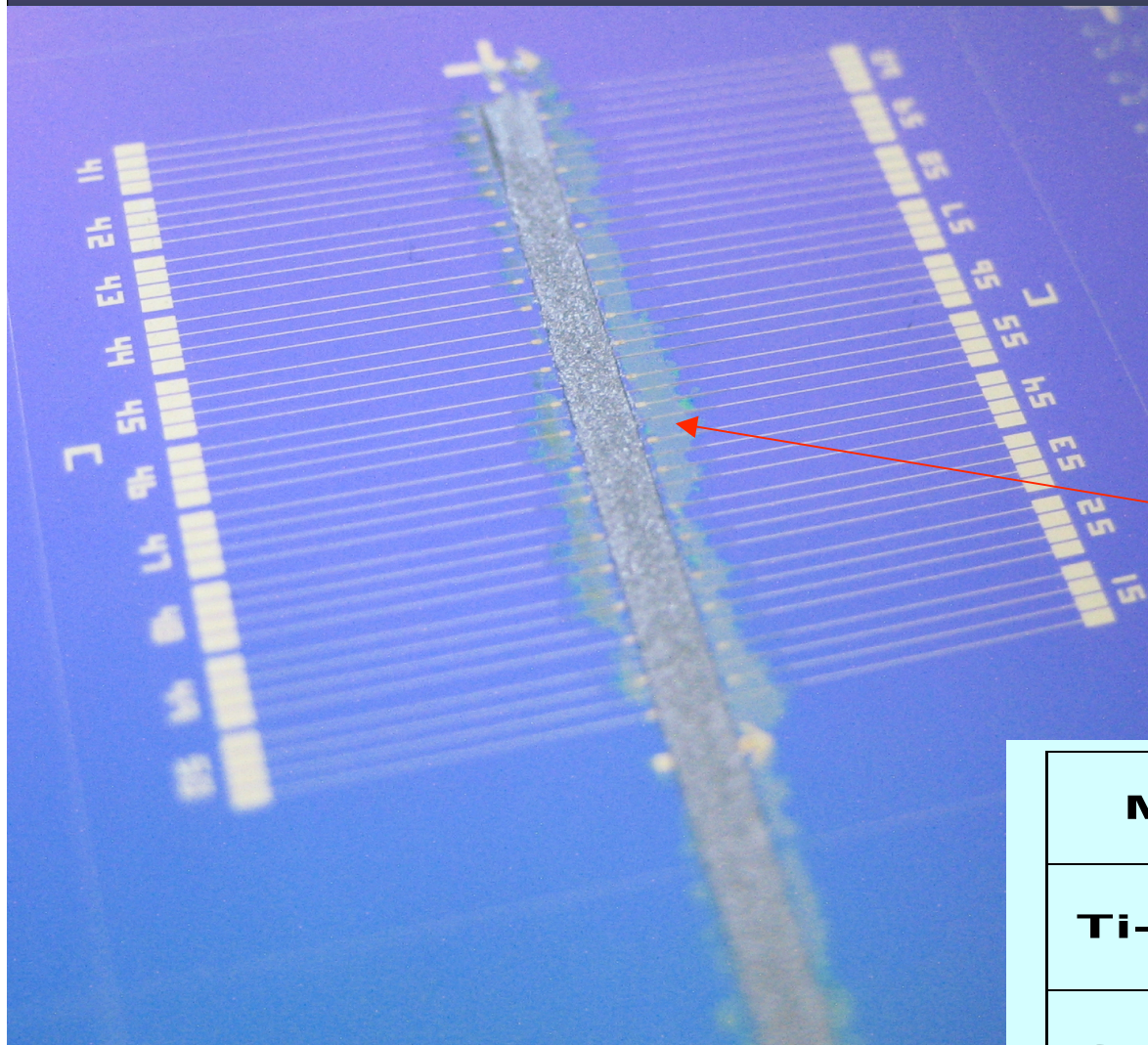


11/6/2009	Lens Mode	WD	HFV	HV	mag	spot	20 μm
12:26:36 PM	Field-Free	9.4 mm	126 μm	5.00 kV	2 375 x	2.0	Nova NanoSEM



11/6/2009	Lens Mode	WD	HFV	HV	mag	spot	30 μm
12:49:39 PM	Field-Free	6.6 mm	204 μm	5.00 kV	1 465 x	2.0	Nova NanoSEM

Under-Bump Metallization Studies



Bleed-out

Metal-Stack	Mean Resistance
Ti-W / Al	25 Ω
Cu / Cr / Al	8-10 Ω
Au / Cr / Al	10 mΩ

Z-Axis Conducting Adhesive

3M: 7303 ACF Adhesive

~45 μm particles

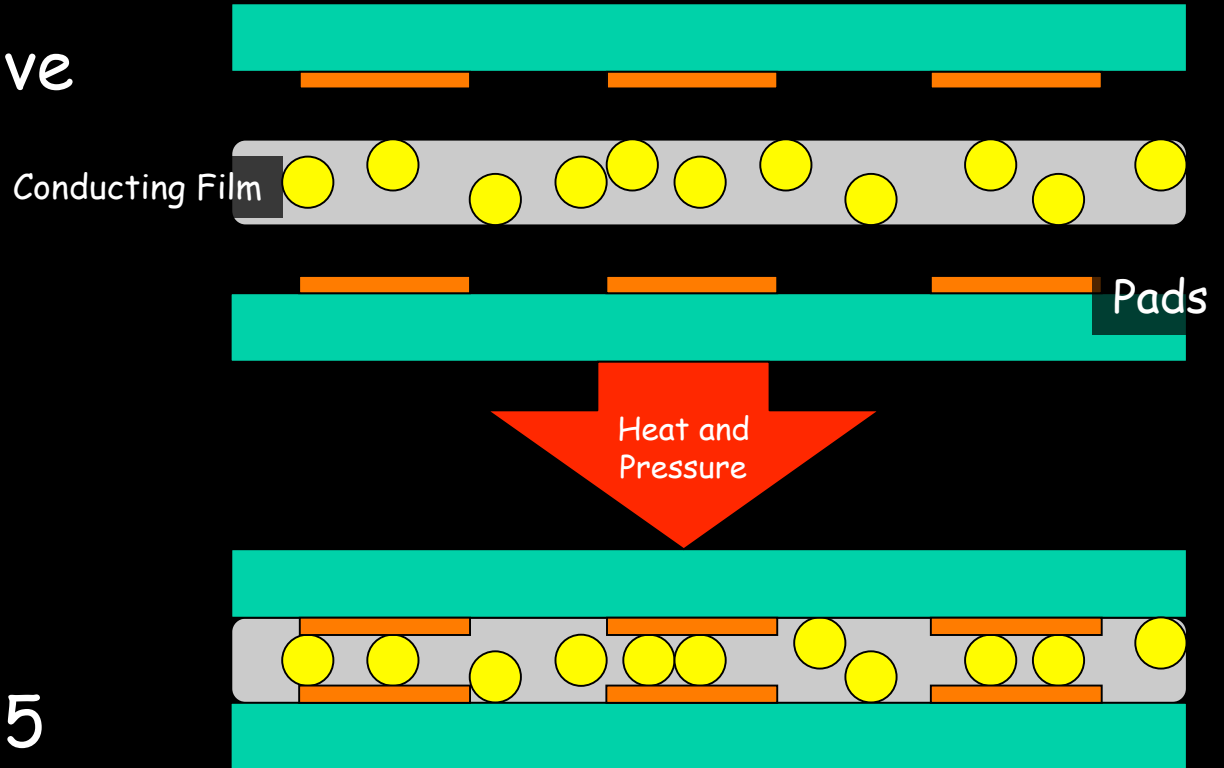
~75 μm film thickness

≥ 250 μm pad pitch

Bonding Conditions:

140°C @ 260 PSI for 25

secs



Cairns et al, SID Digest, 2001

Contact resistance $\leq 0.2 \Omega$ (for flex-cable to PC board).

$\leq 0.2 \Omega$ maintained after 80°C for 1000 hours or 25°C for 4 yrs

Flex cable to wafer attachment is not common => R&D.

Thermoplastic Conducting Adhesive

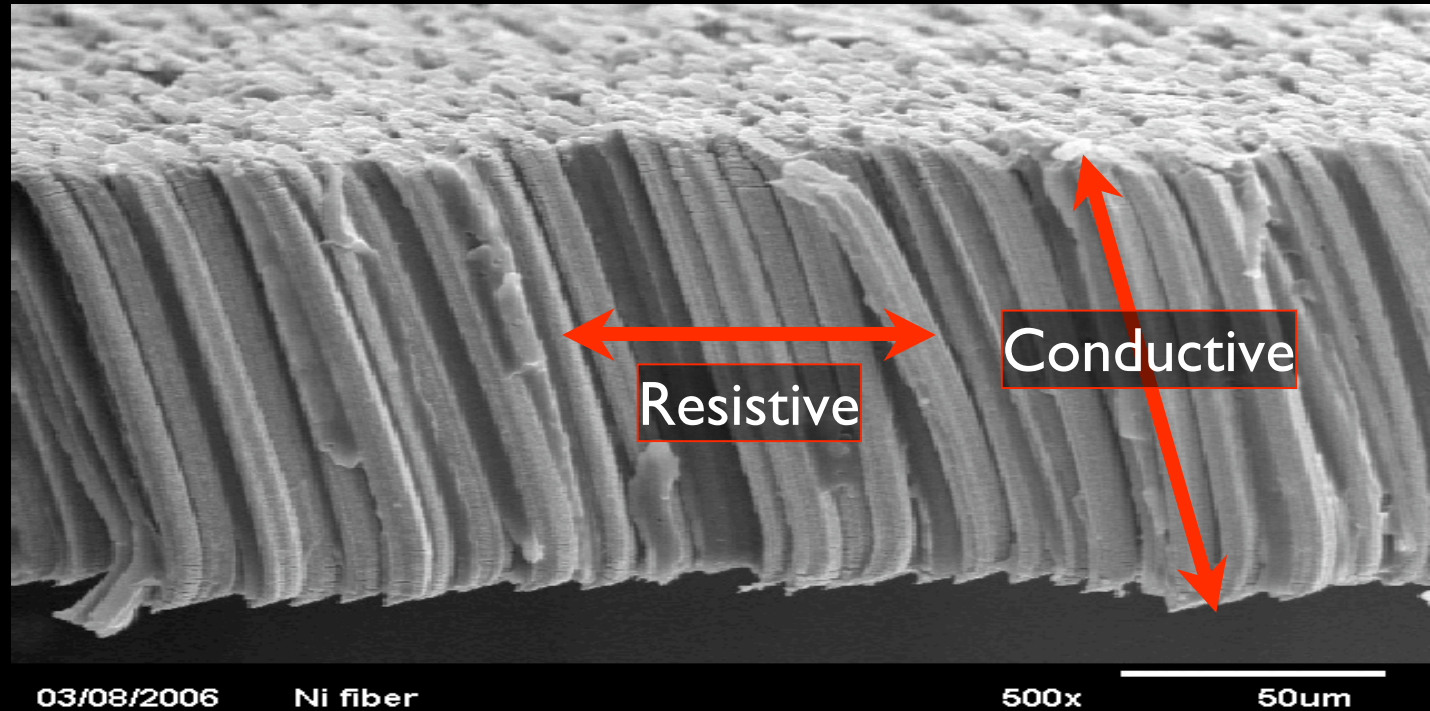
Btechcorp:

Metal fibers in a matrix
 $\sim 2 \times 10^7$
fibers/in²

Low Cure
pressure: 50 psi

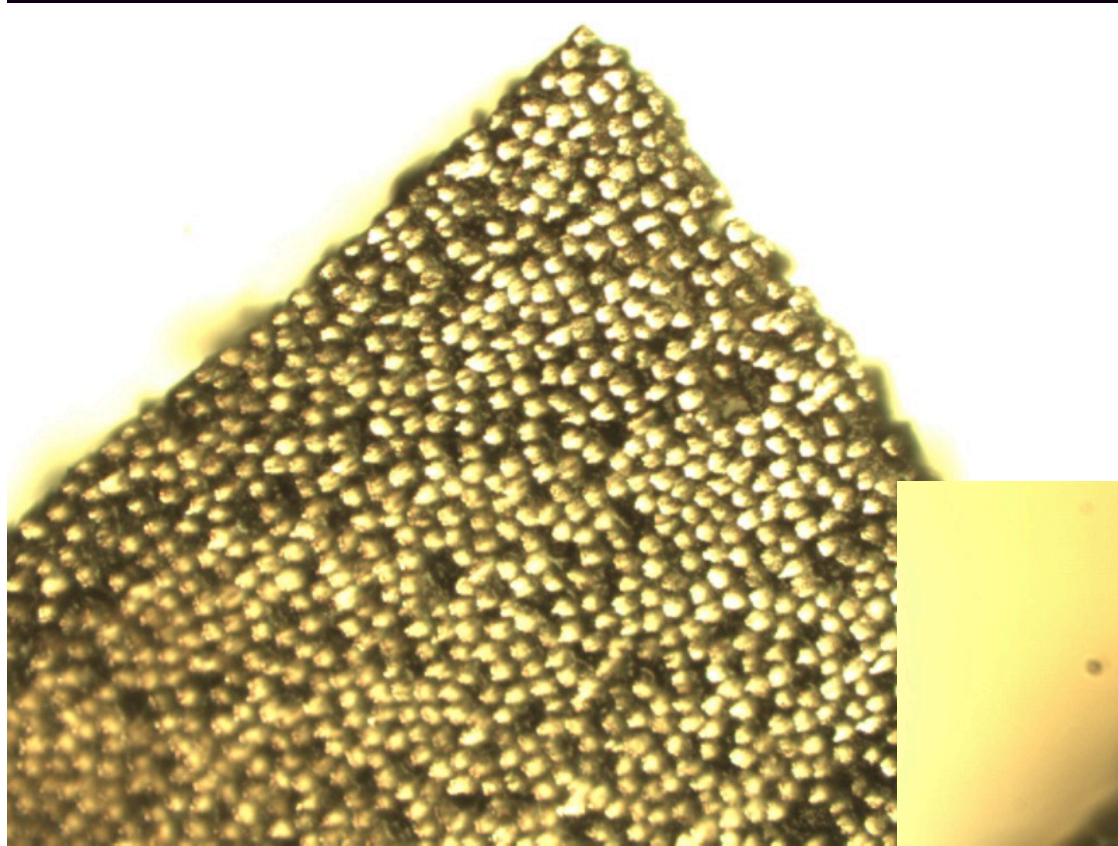
Thermal Conductivity \geq Cu. Smaller resistance
Cheaper.

Sub mm bonding has not been attempted widely. Needs R&D.

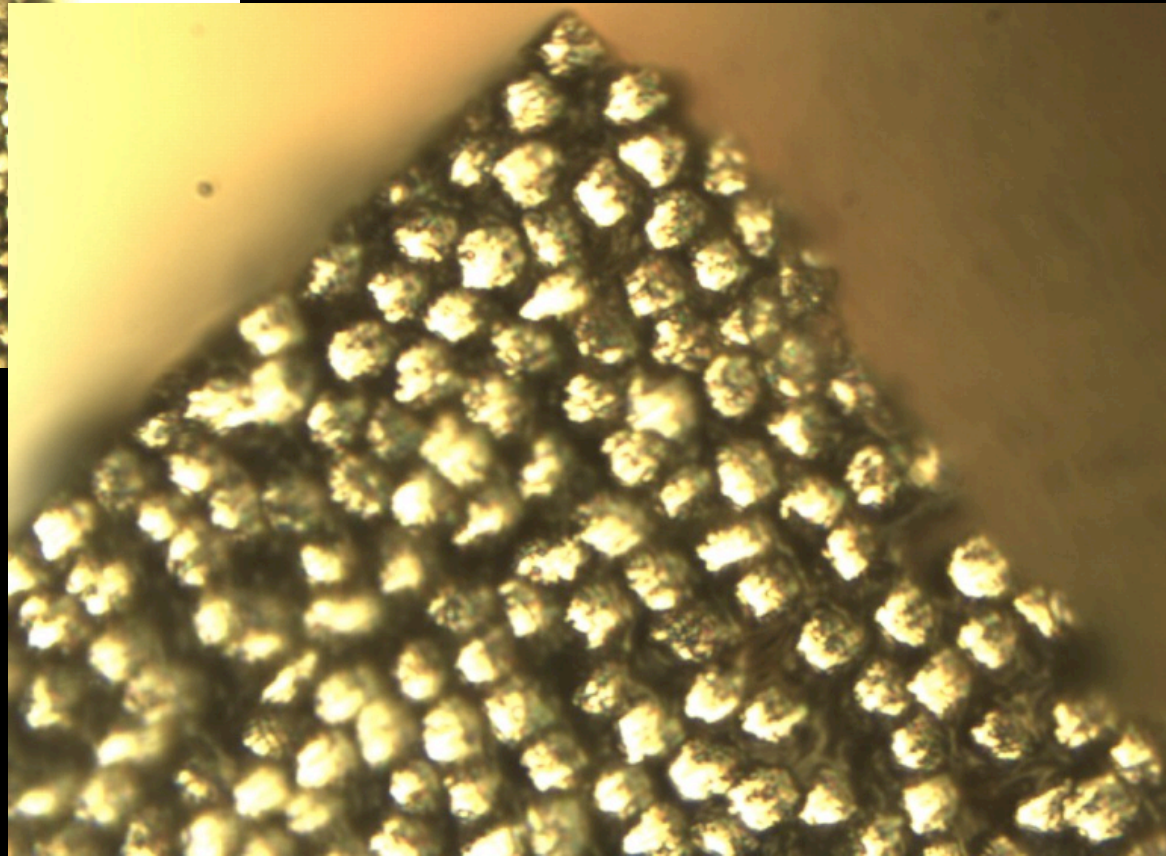


Nickel fiber structure.

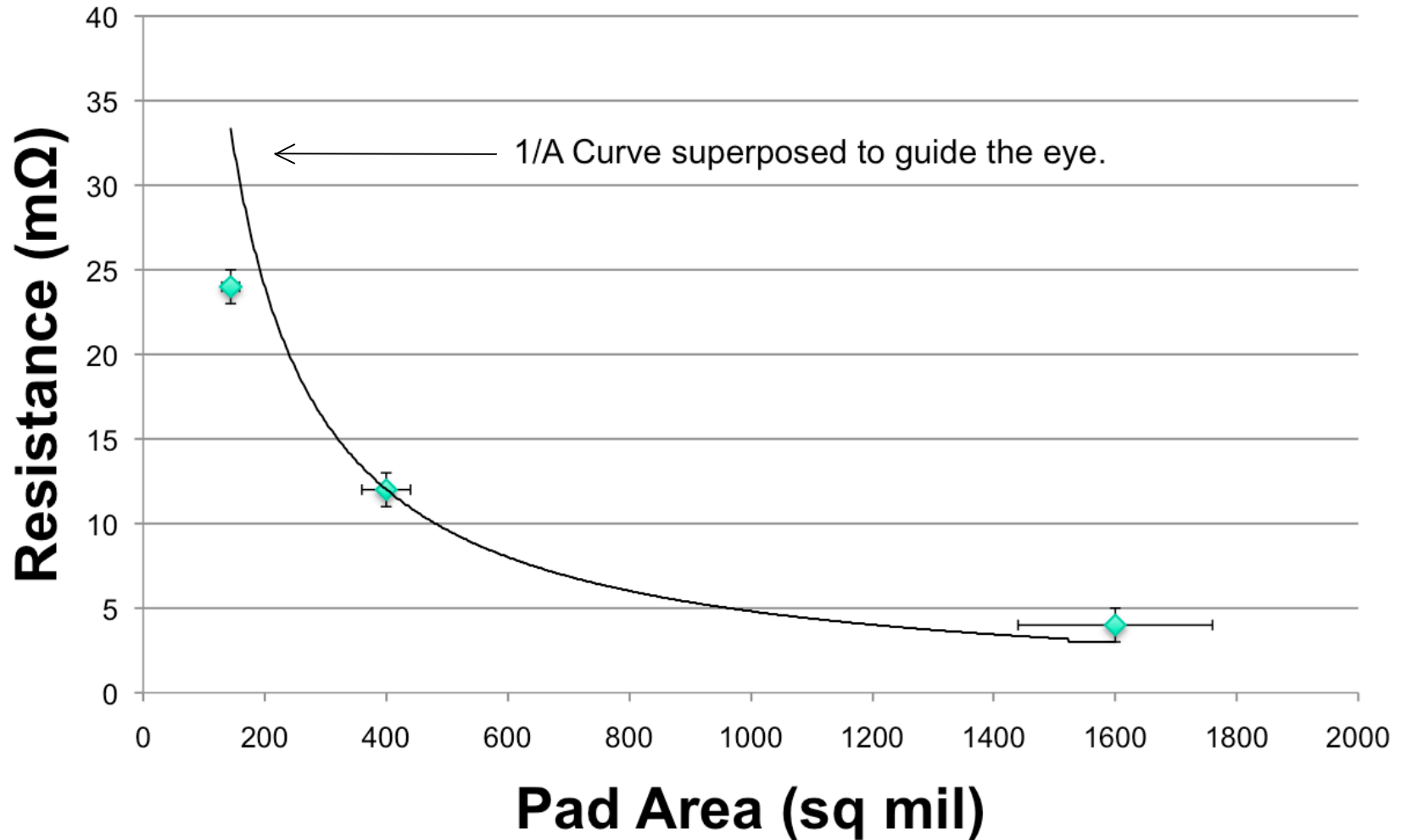
ACF Up Close



8 um fibers
close-packed array



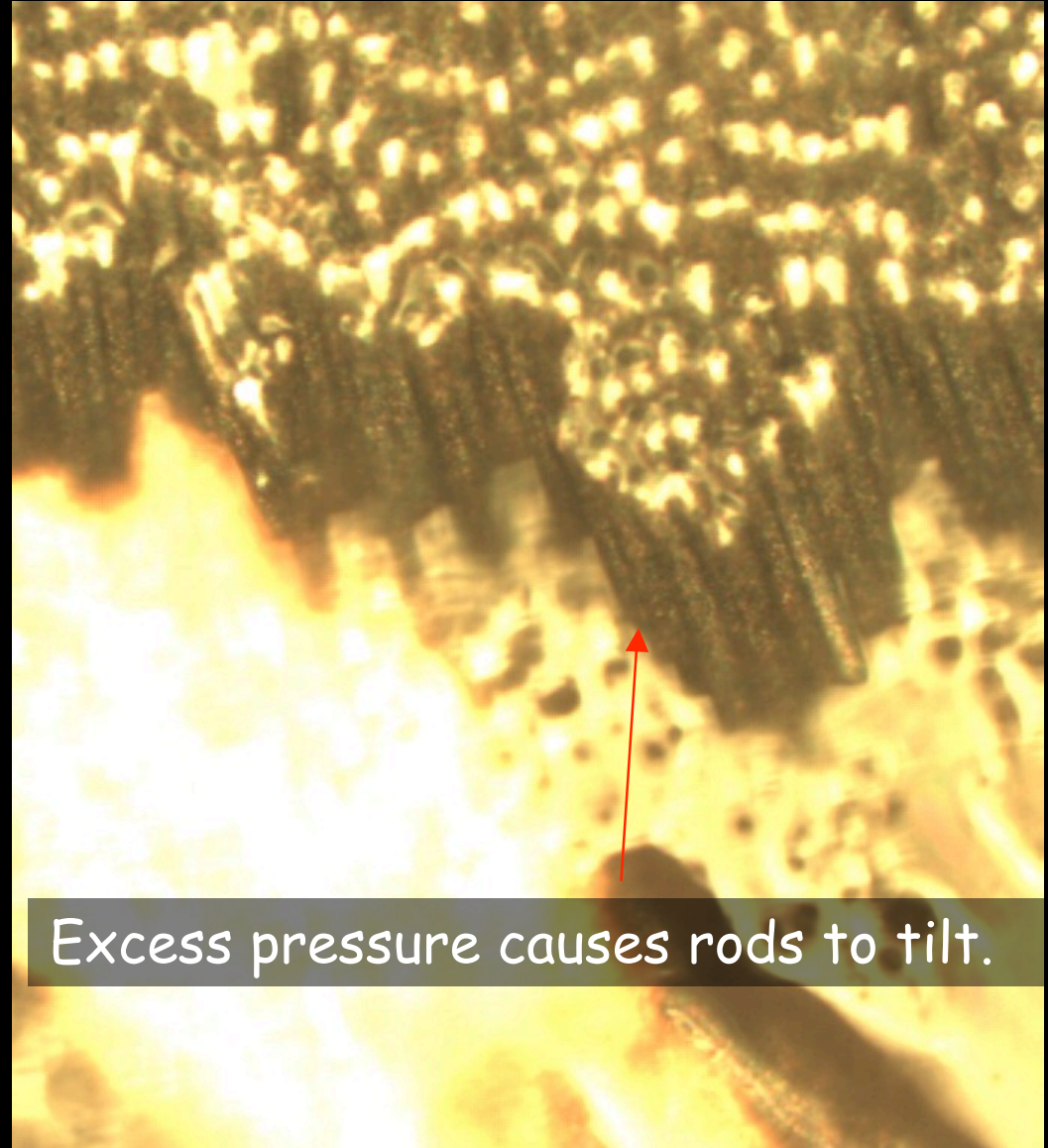
Initial Results



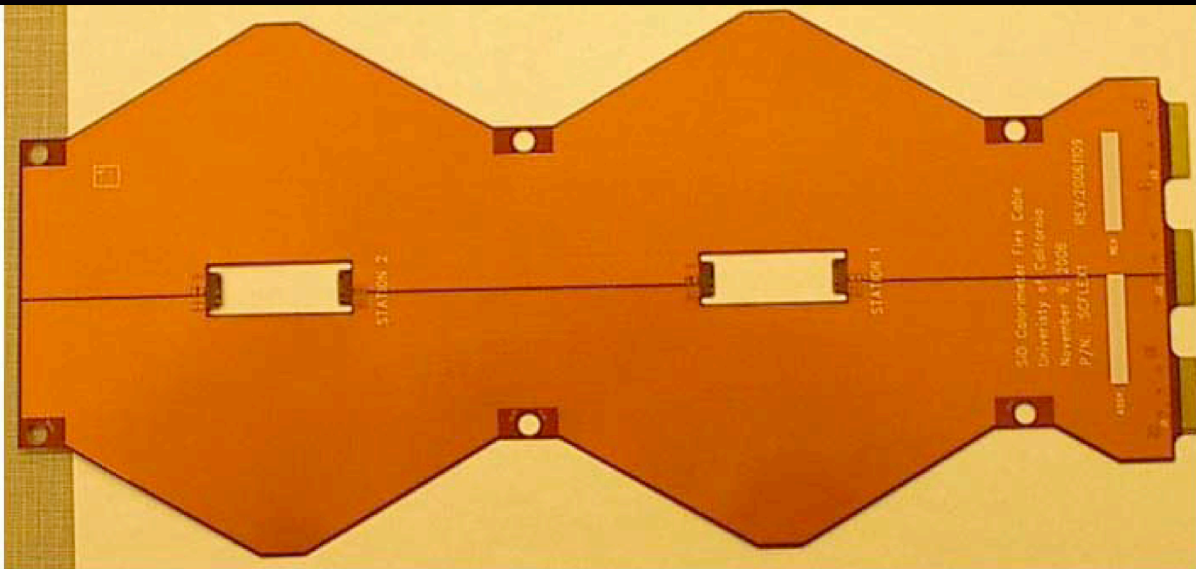
The results are promising. Goal for Flex Cable pads (100 sq mil) is ~ 100 m Ω , which is achievable.

Possible problems in ACF Bonding

- ACF bonded to transparent glass allows for observation under a microscope



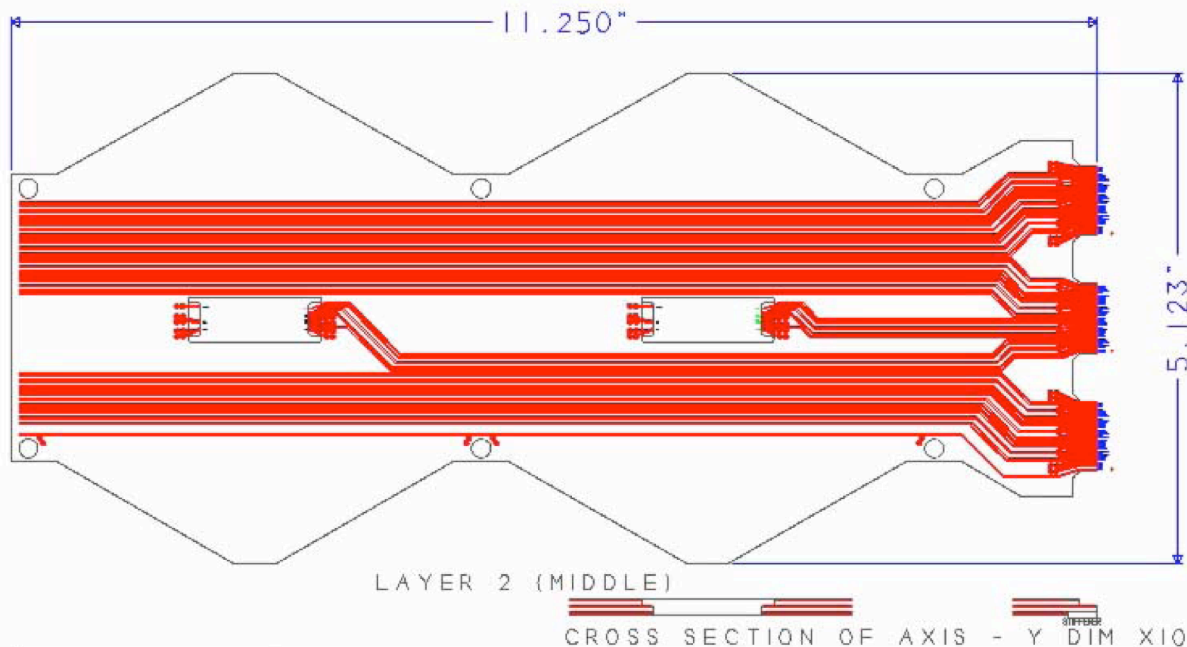
Readout flex cable for Si-W



2 chip stations

Buried digital signal layer
between power and
ground planes

Two "lips" per KPiX from
the buried layer for
attachment to silicon
wafer.

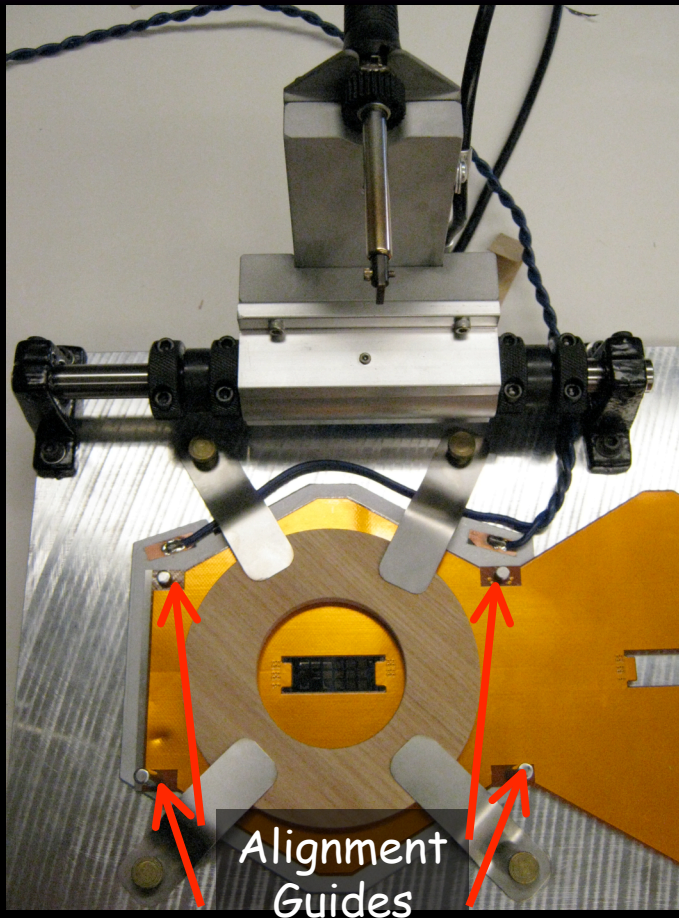


UCD PHYSICS

TITLE SILICON CALORIMETER
FLEX CABLE PROTOTYPE

ENGINEER: BRITT HOLBROOK, P.E.
DATE: 08/09/08

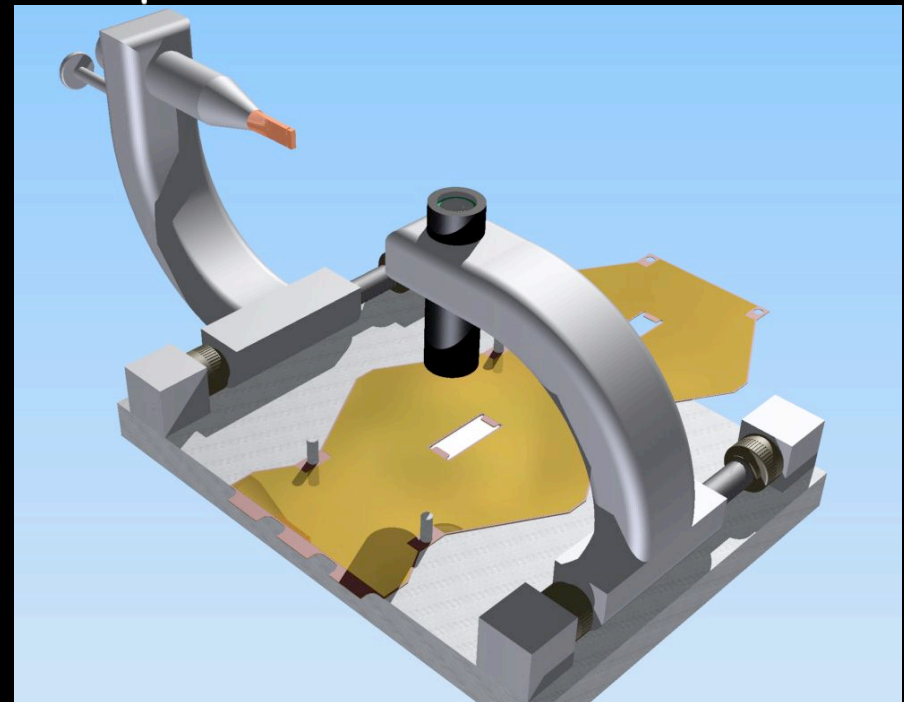
Custom Alignment and Bonding Jig



Swinging heating arm.

Adjustable Factors:

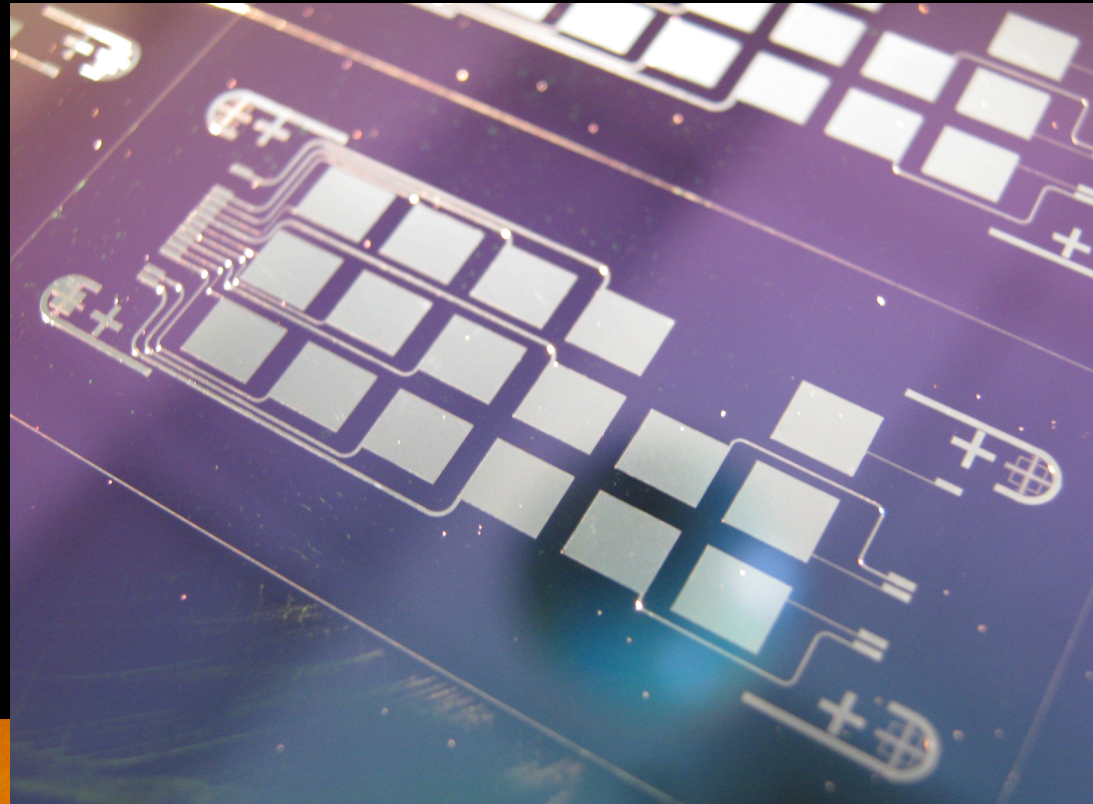
- Preheat wafer and flex cable.
- Tip position
- Tip angle
- Tip temp
- Pressure



ACF manufacturer supplies ideal parameters. Testing requires adjustment toward them.

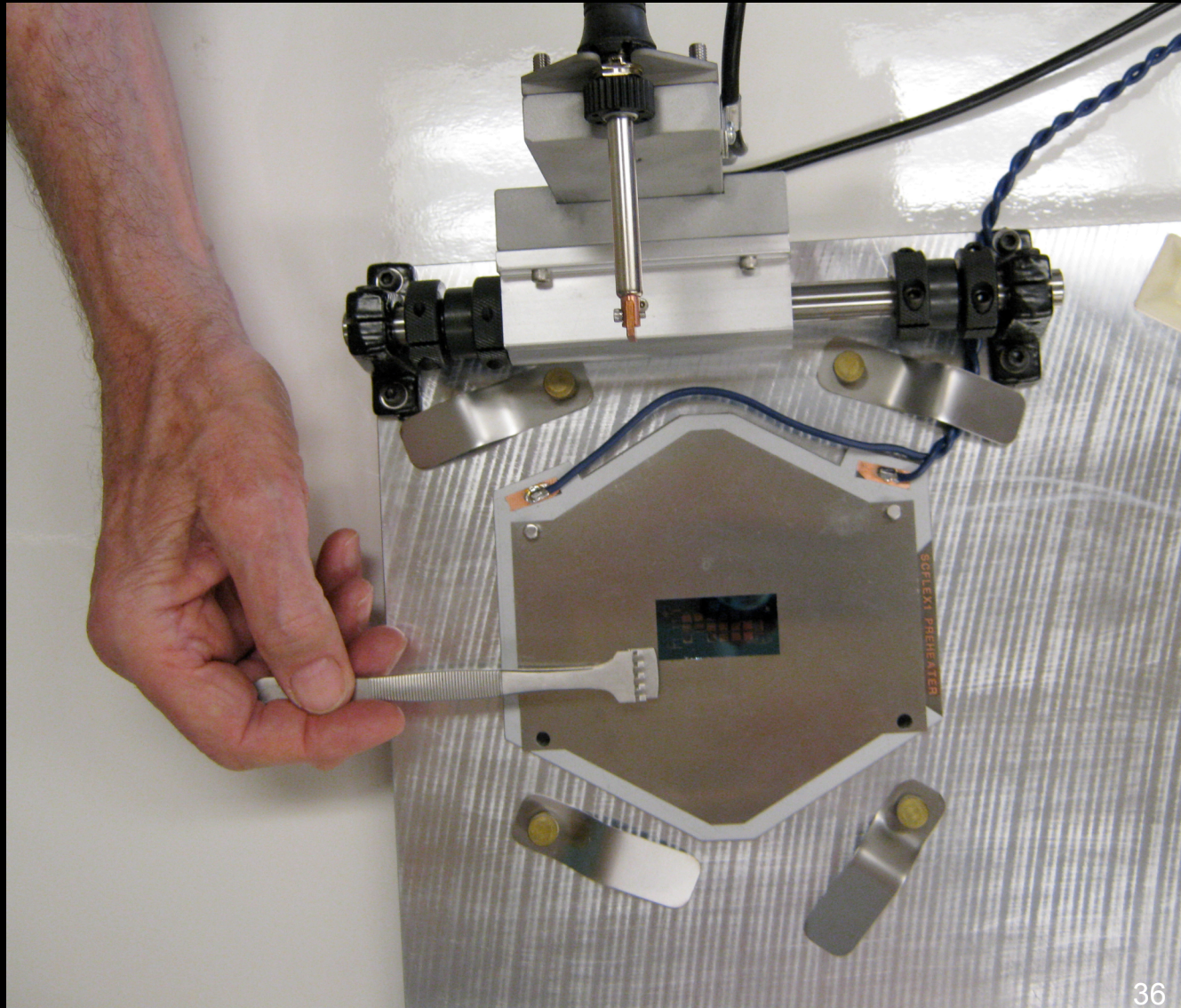
Test Wafer

- Hamamatsu wafers too expensive to test on.
- Ti-W test wafer mimics the read portion of the Hamamatsu wafer.
- Large pads for read out where bump bond positions would be.



Wafer alignment via EDM shim

- A metal shim has been produced using precise electrical discharge machining
- Jig alignment posts hold metal shim in place.
- Shim holds wafer in cutaway.
- Guide posts align all pieces automatically.

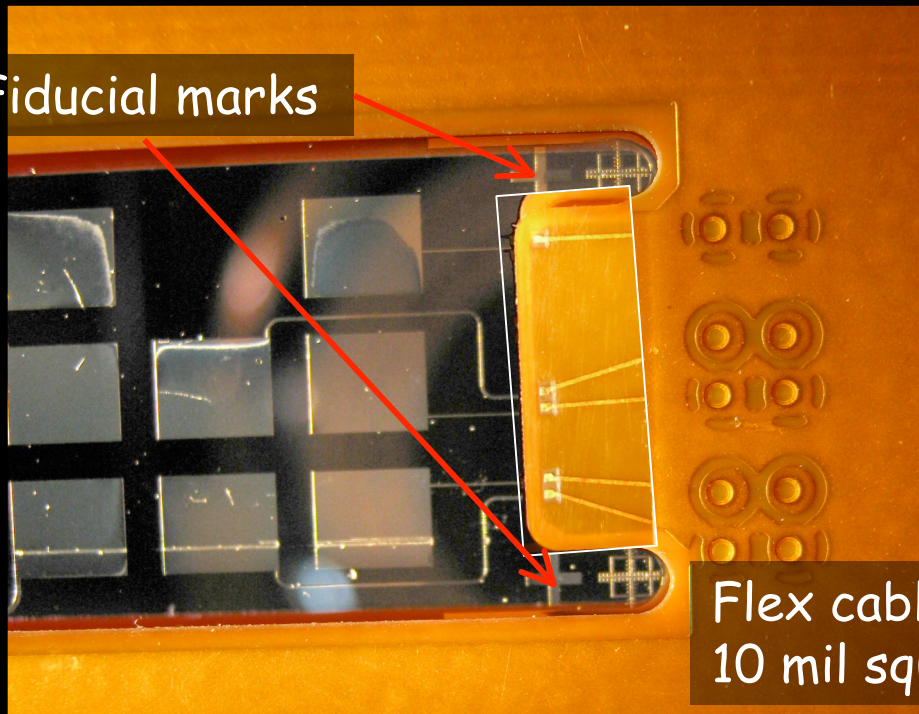


Precision Alignment

- ACF does not need alignment.
- Flex cable and wafer do.



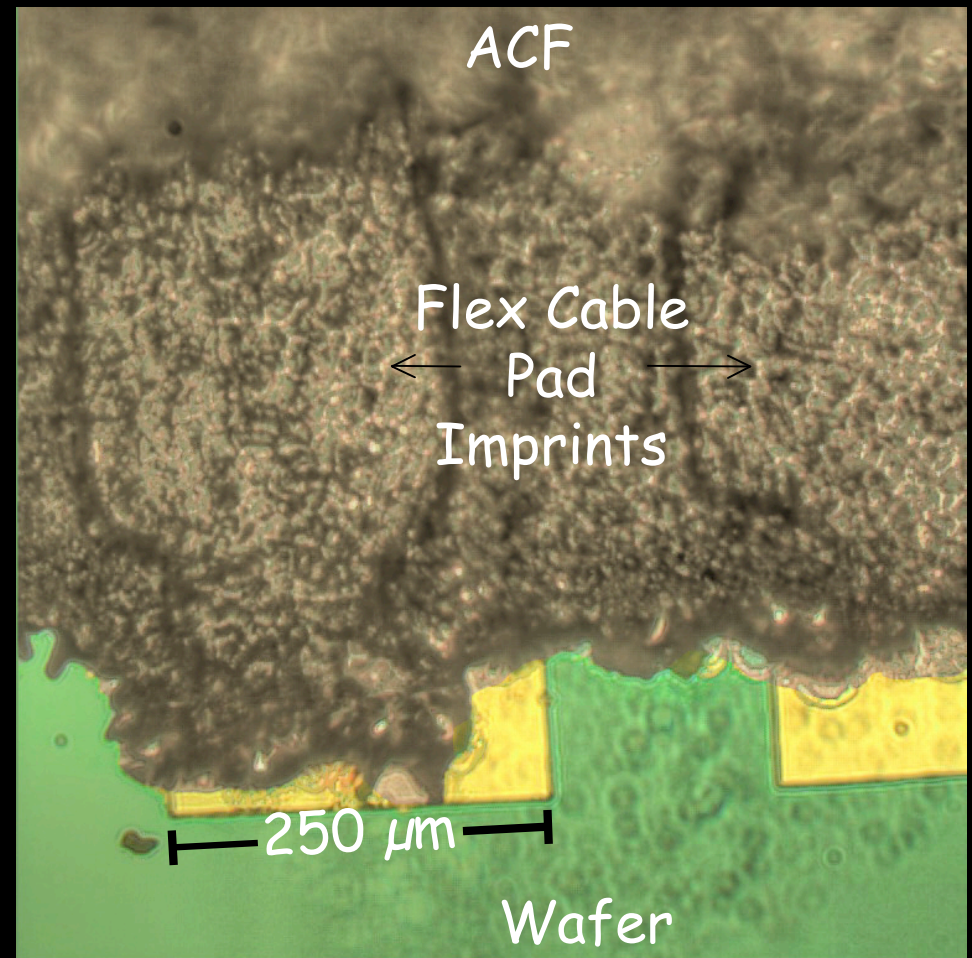
Fiducial marks



Flex cable pads revealed.
10 mil square pads

First results from ACF Attachment

- Flex cable and wafer do.
- Flex cable, jig, and wafer all align to ± 20 microns.
- Full cable to be bonded in stages.

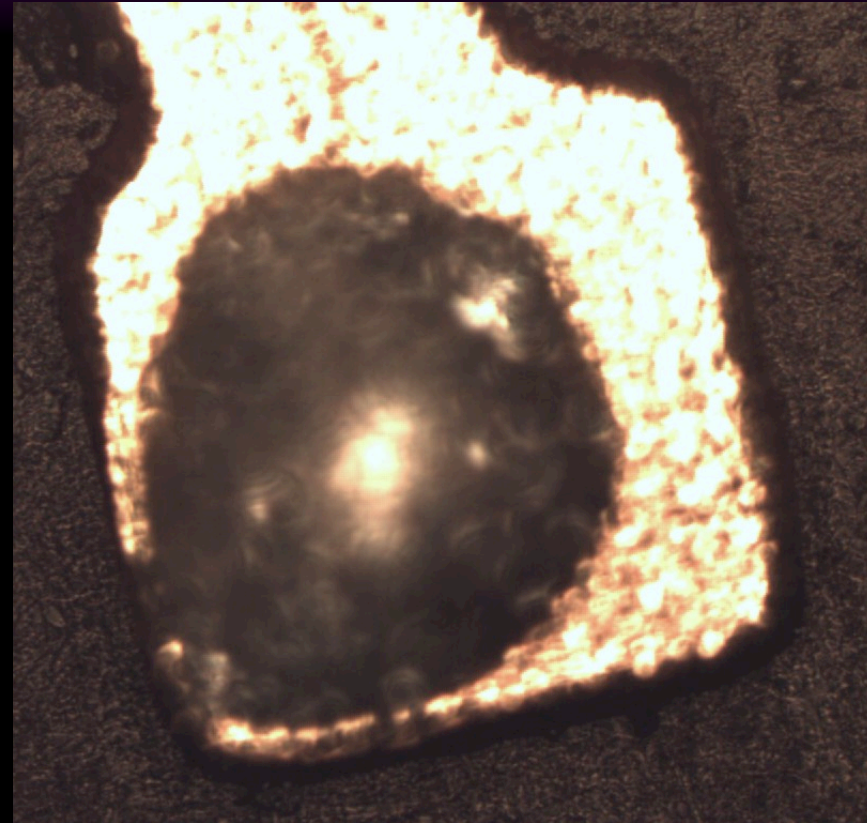
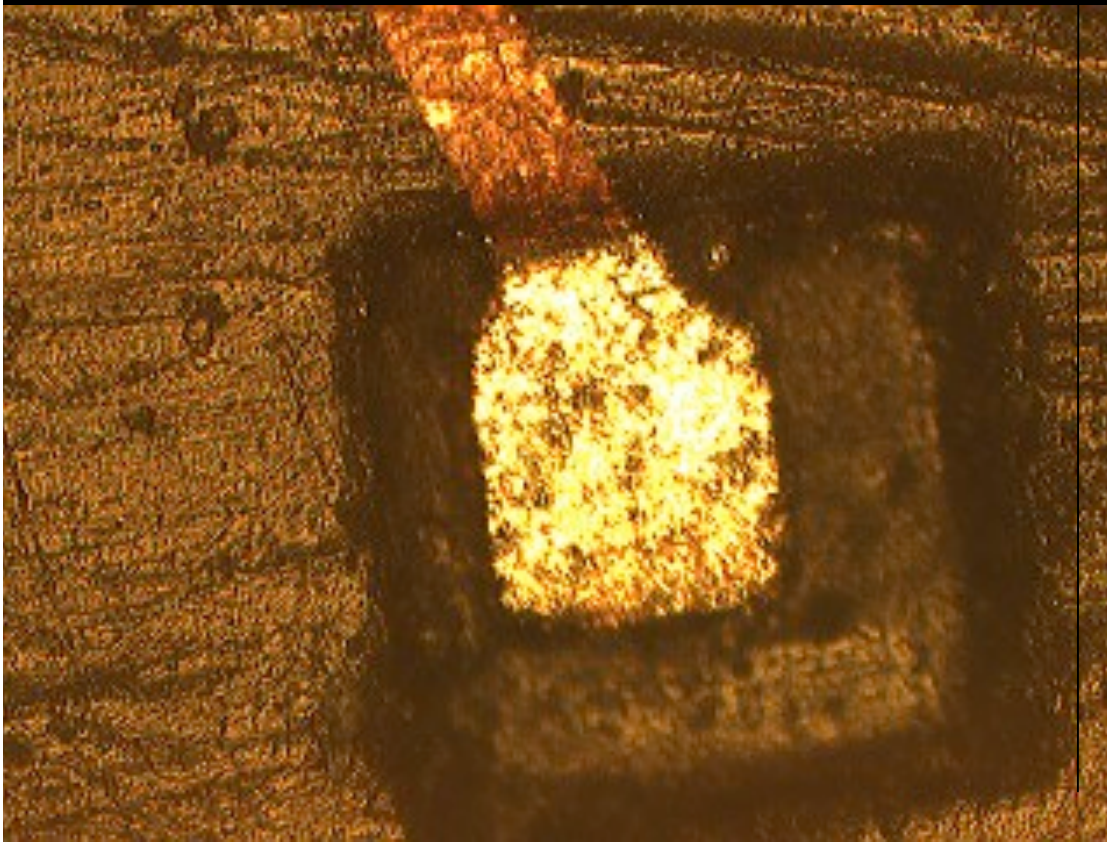


Indentation on ACF from Flex Cable pads after detachment of bonding surfaces.

Silver Epoxy

Groups of pads in flex cable reside
~20 μm deep in overlay well.

Silver epoxy can be applied using
stencils (holes in shim metal).



Solder balls "pick-n-
place" being investigated.

Summary

Ongoing work for Specific Detector R&D

- Flex Cable Development
- Gold Stud Bonding
- ACF attachment
- Flip-chip bonding
- Solder Ball and epoxy stencils

Generic R&D for Interconnect issues

- Single die photolithography for Indium (PDMS substrate)
- Under bump metallization studies
- Smart flex cables
- ACF and conductive epoxy evaluations