3D Technology for Intelligent Trackers

Ronald Lipton, Fermilab WIT 2010

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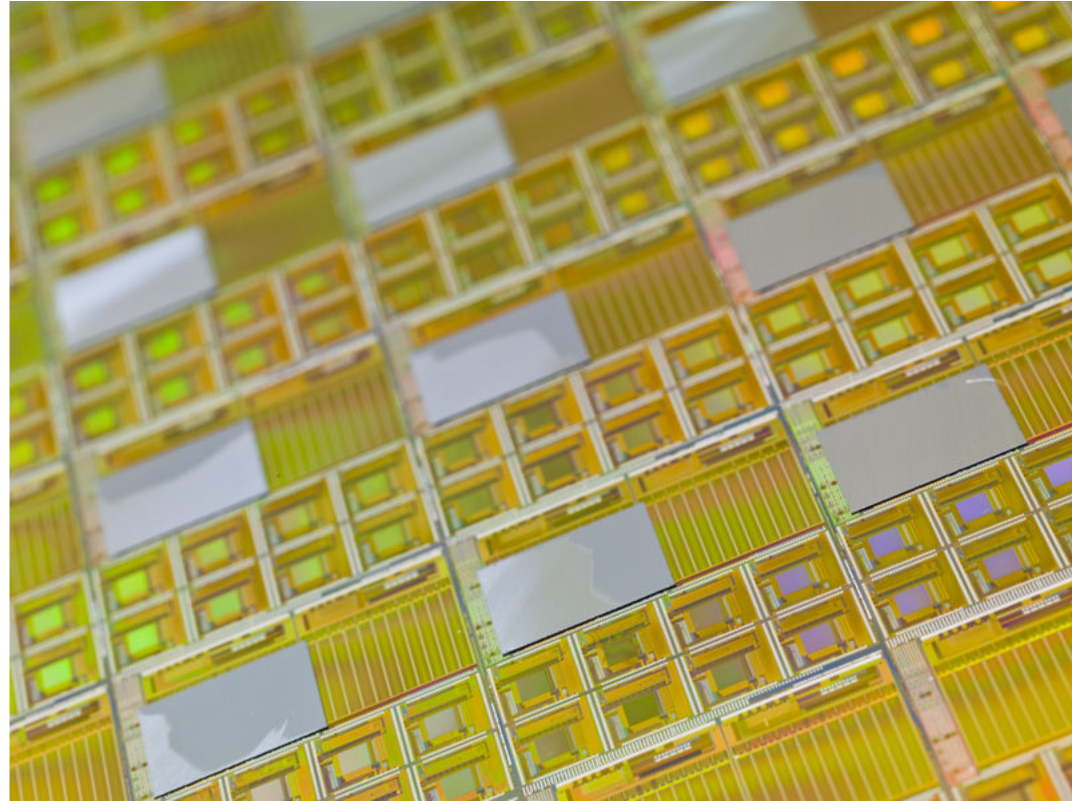

Oxide bonded 100 micron thick sensors on FPIX (BTeV) wafer

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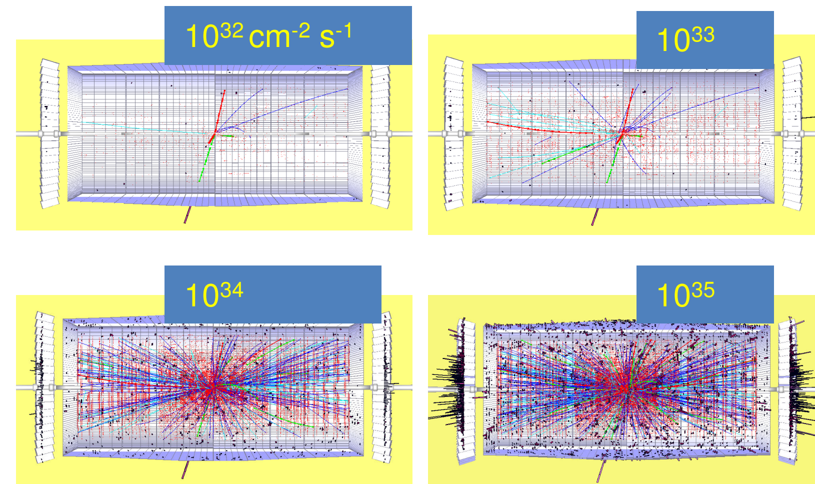
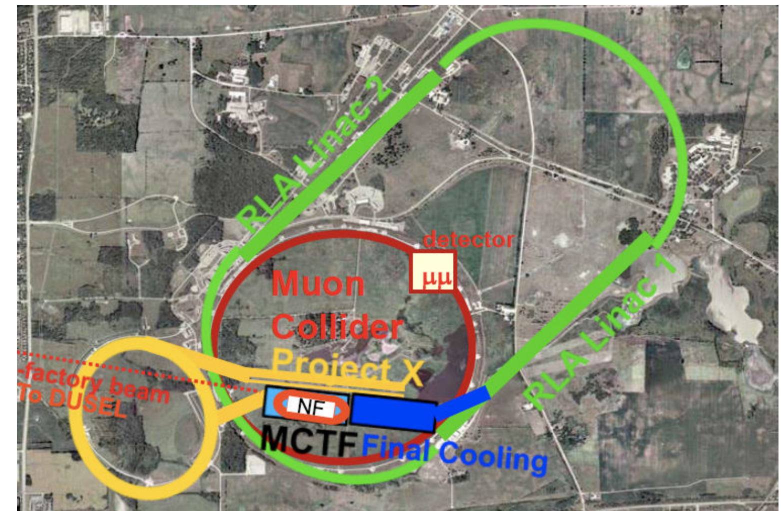
Future Detectors

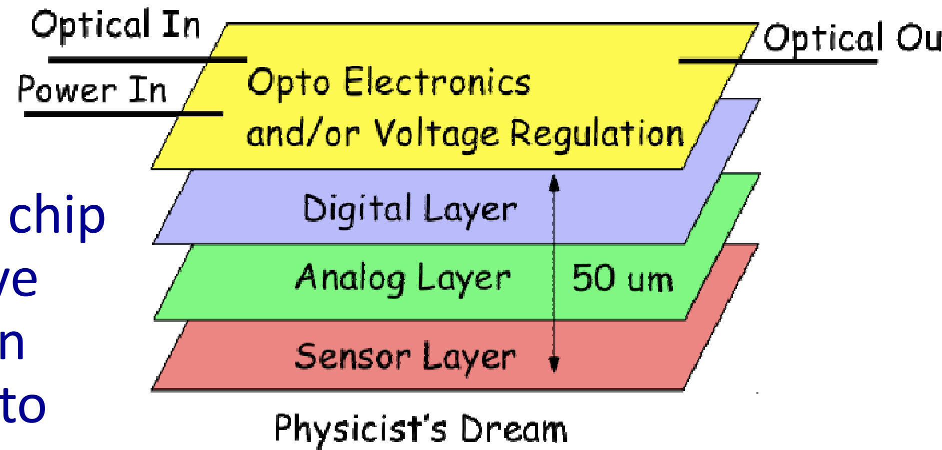
- The next generation of detectors will face unprecedented challenges
- ILC Vertex Detector
  - Superb impact parameter resolution ($5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$)
  - Transparency (~0.1% X0 per layer)
- Muon Collider
  - 1-3 TeV muon collider on FNAL site
  - Many accelerator issues
  - Substantial detector and radiation backgrounds
- CLIC
  - ILC + ns time resolution
- SLHC
  - 200-400 int/25 ns crossing
- X-Ray Imaging
  - Variety of challenges – timing



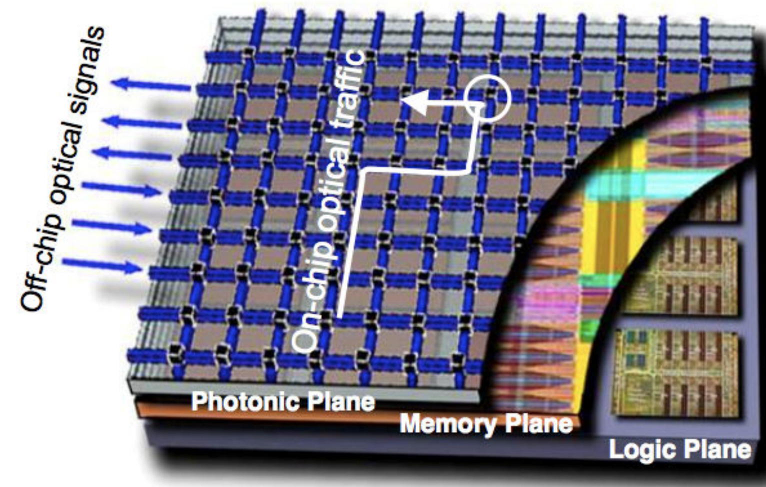


It is crucial that we capitalize on the impressive innovations coming from the electronics industry to provide tools for the next generation

3D Technology



- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- This is a major direction for the semiconductor industry.

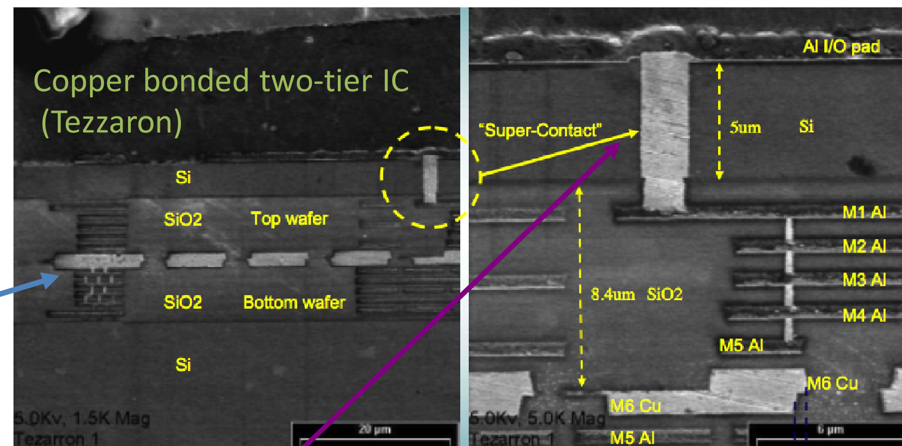


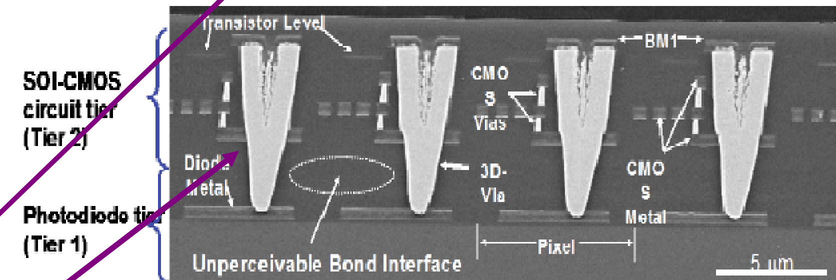
IBM/Cornell/UCSB Study – vision of 22 nm 10Tflop 3D chip (2018)

3D Ingredients

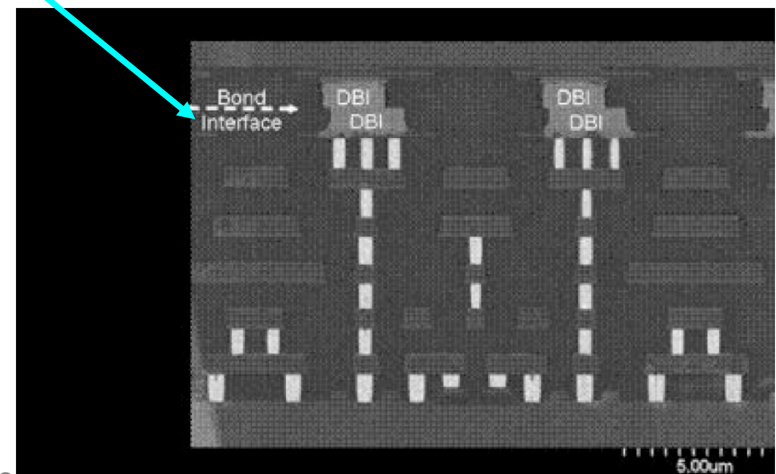
Suite of technologies based on:

- 1) Bonding between layers
  - Copper/copper
  - Oxide to oxide fusion
  - Copper/tin bonding
  - Polymer/adhesive bonding
- 2) Wafer thinning
  - Grinding, lapping, etching, CMP
- 3) Through wafer via formation and metalization
  - With isolation
  - Without isolation (SOI)
- 4) High precision alignment



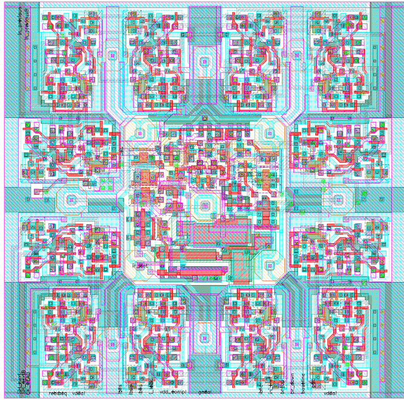


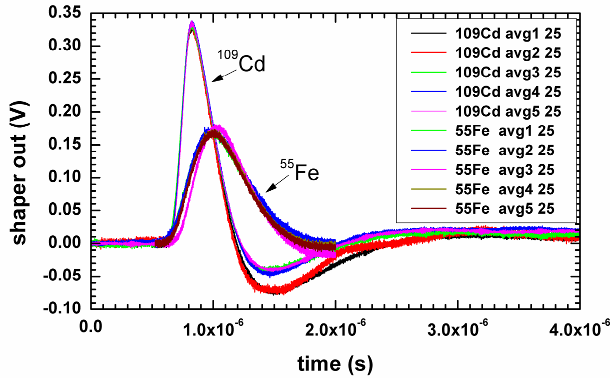
8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)



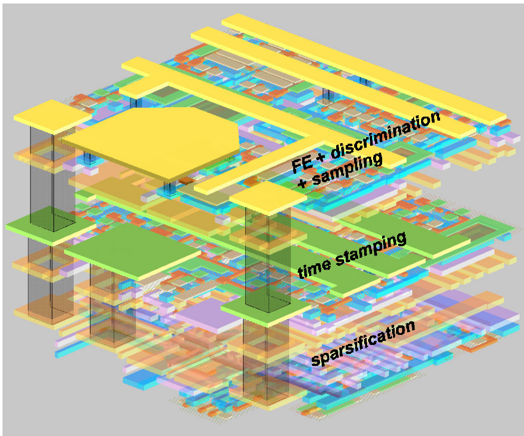
8 micron pitch DBI (oxide-metal) bonded PIN imager (Ziptronix)

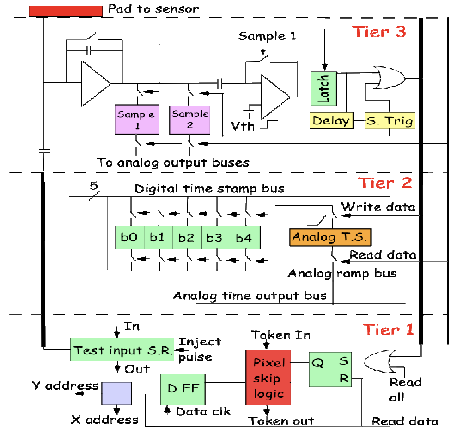
FNAL SOI/3D Studies



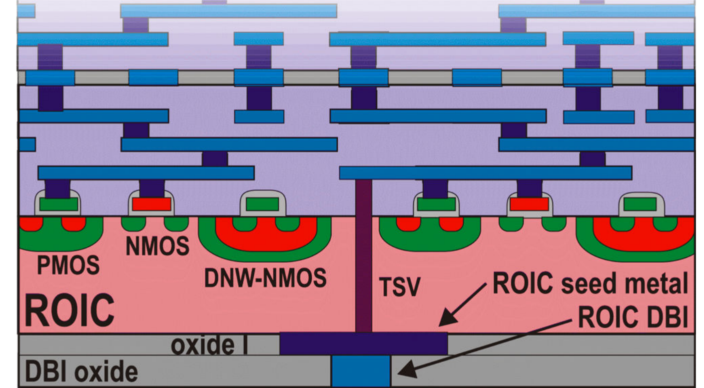


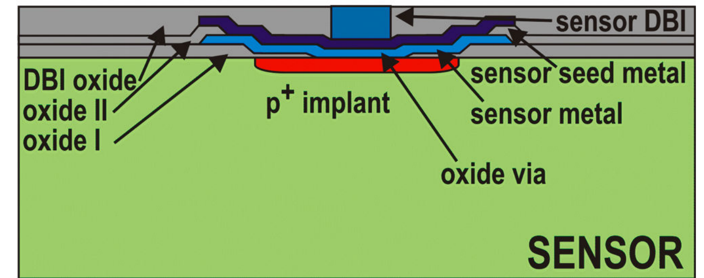
Mambo SOI Chip (KEK/OKI)

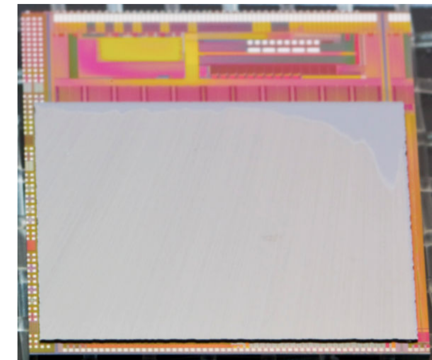




3-Tier Vertex chip for ILC

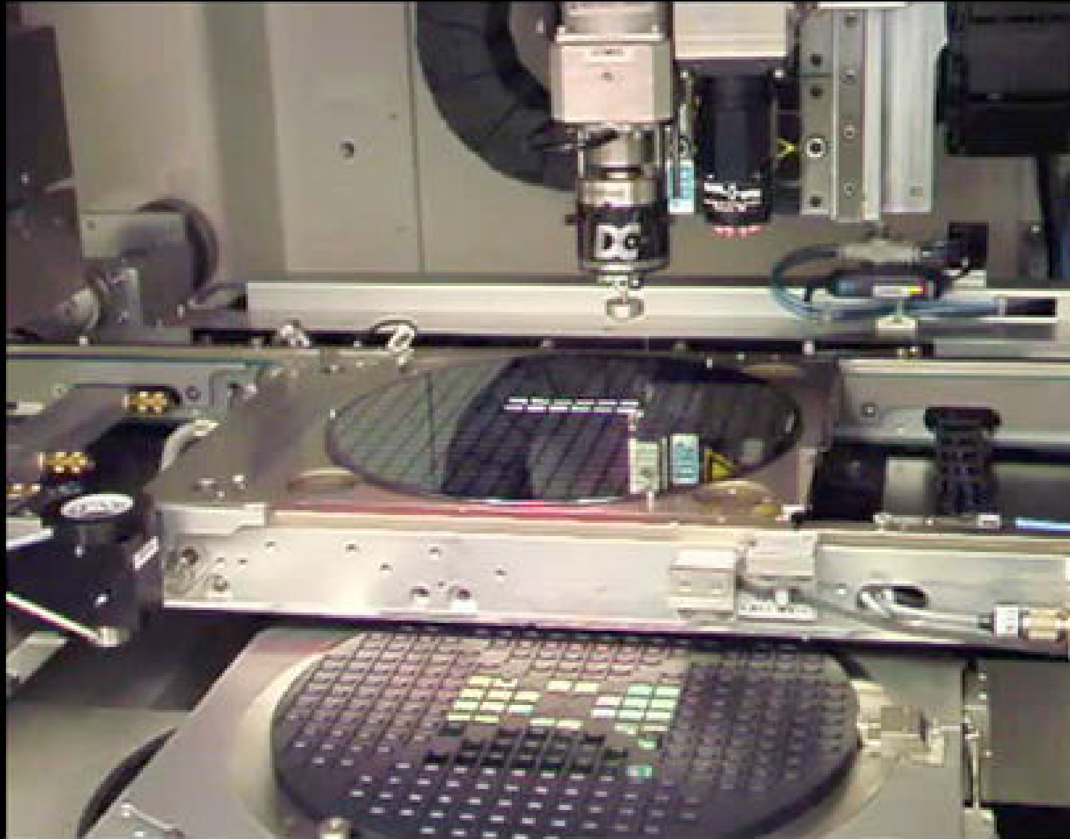






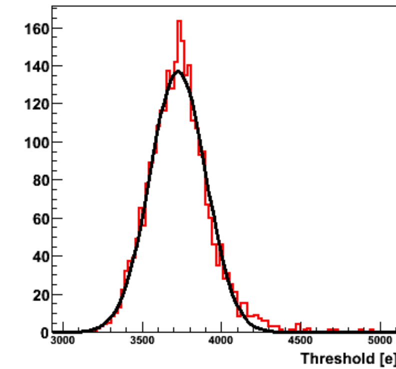
+ Detector thinning
Laser annealing
Cu-Sn interconnect
SOI technology

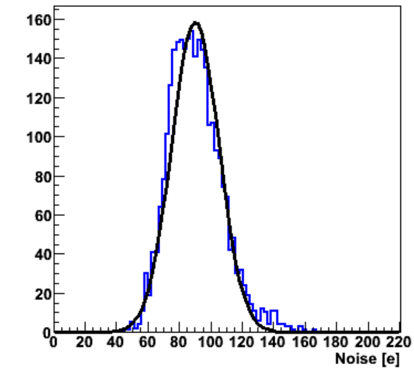
DBI Movie

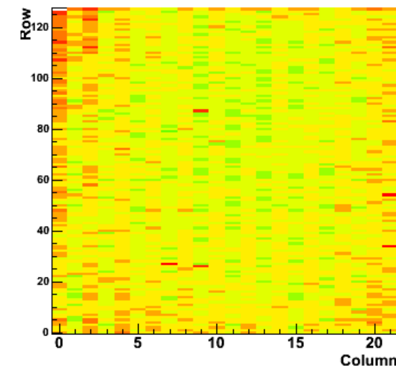


DBI Studies

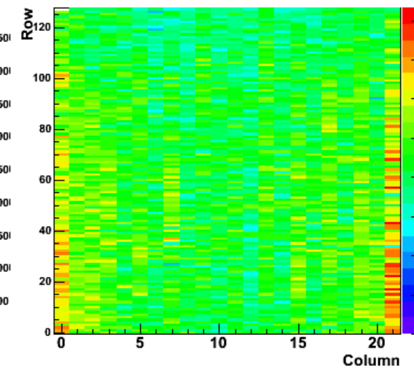
- Studied DBI using MIT-LL sensors and BTeV FPIX
- Good connectivity, but some bond voids
- Verified performance
  - X-ray source tests
  - Radiation tests to 10 Mrad
  - Beam tests



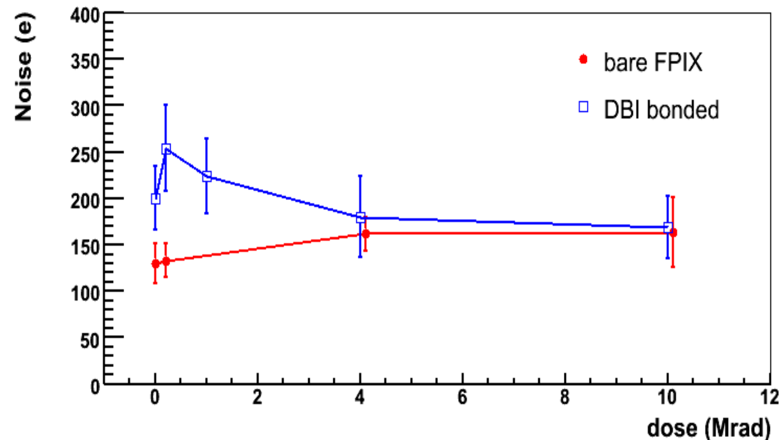


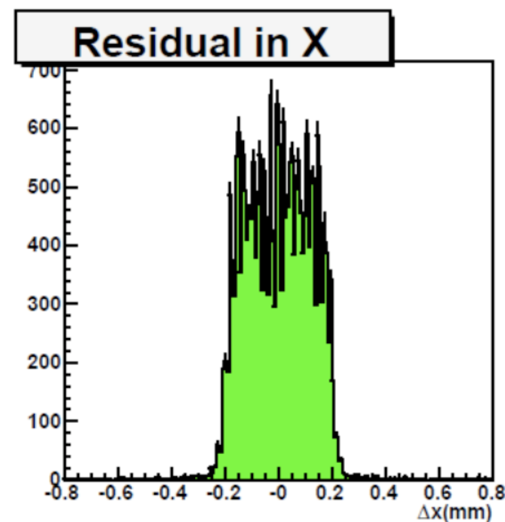


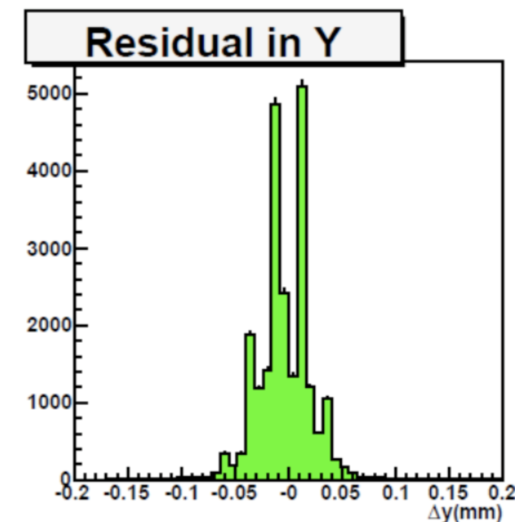
Threshold scan



Noise scan





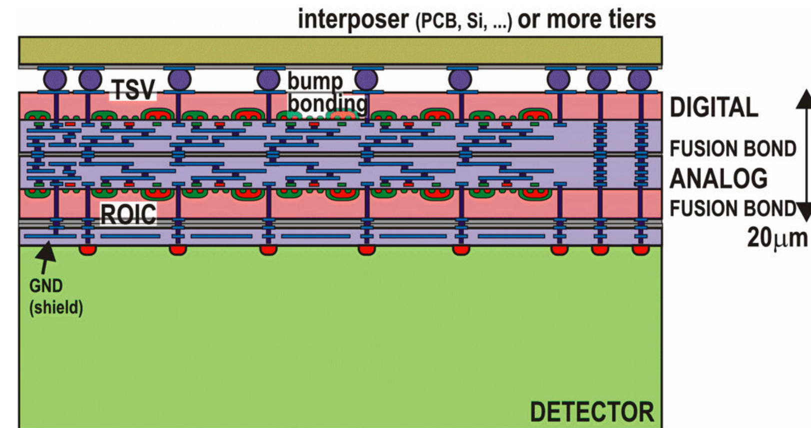


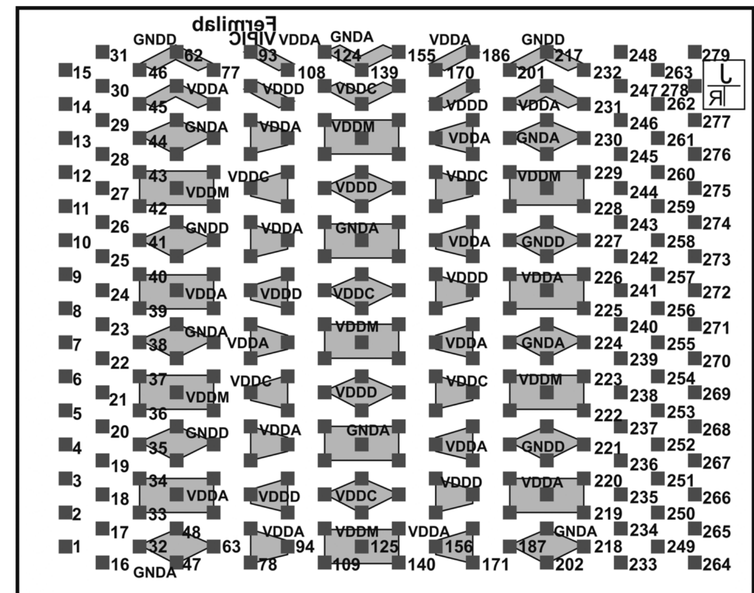
3D Tiled Arrays

These 3D technologies provide the ability to fabricate large area 4-side buttable arrays

- DBI can bond chips with 10 micron spacing
- Topside thinning provides access to interconnects over the full chip area
  - No dead area on edges for interconnects
  - Low impedance connection to ground and power planes
  - Good shielding
- Separation of analog and digital circuit layers

We hope to demonstrate this with the VIPIC and VIP chips in the Tezzaron/Ziptronix run



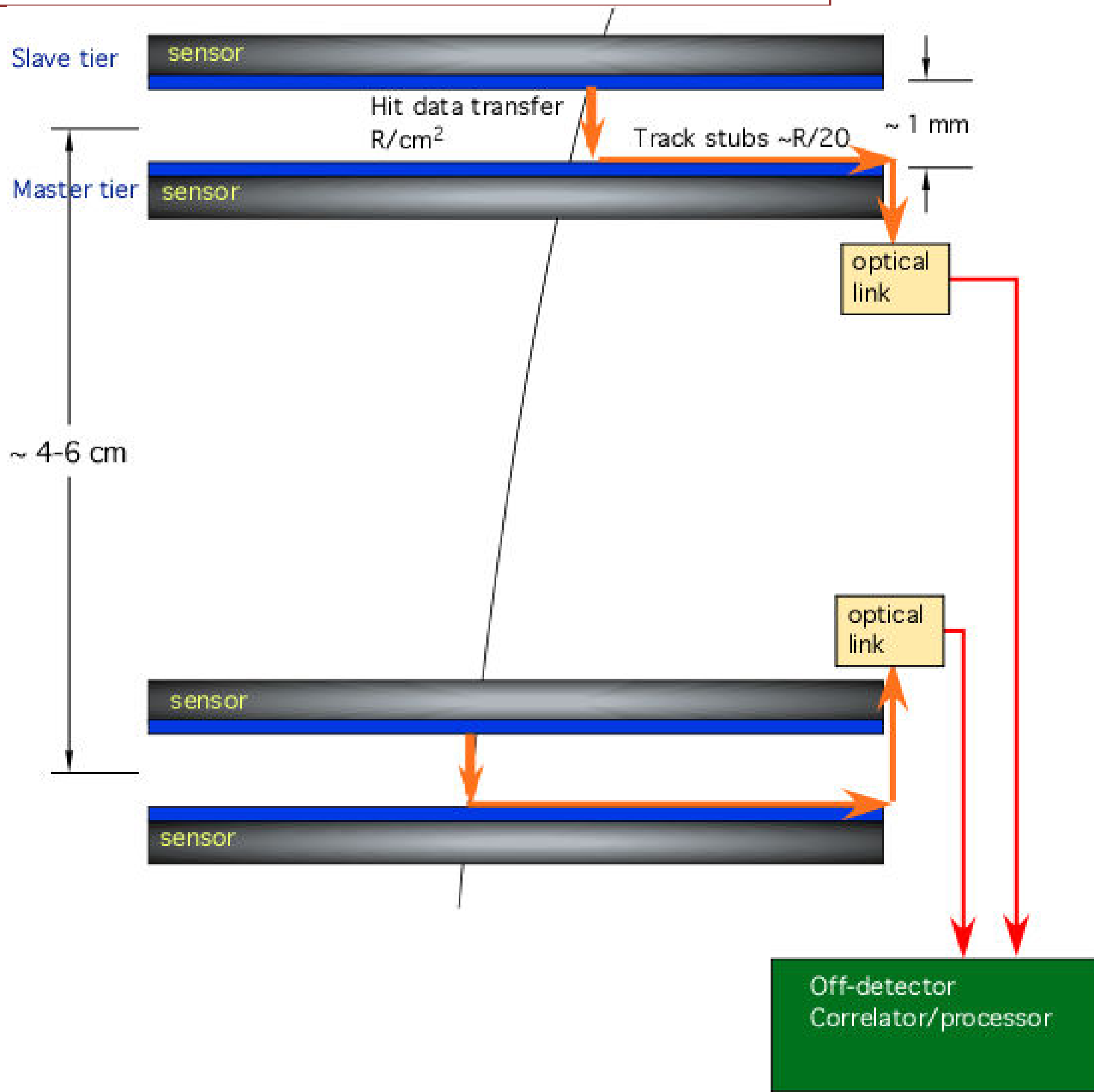


(Deptuch)

The CMS Track Trigger

- At SLHC the standard L1 triggers for CMS will saturate
- It is generally agreed that some sort of momentum-based track trigger will be needed to accommodate $L \sim 10^{35}$
- Such a trigger would need to gather information from 10^8 pixels in $200 m^2$ of silicon at 40 MHz
- Power and bandwidth to send all of the data off-detector is prohibitive
  - Local filtering will be necessary
  - Smart pixels needed to locally correlate hit Pt information
- There are several schemes being studied
  - Correlation of bits between two closely spaced layers
  - Use of cluster width to estimate local curvature
- We are studying the use of 3D for the first option

Double Stack Concept



Data flow:

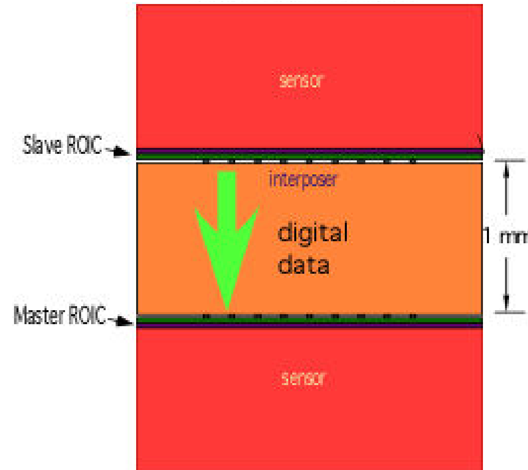
- Hit information flows from top to bottom tier
- Bottom (master) tier looks for local correlations, filters clusters, and sends data off-module
- Stubs are sent off the rod to a processor which forms local tracks (tracklets) and tracks.
- Tracklets are used to seed full tracks

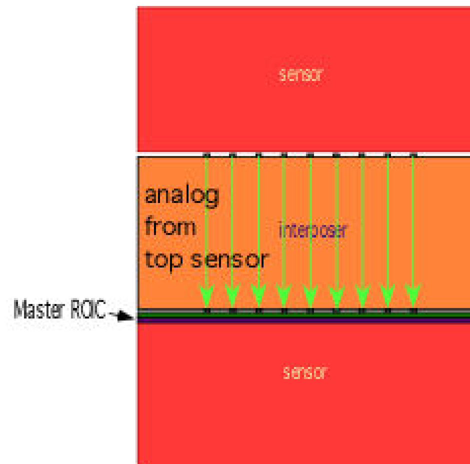
This technique ensures that all information can be localized into sectors whose size depends on the Pt cutoff

Top to Bottom Data Transfer

- Options:
  - Digital transfer through an interposer
  - Digital transfer at edge
  - Digital transfer through PCB (conventional)
  - Analog transfer through interposer
- 3D allows direct vertical interconnection – allowing for local correlations to be formed, minimizing power and complexity of the logic, allowing fully integrated module design

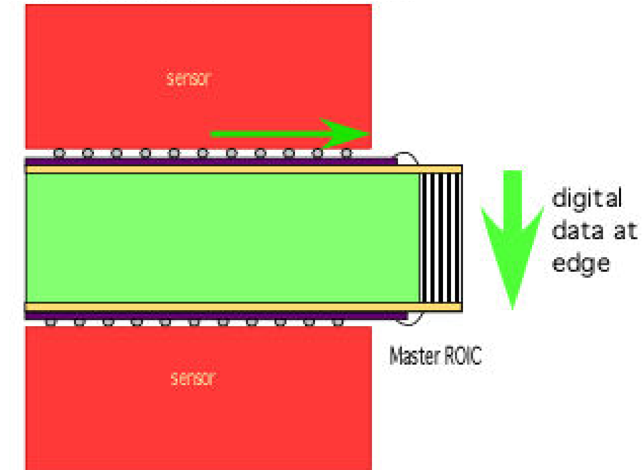
Vertical solutions

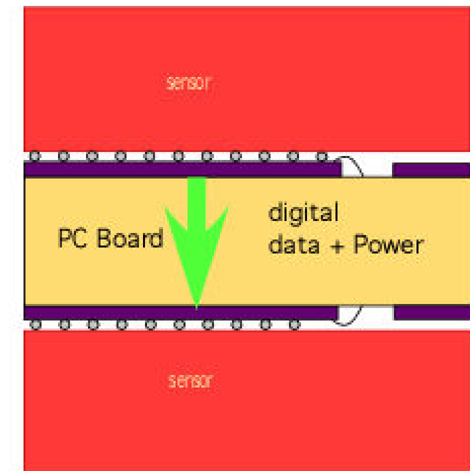




Model explored in 3D R&D program

Horizontal solutions





Models explored in Pt module R&D program

Data transfer options

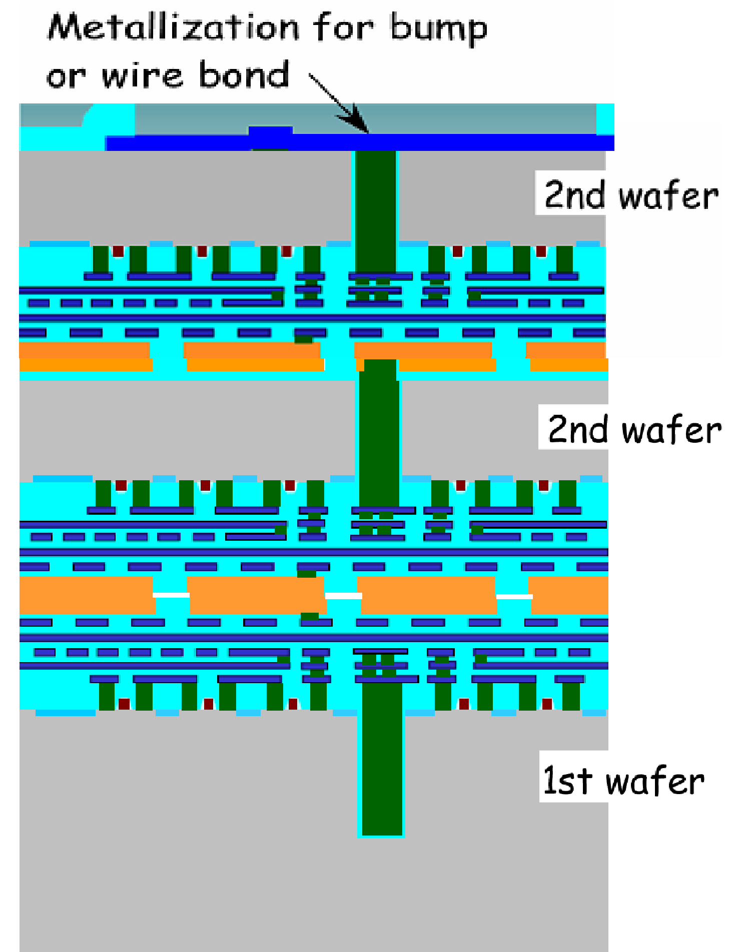
- Digital transfer at edge or through interposer
  - Chips must encode/decode hit addresses (power?)
  - Each cluster must be routed at high speed through interposer/PC/interconnect
    - Noise injection into sensor many 100 MHz busses-> current mode transmission or balanced differential signals.
    - Neighbor chip connections will be needed in phi and z
    - Does data need to be buffered? Where?
- Analog transfer from top sensor
  - Possible in 3D design
  - Requires longer (~1 cm) z strips in top tier (limit interposer vias)
  - Allows for *local* processing of correlations (no address decoding)
  - More front-end power due to more capacitive top->bottom connections
  - Single layer may simplify cooling
  - Allows design with only one tier of chips ($£¢¥)

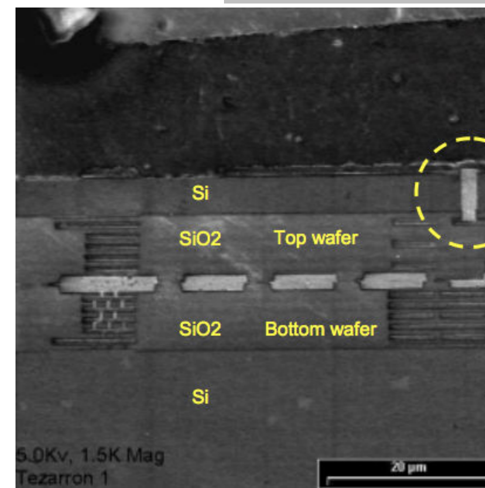
Z Resolution

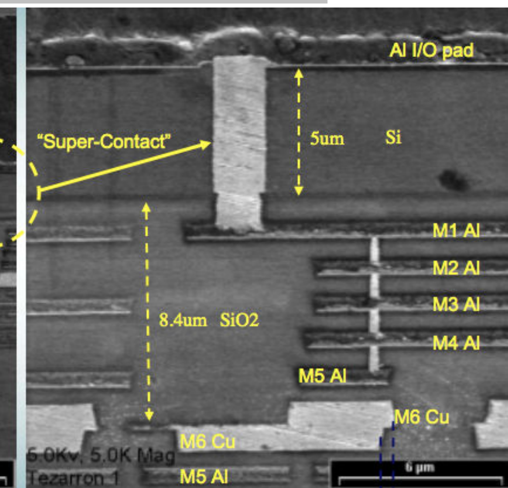
- Any trigger based on multiple track objects will benefit from additional z resolution to limit candidate primary vertices
- Z resolution is most relevant for correlations between widely separated doublet hits (stubs are too close)
  - 3D design assumes ~1 cm strips on top and ~1 mm on bottom
  - Top strip (logical) length sets the interposer density in 3D design
- We assume ~1-2 mm z pitch is possible for both conventional and 3D designs. Smaller pitch is possible, but assembly is more complex, technology challenging, and power may be a problem.
- What will be needed for trigger rates? Rate for many triggers is likely to be linear in z resolution.

Demonstration Chip

- Fermilab is sponsoring a two-tier 3D multiproject run with Tezzaron
- Tezzaron (Naperville) has developed a 3D process utilizing CMOS wafers from a commercial IC foundry with cu-cu bonding and "standard" thinning and lith.
- Wafers with "vias first" are made as a process option at Chartered Semiconductor in Singapore.
- Wafers are bonded, thinned and topside processed in Singapore by Tezzaron
  - Bond pads
  - Bump bond pads
- Commercial (10^6 8" wafers), well characterized 0.13 micron process
- Chip is intended to demonstrate 3D module interconnect



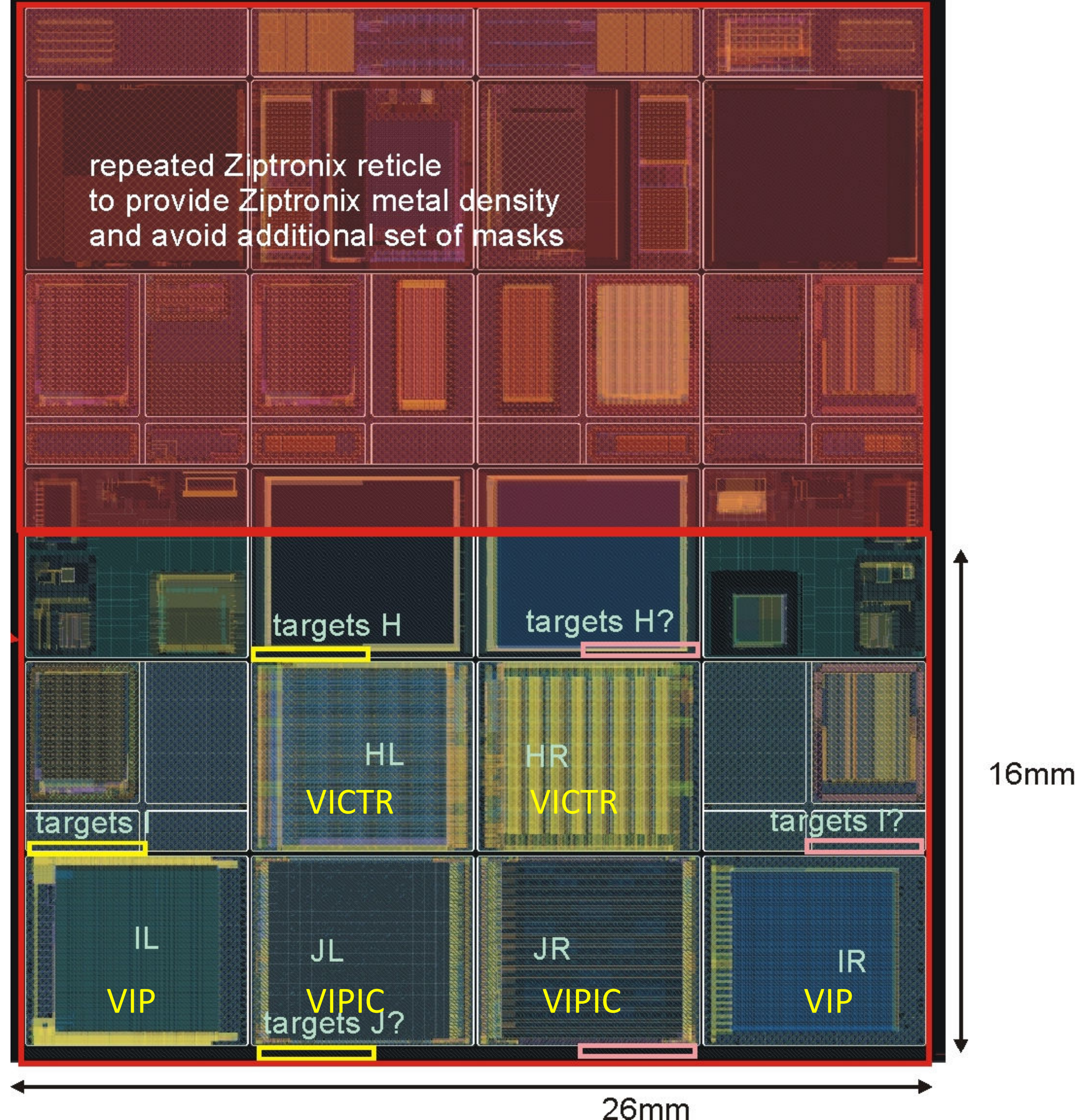




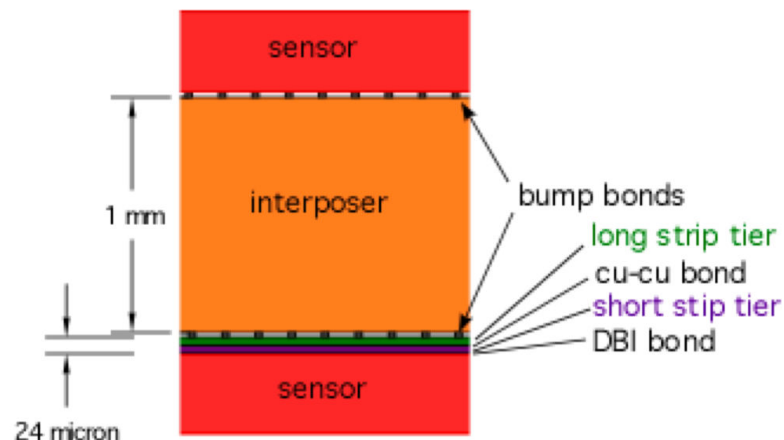
Tezzaron MPW frame – each circuit contains right and left tiers after bonding

• VIP2b – Two –tier implementation of ILC VIP chip
• VIPIC - Vertically Integrated Photon Imaging Chip time stamping chip for x-ray imaging
• VICTR – 3D chip for sLHC CMS trigger

•Status – Continuing struggles with DRC and data validation issues. 'Any day now' for 6 months.



VICTR- Vertically Integrated CMS TRigger Chip



Chartered FEI4 design contributed by ATLAS

Phi strip inputs

Top test in

Test circuit

(2) Ld/clk

Hit in

(2) Ld/clk

T

And

C

B B B B B

CMOS (1) 64 bits

Top OR out

LVDS (2) 1 bit

LVDS (8) 80 pixels, 8b/pix on each of 4 output lines

Data: T C B B B B B X

64 ORs of 5 ORs each

Bottom OR out

LVDS (2) 1 bit

Bottom test in

(2) Ld/clk

CMOS (1) 64 bits

Z strip input

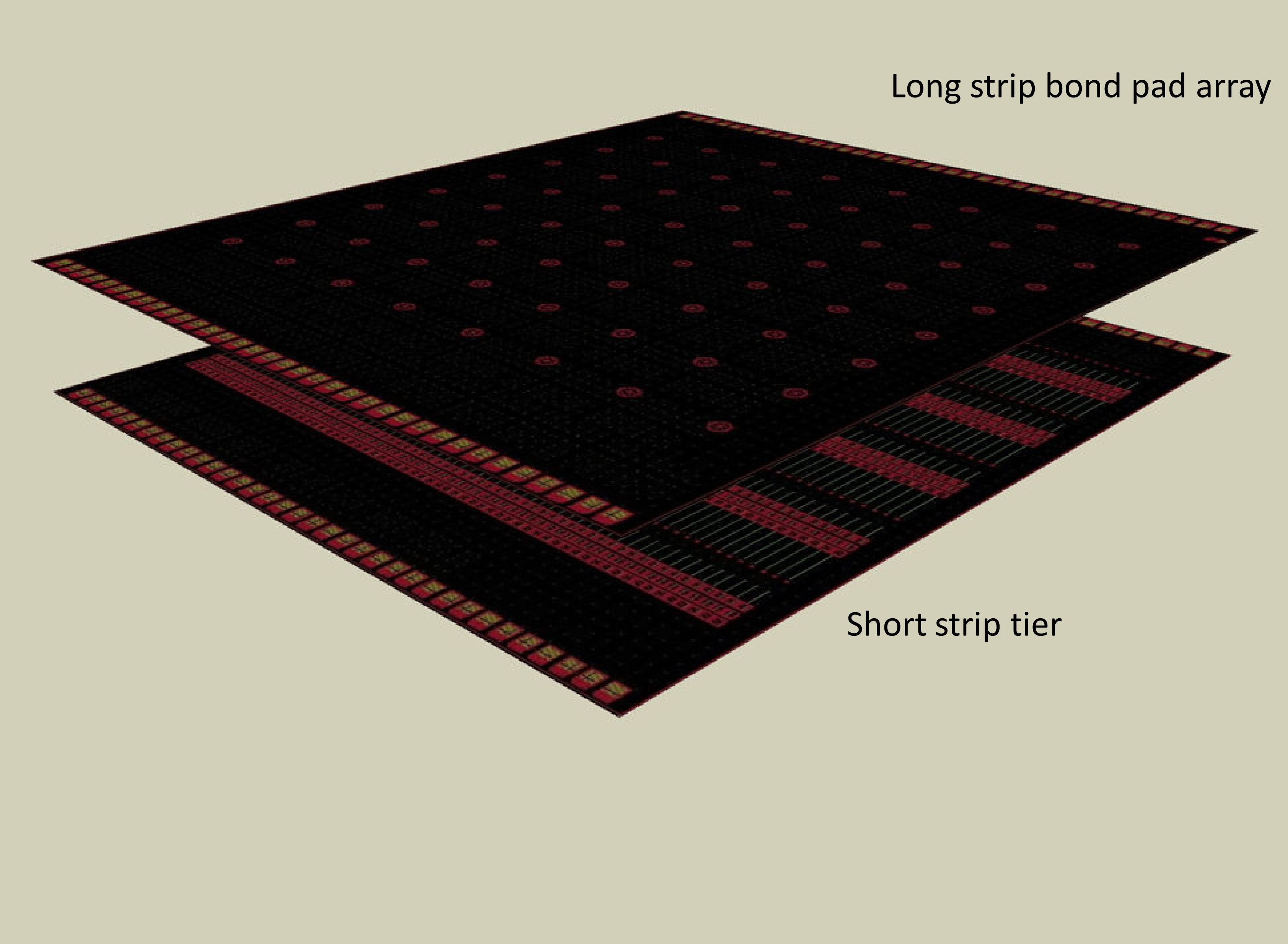
Simple chip digital design

- top/bottom coincidence
  - 5x1 mm bottom with 5mm top
- serial readout
- Fast or output

Top Tier – bump bond pad array

Bottom tier – DBI bond array

VICTR Top Metal



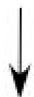
3D Sensor Integration

Tezzaron Wafer after bonding

cu 3D connection

Ziptronix Wafers

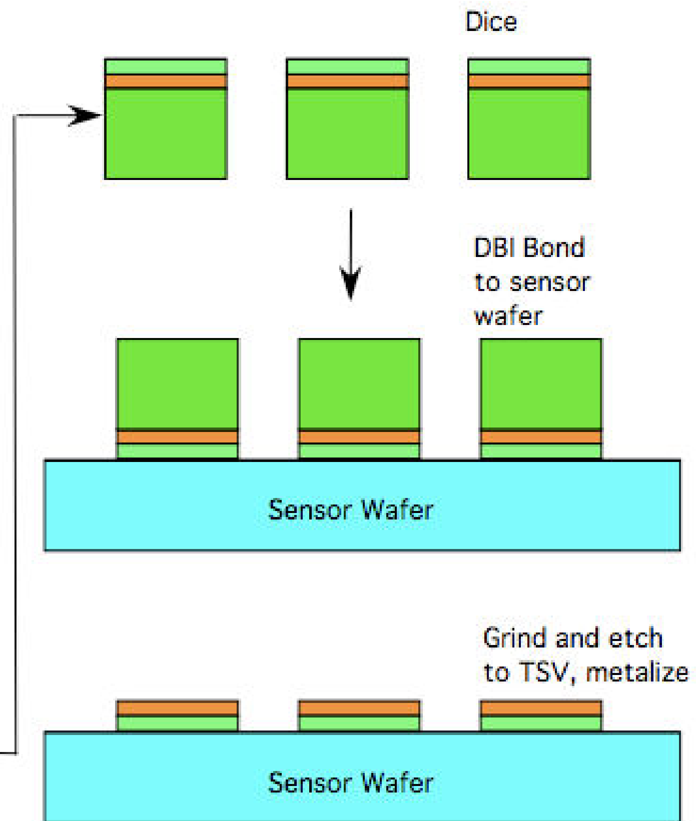
Thin to top pad side TSVs



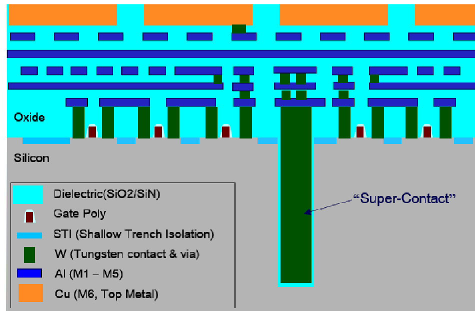
Send to Ziptronix

Oxide bond to handle wafer at Ziptronix

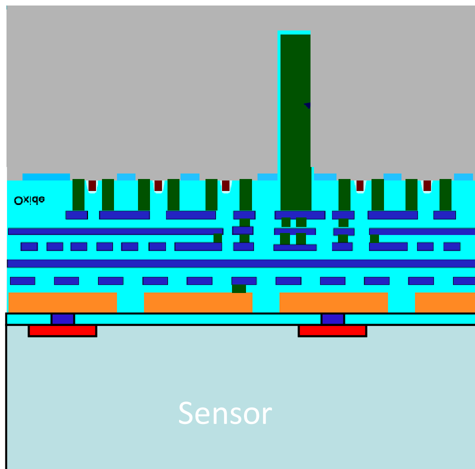
Thin to sensor side TSV at Tezzaron or Ziptronix



3D Fabrication of Stacked Layers

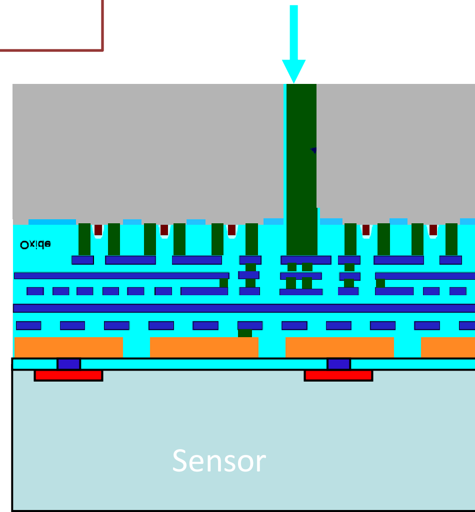


Readout IC wafer with TSV from foundry

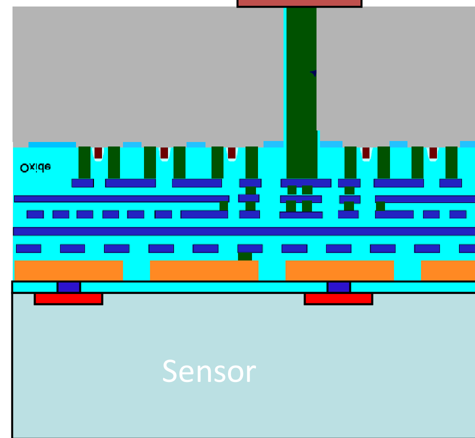


DBI bond

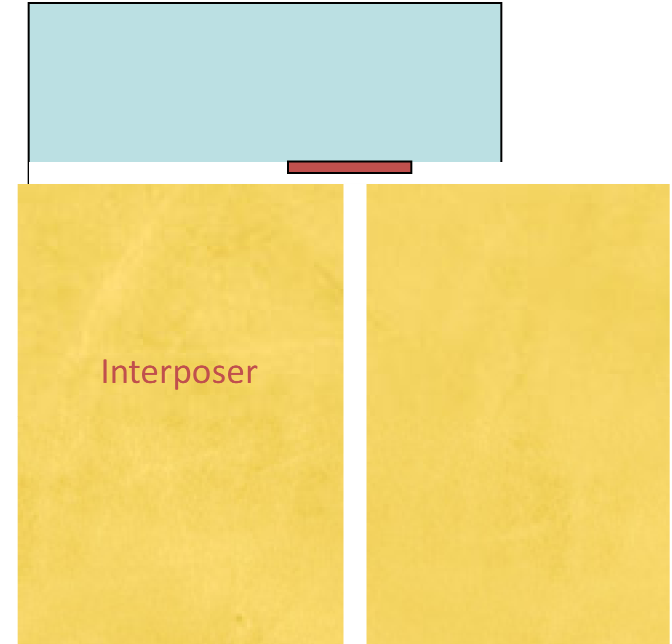
Oxide bond diced ROIC to sensor Wafer.

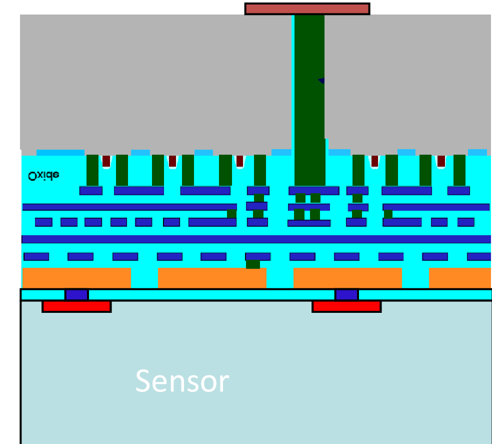


Thin to expose TSV



Contact lithography provides Access to topside pads for vertical data path

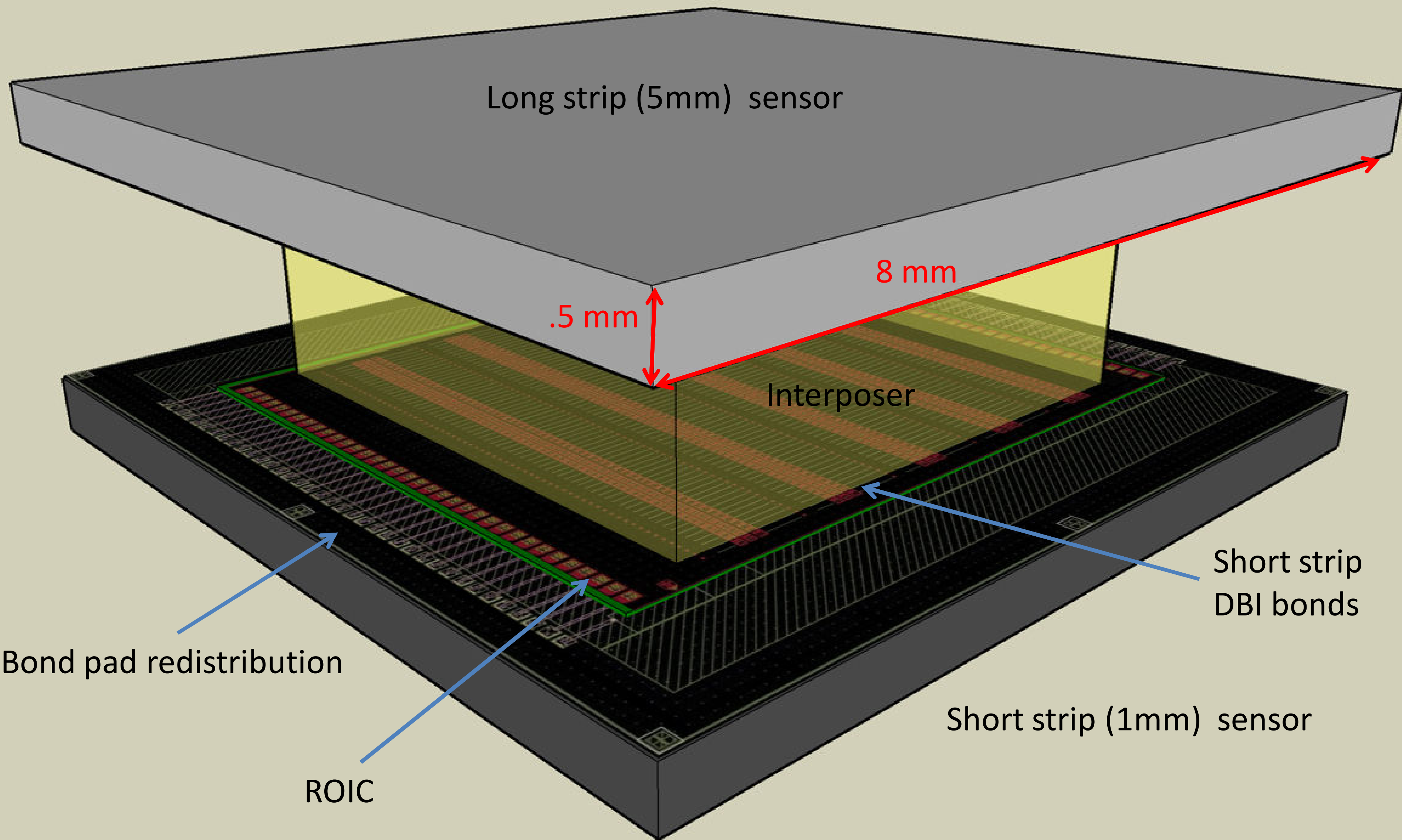




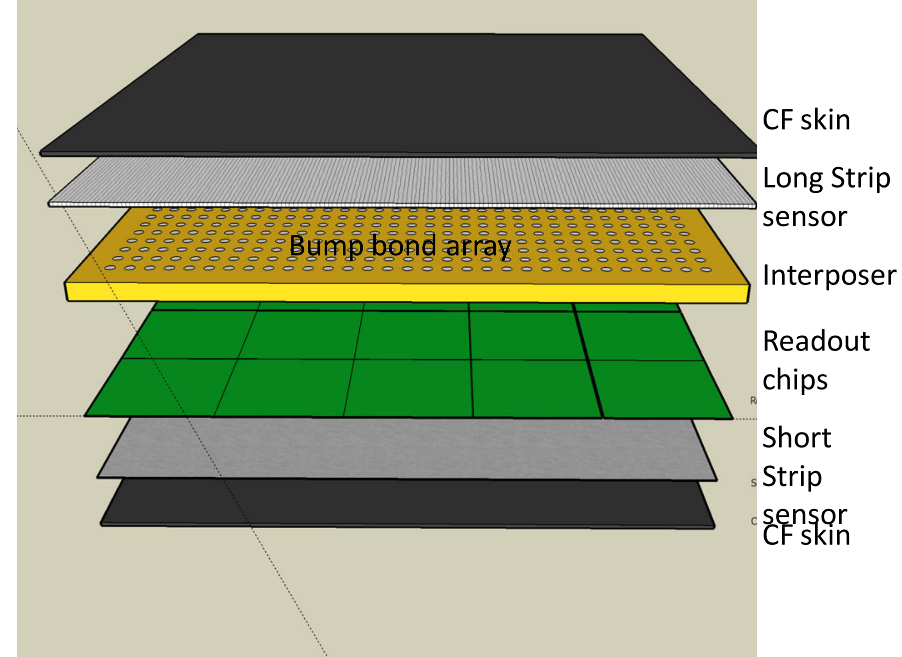
Bump Bond module

Test, assemble module with interposer

Test stack

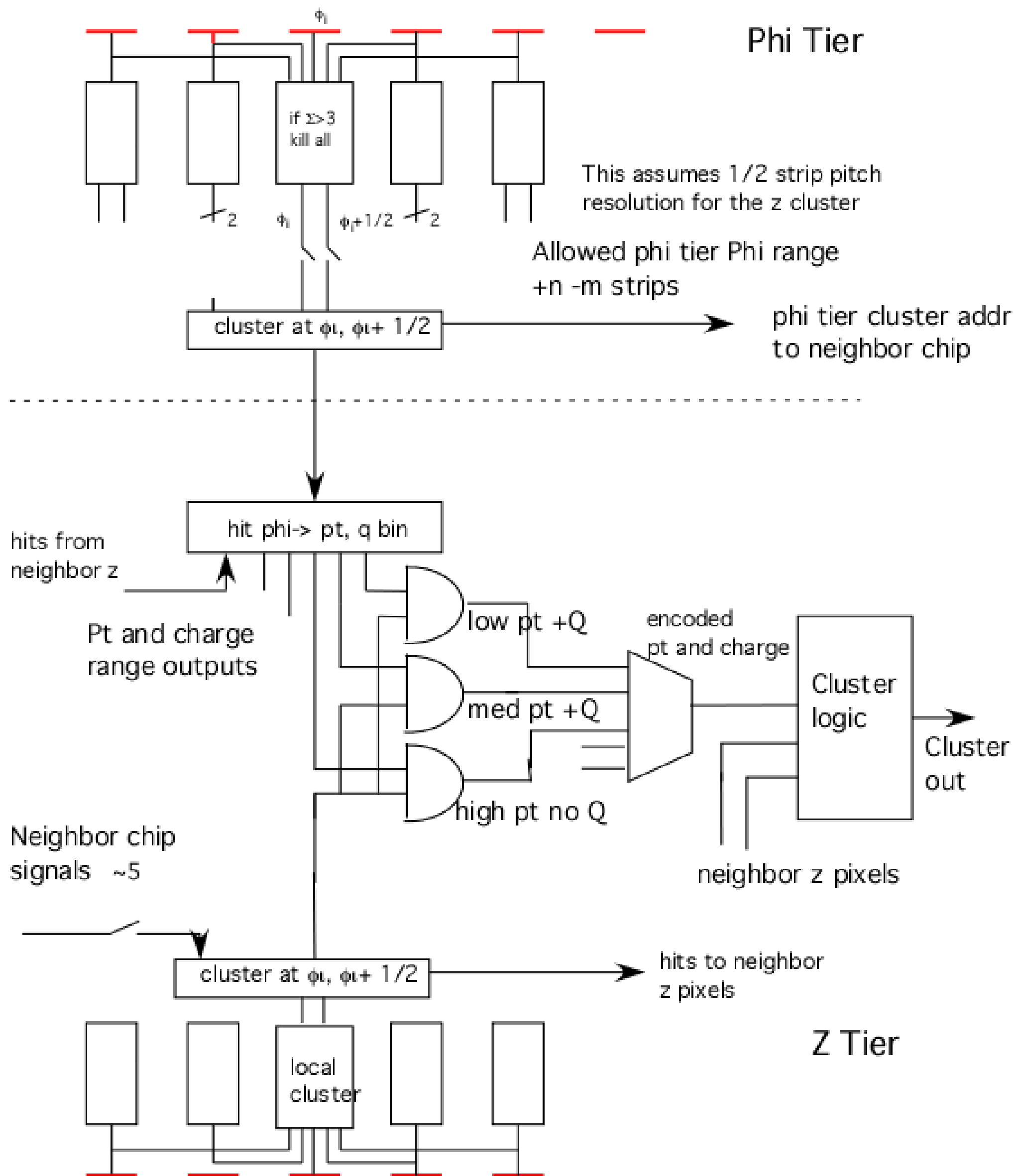


Module Design



- Modules would be nxm arrays of chips DBI bonded to sensor. This can be done because both top and bottom IC pads are accessible.
  - Chips are bump bonded to interposer
  - Top sensor bump bonded to interposer
- Interposer
  - Transmits top sensor analog signals to ROICs
  - Provides interconnect and power to ROICS
  - Provides readout bus interconnect
  - Flex output to optical components
- We are asking a lot of the interposer – major R&D area

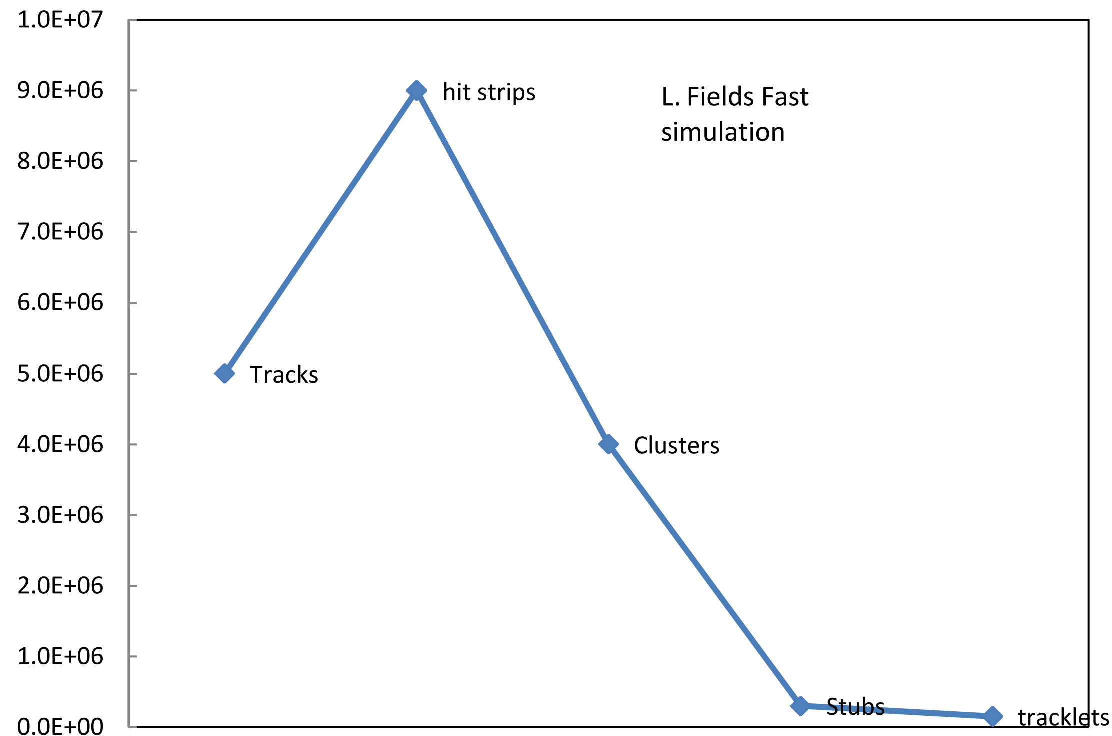
Local Trigger Logic



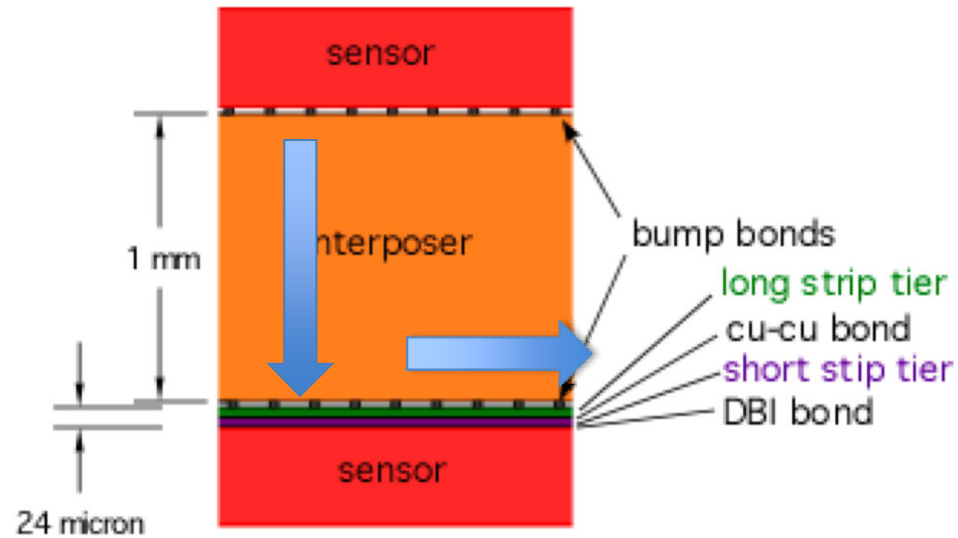
- 3D design allows for local trigger logic – simple example
- Each strip looks at ~ 4 neighbors
  - Kill all hits if cluster is too large
  - Central strip outputs hit information to internal logic
  - Interpolation to ½ strip
  - Can output in Pt bins if required
- External settings for dead or noisy strips, shift of information in phi, pt threshold
- Neighbor chip sends cluster information for last short strips
- Pipelined in ~4 steps to allow wide cluster killing, neighbor transfers, cluster formation

Interconnect and rates

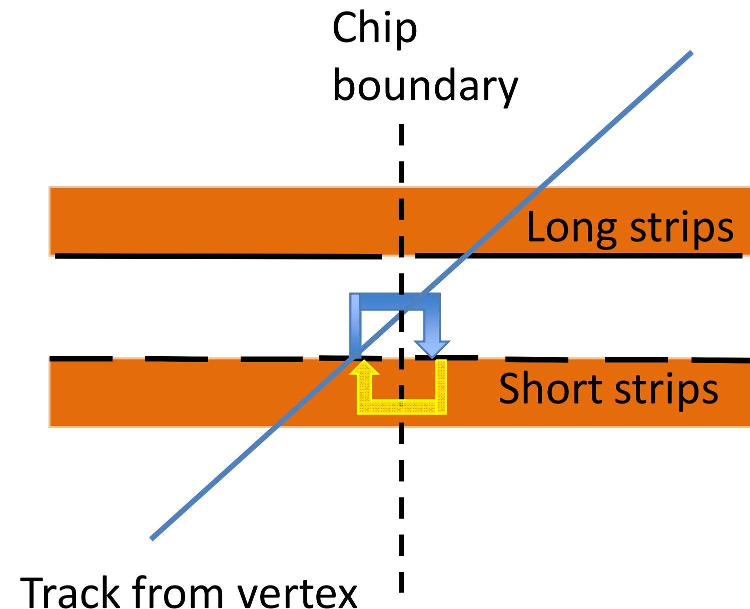
- Assume 2 cm x 2 cm chip
  - 200 x 2 analog vias (for 100µm pitch, 1 cm long strips)
  - Data bus ~ 22 bits, control~8 bits, neighbor ~ 20 bits, power/gnd ~ 20 = 70 interconnects
  - Assume 500/chip Interposer bump bond spacing ~ 800 microns
- Rate/module
  - Rough estimate at about 35 cm based on Fast MC
  - Full MC 3x higher rate
  - Add event readout (few %)
  - 2.25 stubs/xing/module
  - ~2 GHz bit rate/module
- Very large uncertainties (x5?)
- Needs continued detailed MC
- Needs (has?) data



In-Module Data Transfer



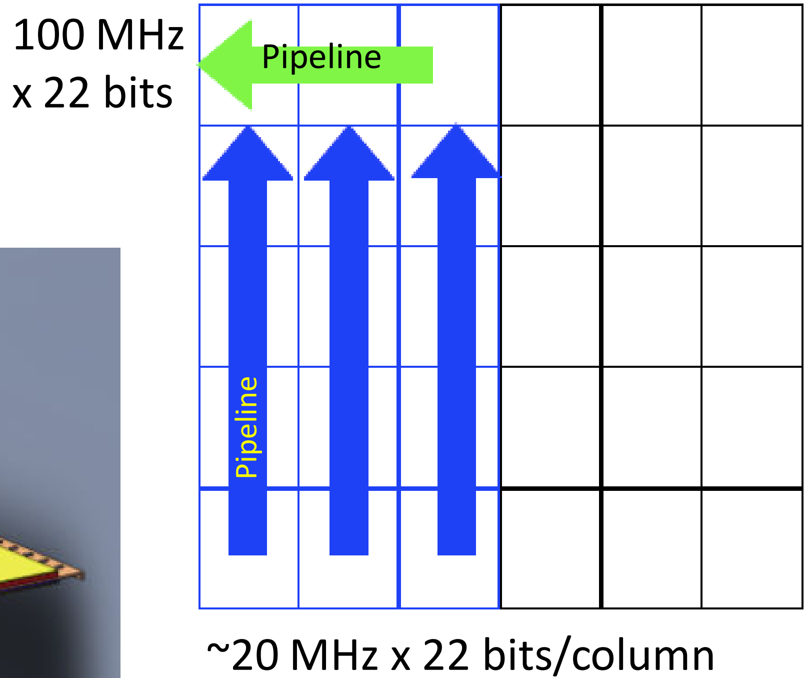
- High rate bus in close proximity to sensors
- All designs but analog transfer require transfer of some digital data at full hit rate within the module
  - Proper electrical shielding will be crucial
- Transfer cluster information across chips.
- In 3D design both horizontal and vertical transfers must be integrated
  - Extra PC board or flex layers
  - Integration of horizontal bus on interposer
  - Other technical solutions (twisted wire …)
  - Bump bonds include both analog and digital transfer
  - Guess about 125 bumps/cm^2 mostly analog

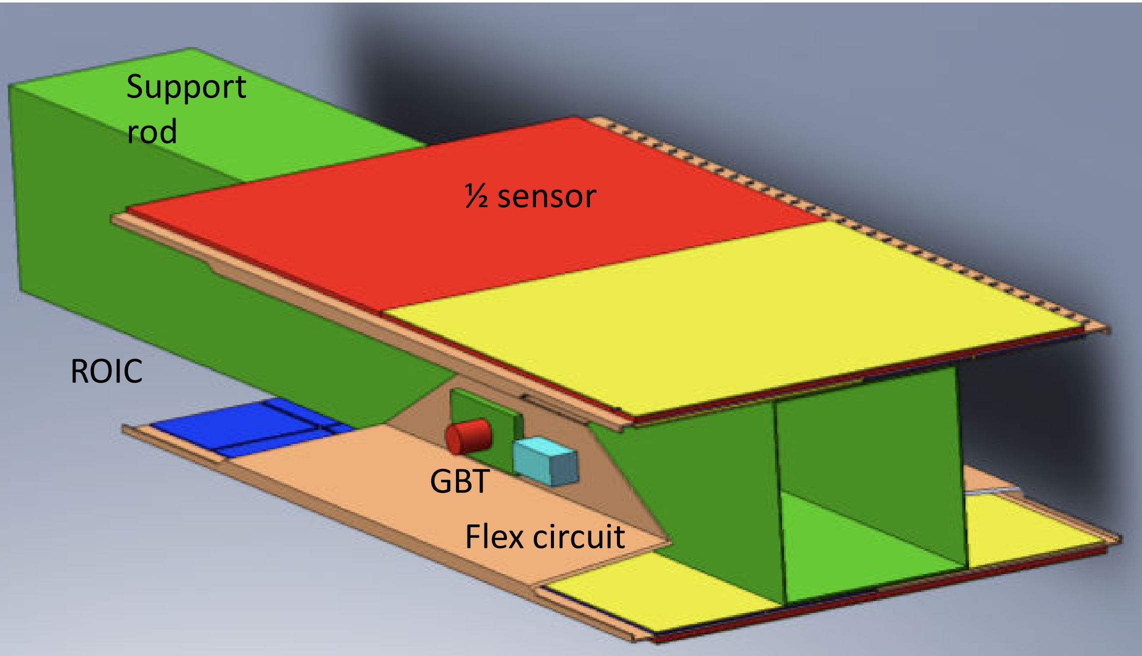


Data Readout (M. Johnson)

- Micropipelined data transfer between chips
- Tri state possible?
- Event data (5%) appended to trigger data
- Can be configured to use 1/2 , 1 or 2 GBT/module

Pipeline Step	Operation
One	Form phi clusters for both sensors
Two	Send boundary phi clusters across chip boundary to the right
Three	Send z data across long z and chip boundaries
Four	Form stubs for trigger
Five	Send trigger and event data to top of chip column
Six	Send trigger and event data across top of chip to fiber driver
Seven	Send data over fiber line to off detector system



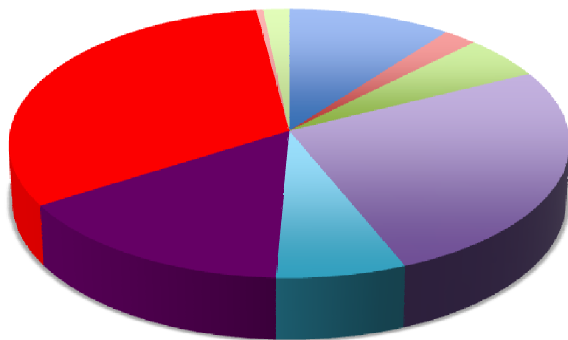


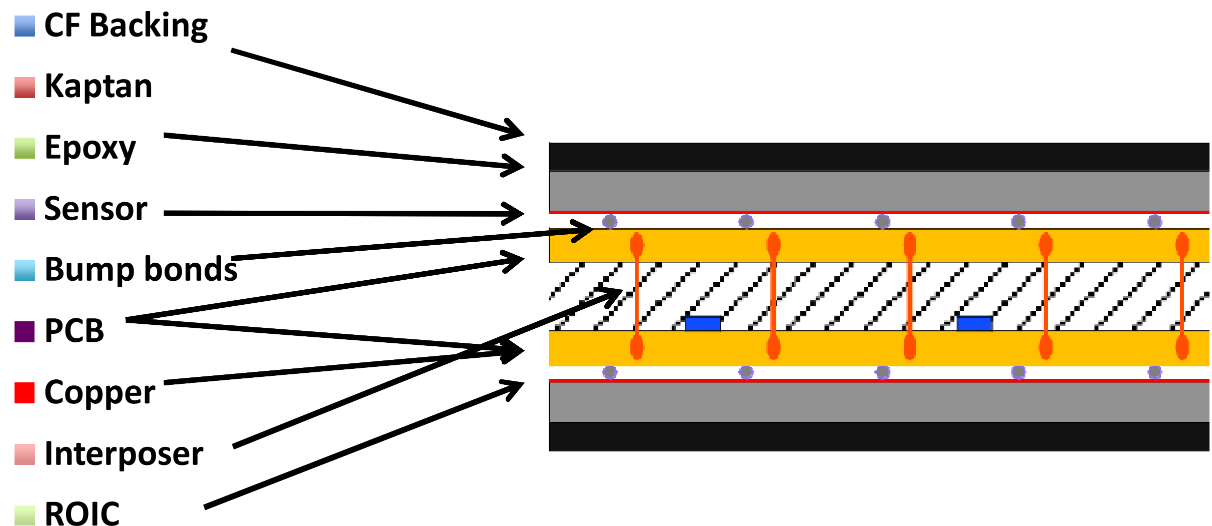
Power

- Analog – most well defined P ~ C^2_{load}
- Digital
  - Base chip power (14 mW/chip) $$P = k \times freq \times C_{int} V^2$$
  - Chip hit processing power (assume 180 pJ/hit) ???
  - Data transmission from master to slave (0.5 pf)
  - Stub transmission to optical interconnect 12 cm x .8pf/cm
  - Optical link power (nlinks/rod)
    - Link picojoule/bit numbers range from 50 – 625
- Survey of RO Chip estimates – single layer only – not really apples/apples
    - ~ 80μW/pixel→0.032 W/cm^2 (GH)
    - ~ 0.026 W/cm^2 (MM+RH)
    - ~ 0.034 W/cm^2 (RL one analog tier 3D)
  - CMS pixel chip 0.194 W/cm^2 ~ 7x more
- Not including 1/(.75-.8) penalty for DC-DC conversion

Mass

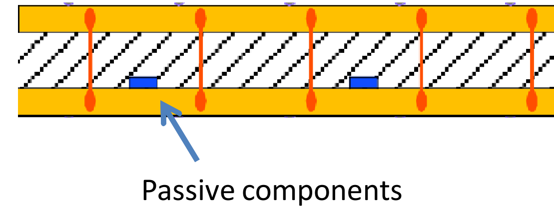
- DC-DC converter and GBT not included
  - Copper 2x D0 HDI density, low mass interposer
- How to minimize mass (in 3D design)
  - Minimize copper
  - Low mass interposer
    - Local bypass of power lines (?)
    - Foam spacer
    - “swiss cheese” silicon

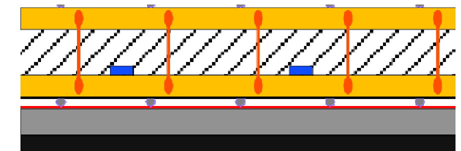


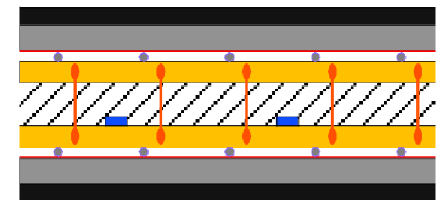


Module Fabrication

- Use 3D analog module as example
  - Assemble interposer with electronics
    - Bed of nails test?
    - Sacrificial test connector?
  - Test components
    - Test ROIC die on production wafer
    - Test sensors
  - DBI bond die to sensor (industry)
  - Glue sensors to bottom CF, Kapton (HV connection)
  - Bump bond interposer to bottom sensor
    - Test bottom assembly
  - Bump bond sensor/interposer to top sensor
    - Test full module

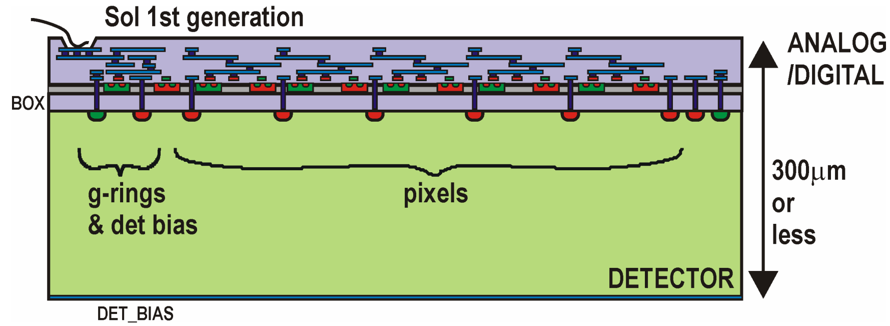


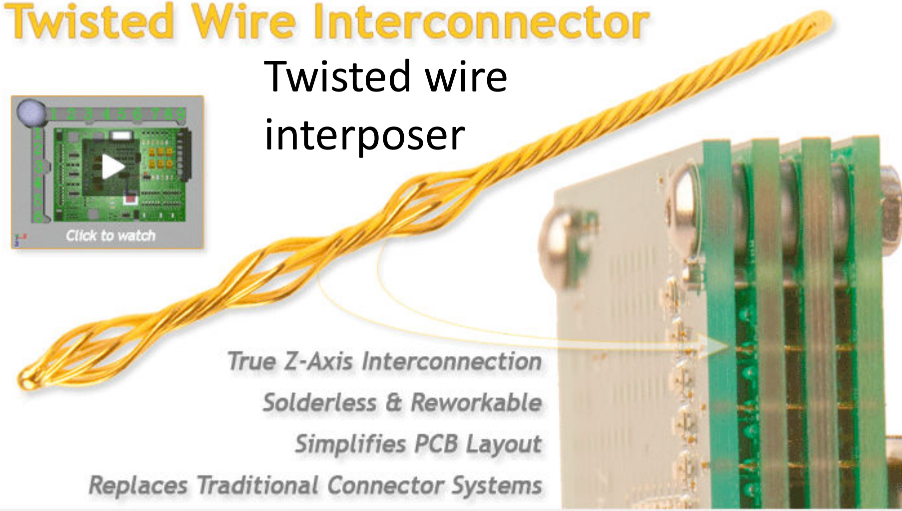


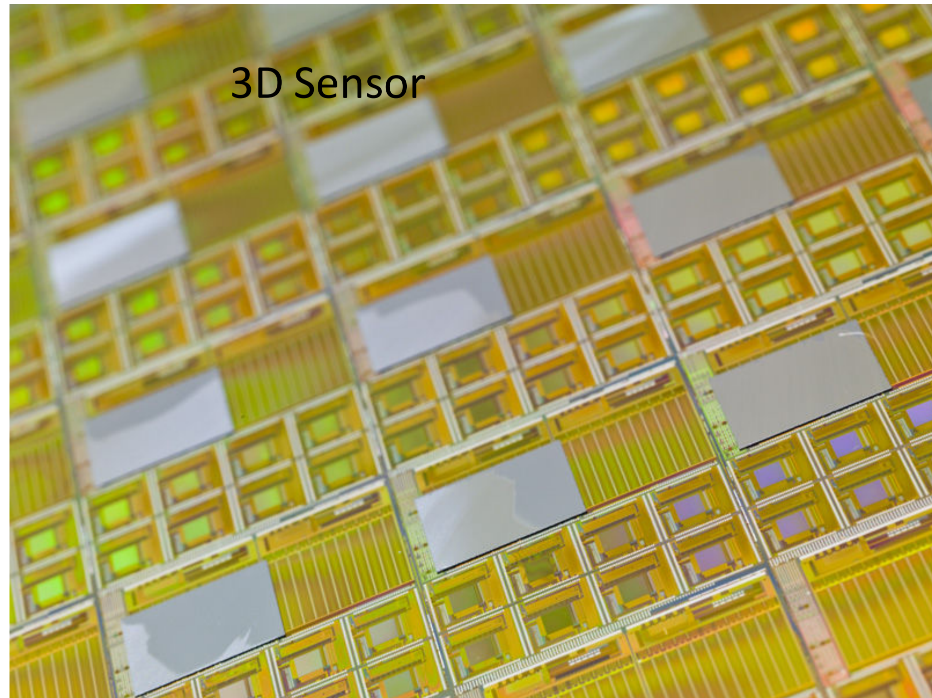


Parts for Vertical Module

SOI or MAPS

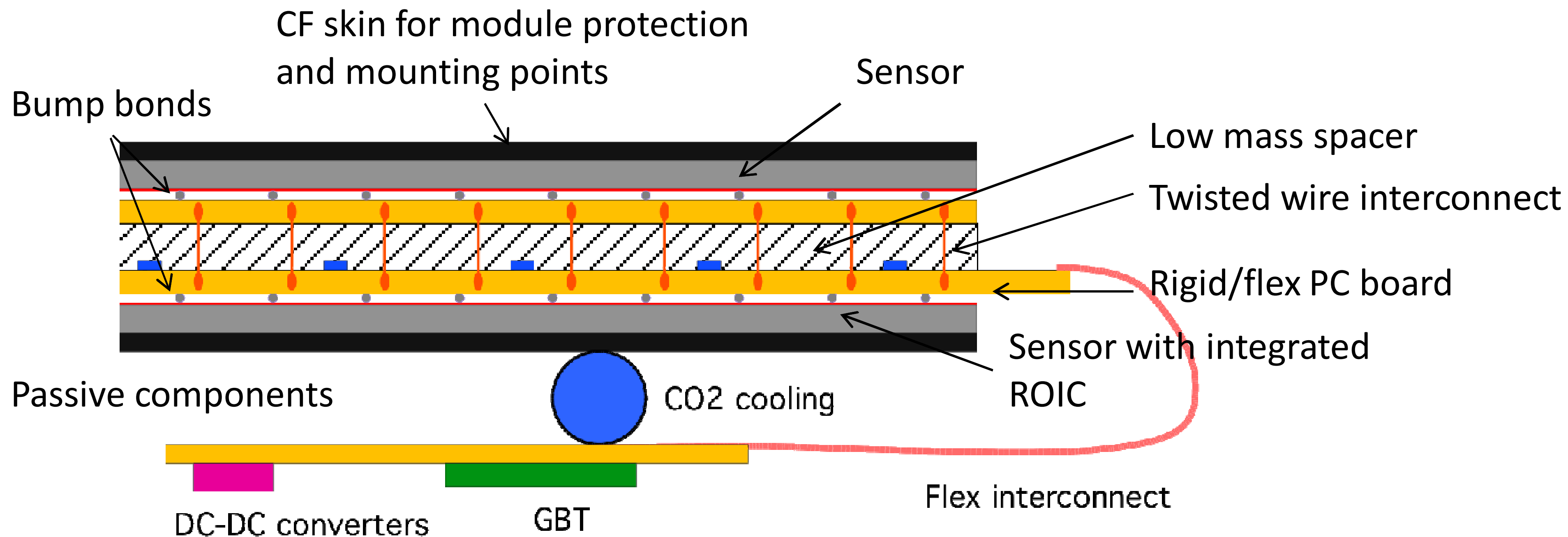






Silicon Interposer

Vertically Interconnected Module conceptual design

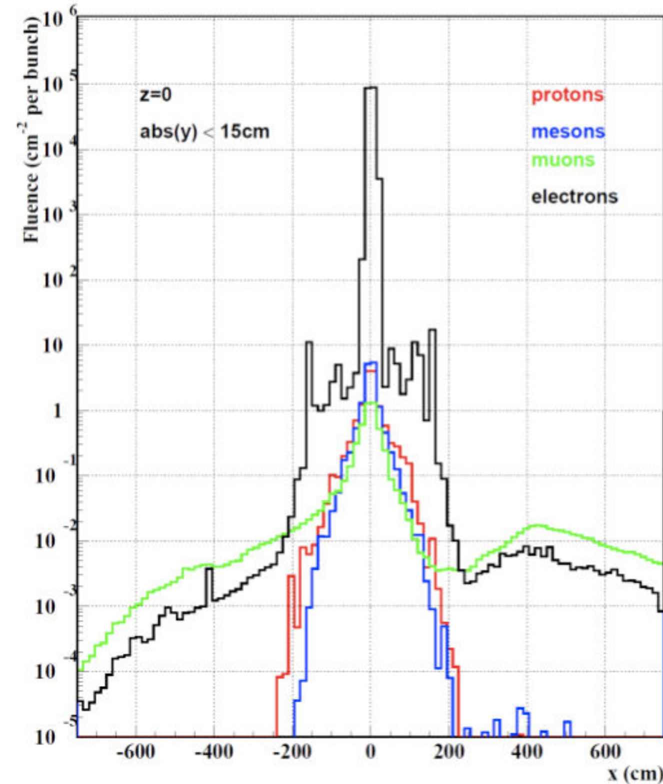


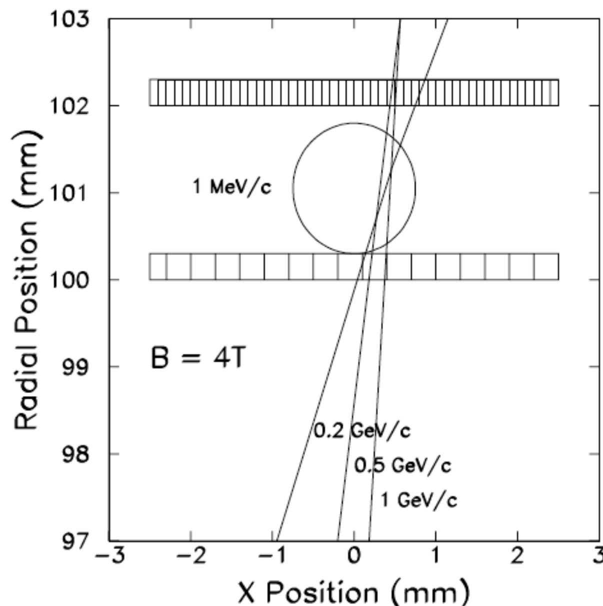
Physically robust module
Power hungry parts near cooling
Provides electrical interconnect paths which should be conventional
- Needs 2 layers of bump bonding
- Relies on vertical interconnection of sensors and ICs

Application to Muon Collider

Muon Collider VTX

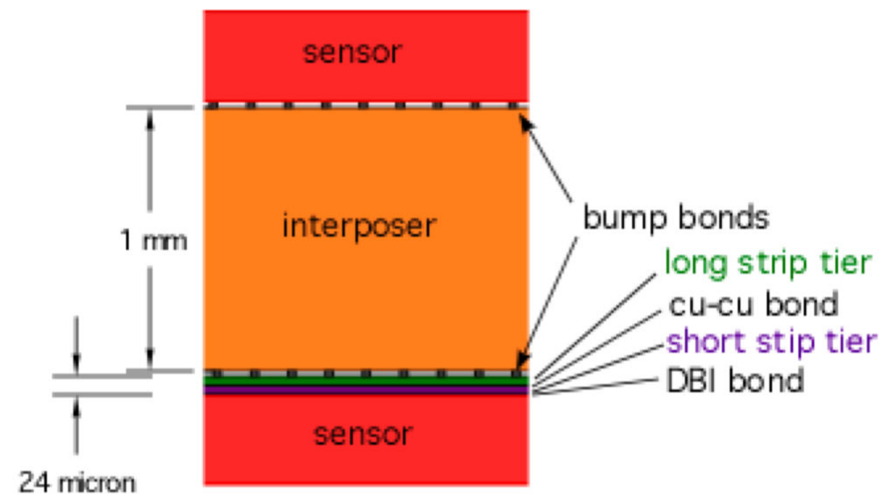
- Muon collider has very high occupancy near the vertex
- S. Geer suggested a stacked layer design to reduce occupancy based on inter-layer correlations for the muon collider in 1998
- This technology looks very much like what we are developing for the CMS upgrade





1999 μCol Track correlation module

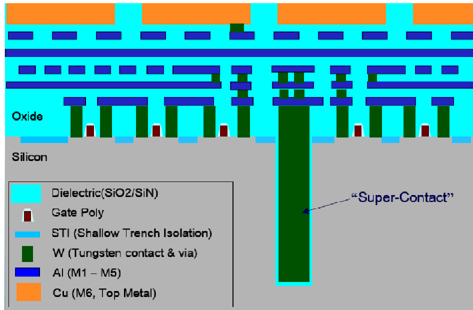
2009 Track trigger module for CMS Phase II Based on 3D electronics



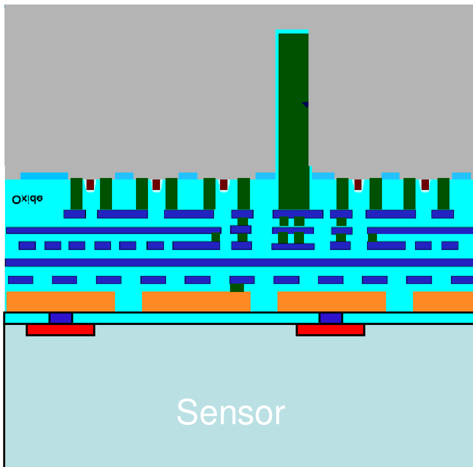
Conclusions

- Track trigger modules seems to be an ideal application for 3D/SOI
- Initial studies of bandwidth, rejection, power look promising
- Need to understand cost and yield issues
- Studying the design parameters:
  - Stub rejection – correlation algorithms
  - Algorithm and connectivity – how much is hard-wired?
  - Pt threshold
    - Power consumption – IC design modeling
    - Power consumption – optical link power
    - Power consumption – data bandwidth
  - Z segmentation
- We are investigating the concept in the FNAL 3D multiproject run

Building a Trigger module with 3D

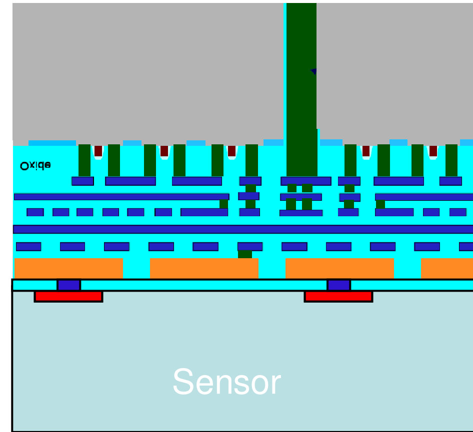


Readout IC wafer with TSV from foundry

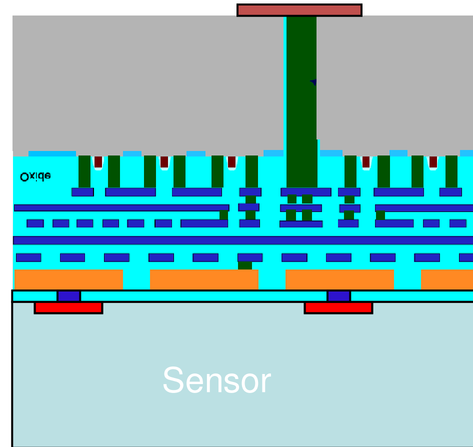


DBI bond

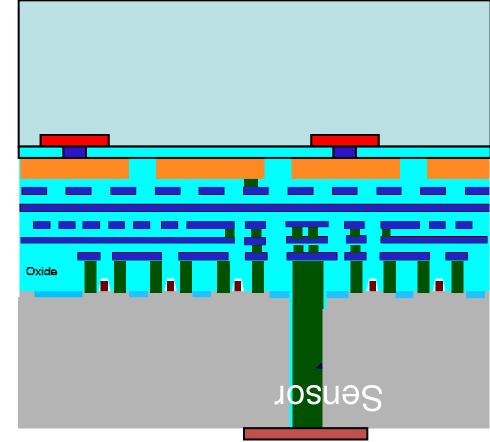
Oxide bond diced ROIC to sensor Wafer.

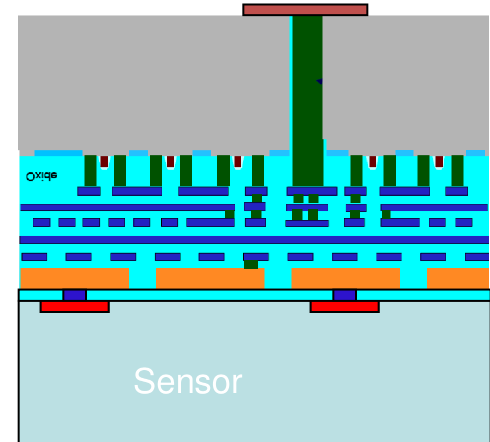


Thin to expose TSV



Contact lithography provides
Access to topside pads for vertical data path





Bump Bond module

VICTR Logic and Floorplan