LAPP electronics developments

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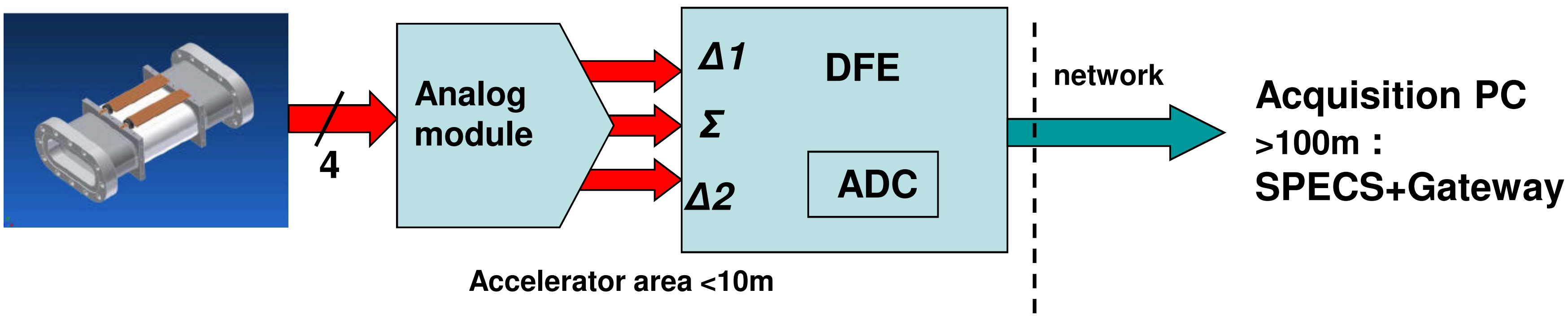
1- LAPP in CTF3: principles

Aim: *reduction of costs of long analog cables/VME ADCs - idea that future electronics should be close to the beam → Rad-hard acquisition electronics close to beam.*



Analog module: *Intensity & deviations processing BPI or BPM.*

DFE board:
- *sampling* ***3 channels, 12 bits / 500MSps****.*
- *Feed-back for analog modules: gains, calibration and attenuations.*
- *Daisy chain acquisition:* ***1 network cable per crate*** *(~4 boards per crate).*

Acquisition PC : *FESA-OASIS soft and specialist requirements feed-back.*

→ Cost divided by a factor 3 comparing to a « far » acquisition.

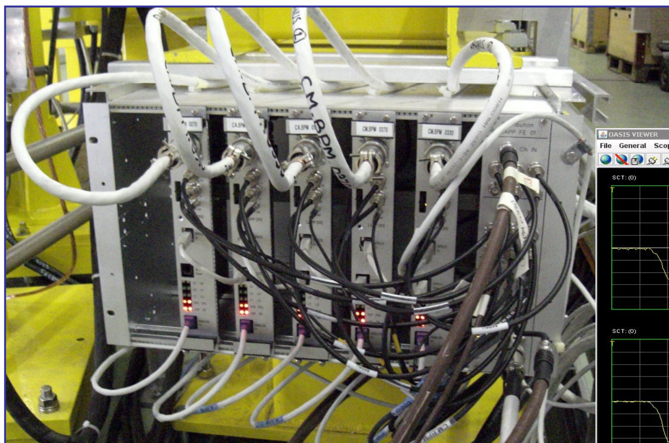
1- LAPP in CTF3: results

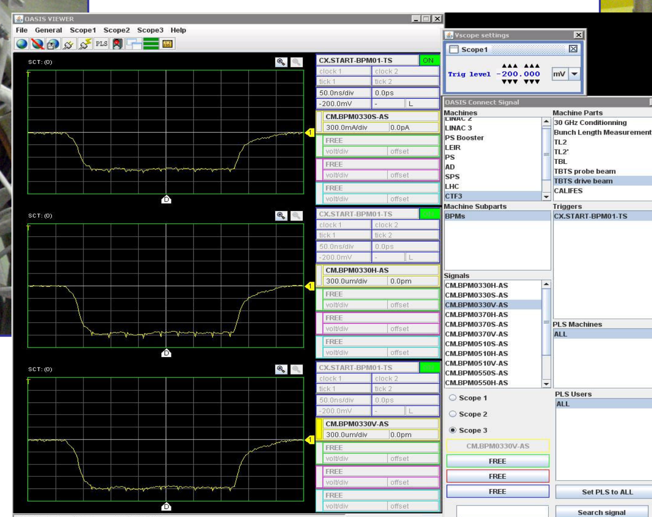
From November 2006 to summer 2009: production and installation of 47 analog modules and 46 DFE boards distributed in 12 crates in TL1, CR, TL2 and CLEX.
*Acquisition of **BPM**, **BPI** and **BPS**.*

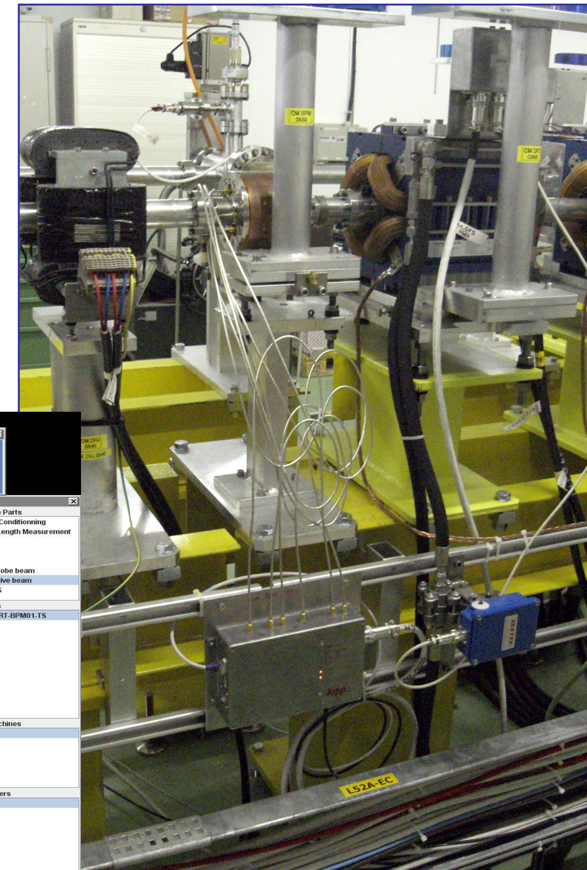
Man power: ~2,5men/year FTE since September 2005

IN2P3 funding: ~100k€.

*Results: **OK** but recurrent problems of noise and data transmission.*







2- R&D: new acquisition for CTF3/CLIC

Motivations for a new development:

We met problems with analog memory sampling and network transmissions.
Logical evolution dedicated to a larger accelerator as CLIC:
Rare acces from surface, high number of channels, rad-hard, low-cost, low consumption, all-around accelerator standard acquisition.…
We got experience and we are committed in accelerators.

Since spring 2009:

first discussion with CTF3, definition of possible future solutions:
→ elimination of last copper links: use of optical link network.
→ A crate including ~ 6 acquisitions, 1calibration, 1power supplies, 1network switch.

Selection of 2 ADCs, design of an evaluation board.
→ last summer tests and specifications discussions have concluded to a 100Msps/12 ENOB solution.
Design of a local calibration current generator with a first prototype last summer.
→ Tests validated the solution: adjustable up to 10A pulse.

Tests on optical links shown the possibility to use the carrier to transmit the machine clock.

2- R&D: new acquisition for CTF3/CLIC

It brought to a meeting with CLIC for a definition of possible collaboration.
CLIC and CTF3 needs are converging: 4 objects to acquire per module or crate.

As these objects are hard to define now, our approach is to propose a "state-of-the-art" solution which could be a first step to a larger acquisition system: a paper is being currently finalized.

A meeting with CLIC based on this proposal is foreseen next month to fix the bases of the collaboration.

Last studies fixed a simpler architecture proposal:

Single acquisition board 4X4 channels possible for the whole module:
→ direct electrode sampling: no more analog module.
→ only one acquisition board, only one FPGA, only one SFP link.
→ huge cost reduction: components, PCBs, hardware…
→ no more local crate collection board (switch): one less network level,
no more front panel cabling.

2- R&D: new acquisition for CTF3/CLIC

Next crate simpler:

4X4 Acquisition board directly linked to the network.

Calibration board controlled by the FPGA.

Autonomous power supplies.

- ***Acquisition board:*** *4 quad ADCs, 1 FPGA.*
  Foreseen sampling: ***100Msps*** *(10ns),* ***14bits***, ***12ENOB.***
  → Quad ADCs allow good CMRR and low clock skew between channels.
  → Simple analog stage: attenuation/gain before ADC.

  Possible local FPGA processing: deviations, averages, auto-trigger, droop compensation…

- ***Calibration board:*** *adjustable current pulse up to* ***10A***.
  → Regulation using a µcontroller linked to ADC FPGA.
  → output multiplexing 1 current to 8 electrodes.
  → disabled when not used to limit power consumption & EMI problems.

2- R&D: new acquisition for CTF3/CLIC

- ***Autonomous power supplies:*** *local AC-DC converter from 220V line to 12VDC.*

- ***Network :*** *in both case of synchronous or asynchronous acquisition with machine clock, we think that the network should be in a tree configuration:*

  Broadcast descending network.

  Point-to-point ascending network.

  → needs to be connected and compatible with the future solution supported by CERN as ***White Rabbit****.*

First step: *development of a PCI-express transmission board.*

Second step: *development of a data collection board (switch) for network tree.*

Radiations issues: *the choice of rad-hard components is very reduced;*

→ use of components known for their rad-tolerance.

→ digital with specific design techniques: triple voting, small technos…

→ CTF3 will be a good test area.

→ Qualification based on specifications in the future.

→ Infrastructure possibilities have to be studied.

2- R&D: new acquisition for CTF3/CLIC

Milestones

End 2009: definition of the collaboration, final technical discussions.
Mid 2010: crate with ADC board, calibration, power supplies.
Tests and debug with already existing evaluation PCI board.
Fall 2010: PCIe network board.
Tests and debug of the full chain, tests in CTF3.
Could update the current CTF3 acquisition.
Fall 2011: local network switch.

LAPP resources:
for the next two years 3 men FTE and IN2P3 funding ~30k€/year.

CTF3 is a first step and the good place to develop such a system.