SOI Pixel Technology

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SOI Pixel Collaboration

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INFN Padova : D. Bisello, S. Mattiazzo, D. Pantano
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SOI Pixel Detector

Radiation

Circuit

SOI layer
~40 nm

PMOS

NMOS

BOX
(Buried
Oxide)
~200 nm

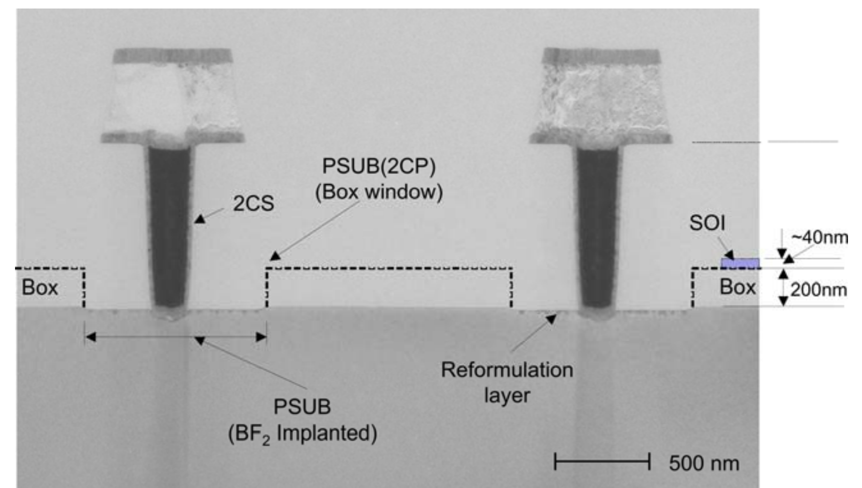
SiO_2

n+

p+

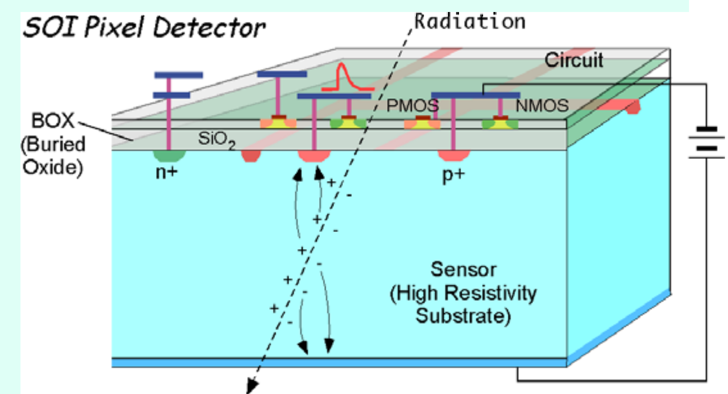
30 μm
~ 600 μm

Sensor
(High Resistivity
Substrate)



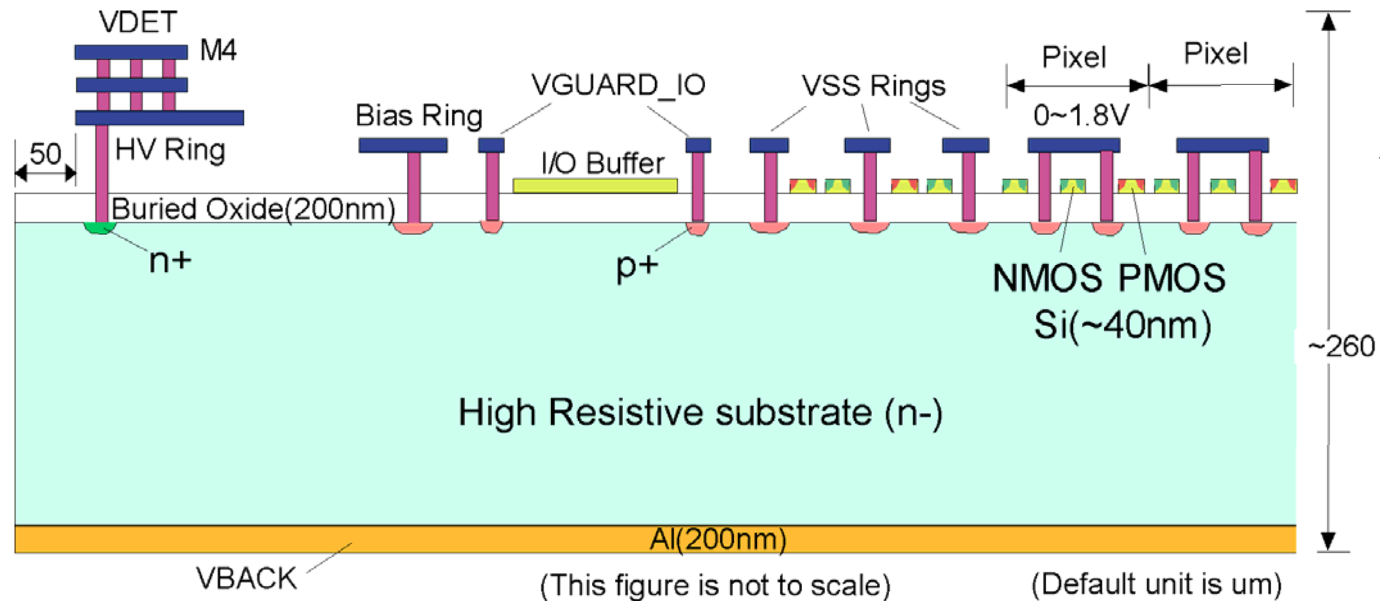
Features of SOI Pixel Detector

- *Truly Monolithic Detector*
  - -> High Density (pixel size of a few μm may be possible).
  - -> Less material and can be Thin (~30 μm).
- *Standard CMOS circuit*
  - -> Complex functions can be implemented in a pixel.
- *Seamless connection to Vertical Integration*
  - -> More functions will be packed in a pixel.
- *Based on Industrial standard technology*
  - -> Easy mass production, Less Cost, Scalable.
- *Less parasitic capacitance*
  - -> Low power, High speed, High Gain.
- *Thin active Si layer (~40 nm)*
  - -> No Latch Up, Small SEE Cross section.
- *No Bulk Leakage current*
  - -> Wide Temperature (4K-300C) operation



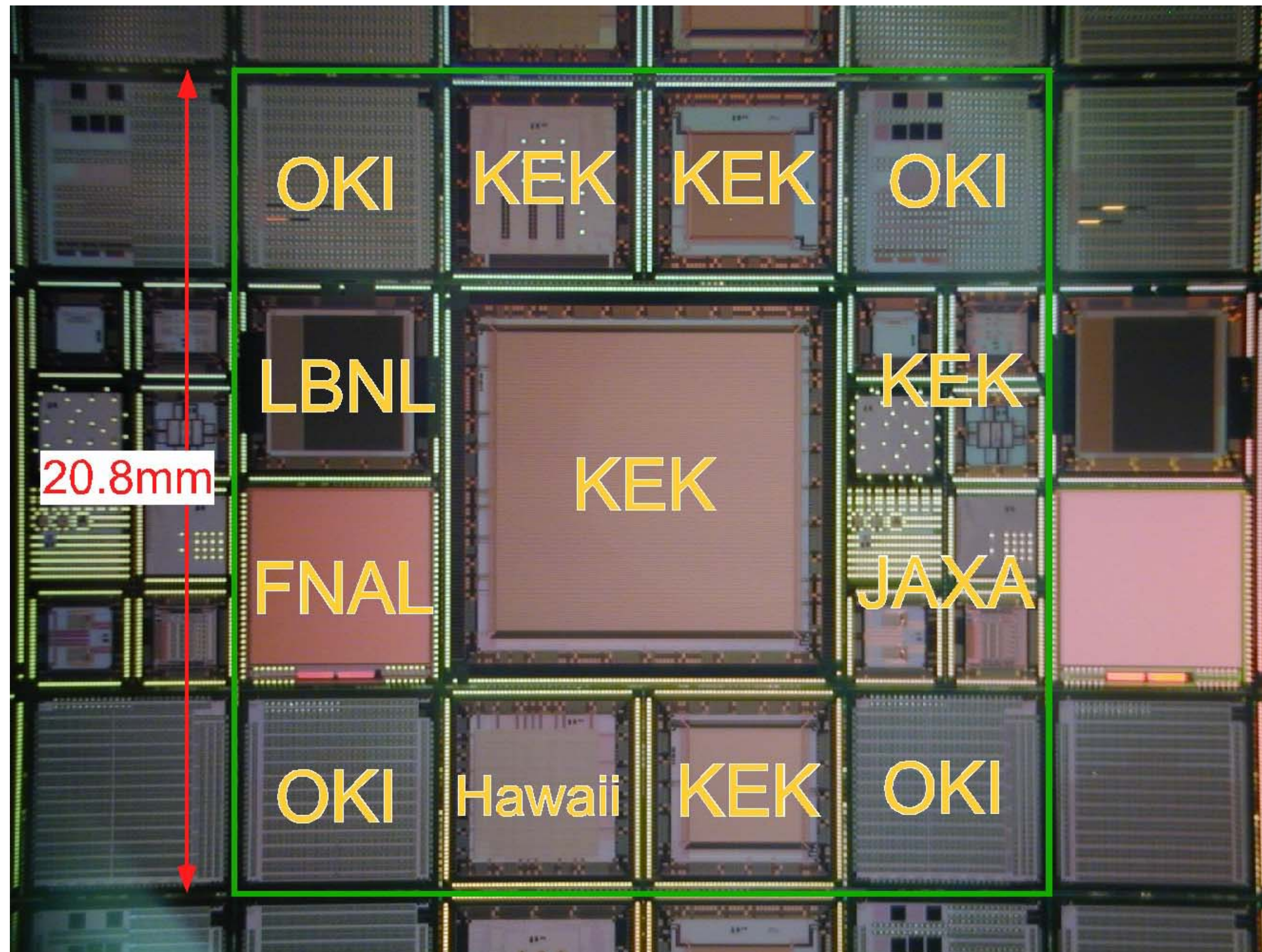
OKI 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI Semiconductor), 1 Poly, 4 Metal layers, MIM Capacitor, DMOS option, Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmφ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、700 Ω-cm (*n-type*), 650 μm thick
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).



An example of a SOI Pixel cross section

KEK SOI Multi Project Wafer (MPW) run

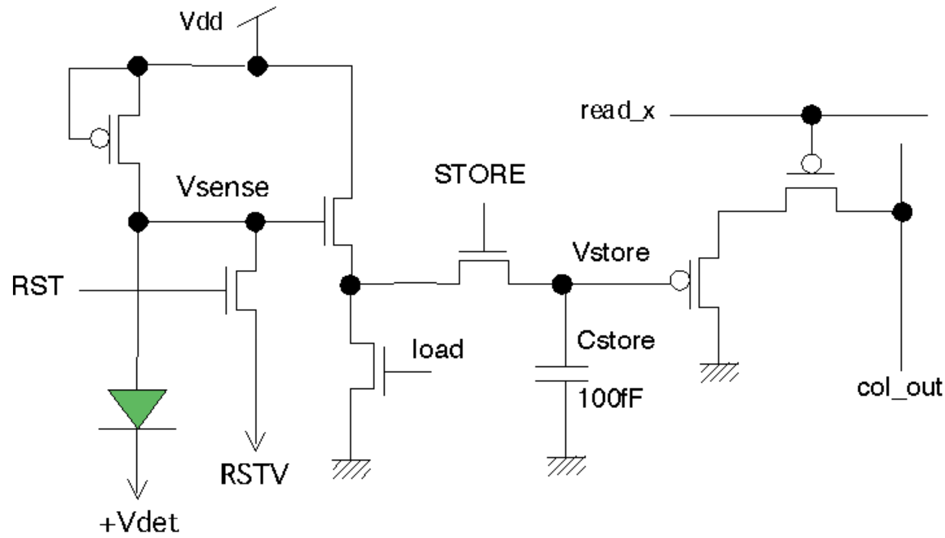


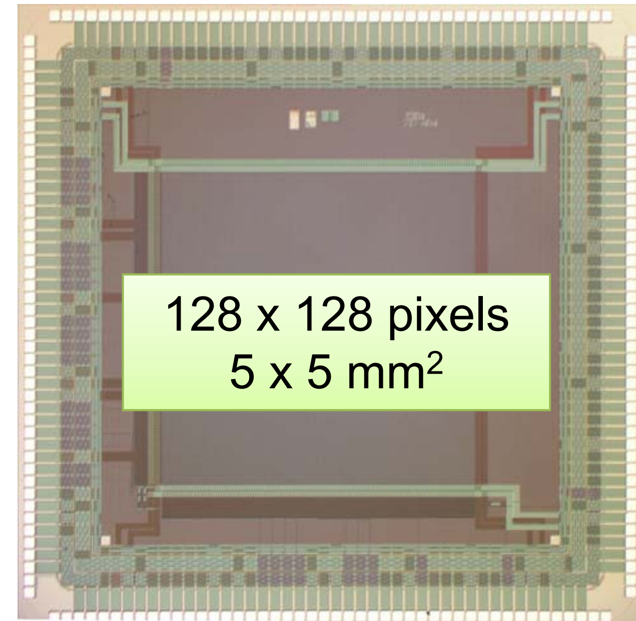
We are operating regular MPW runs.

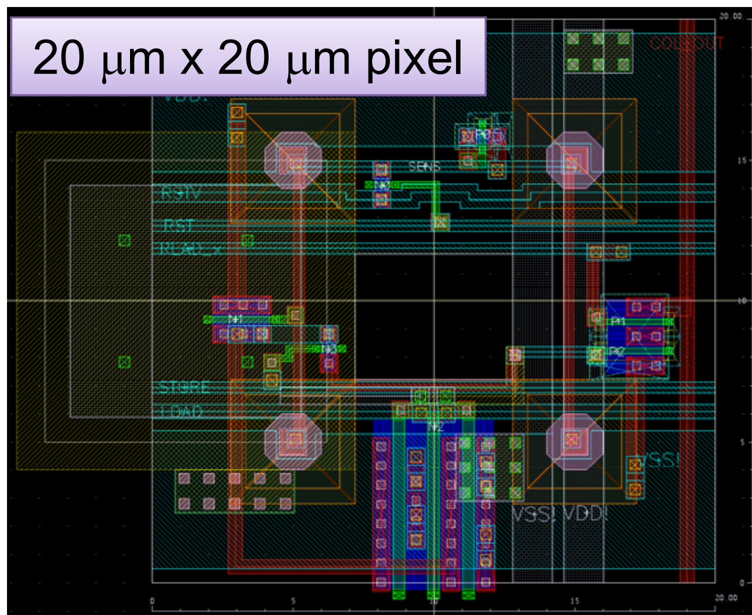
3 MPW runs are scheduled in this fiscal year.

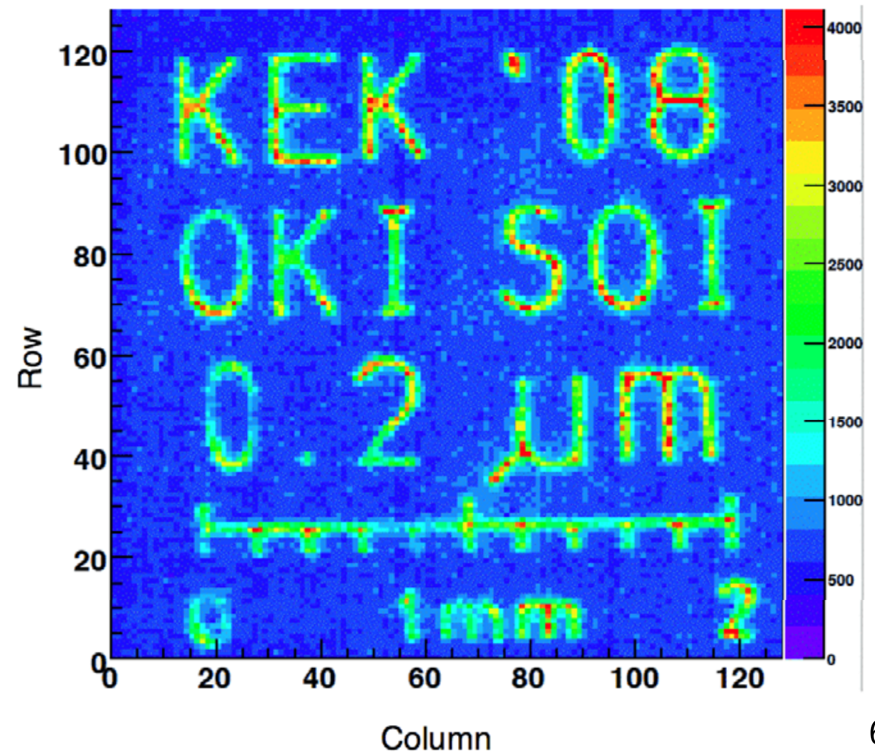
http://rd.kek.jp/project/soi/MPWrun/

Integration Type Pixel (INTPIX)







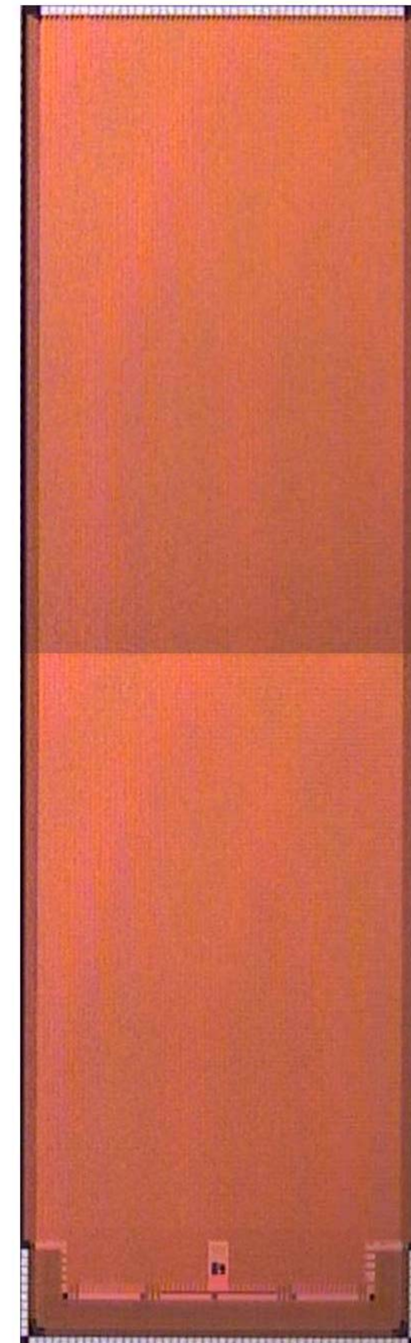


Counting Type Pixel (CNTPIX)

Energy window and counting in each pixel.

5 x15.4 mm^2
72 x 272 pixcels

test_in
Vfb
Dual Discri
xout
write
Data
Counter
yo
VthH
Double Discri Logic
16bit Counter
CLK
Charge Amp
VthL
16
rst
se
csl
fineH 3bit
fineL 3bit
9
Control Registers
+Vdet



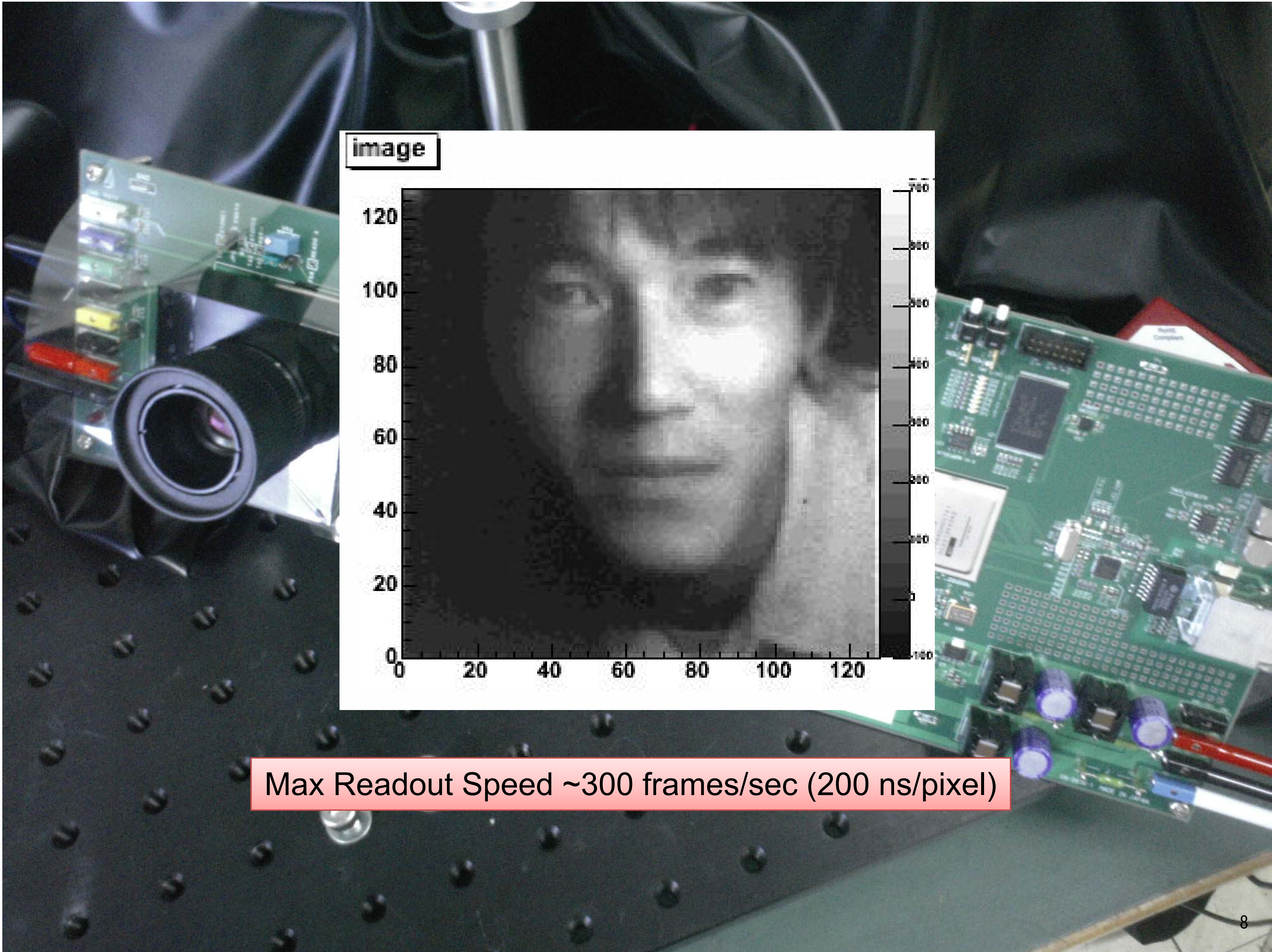
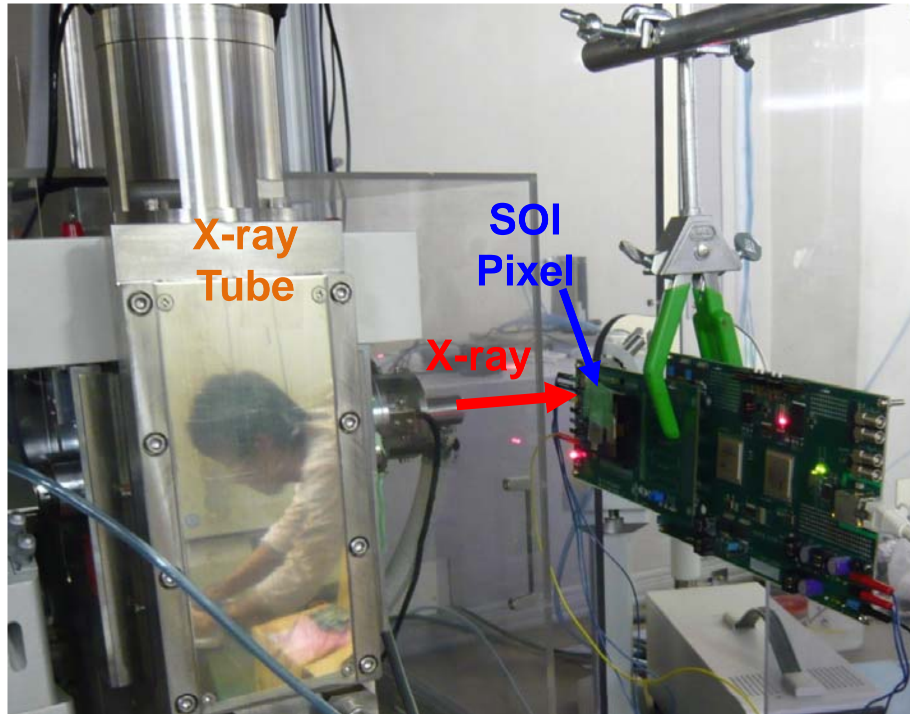


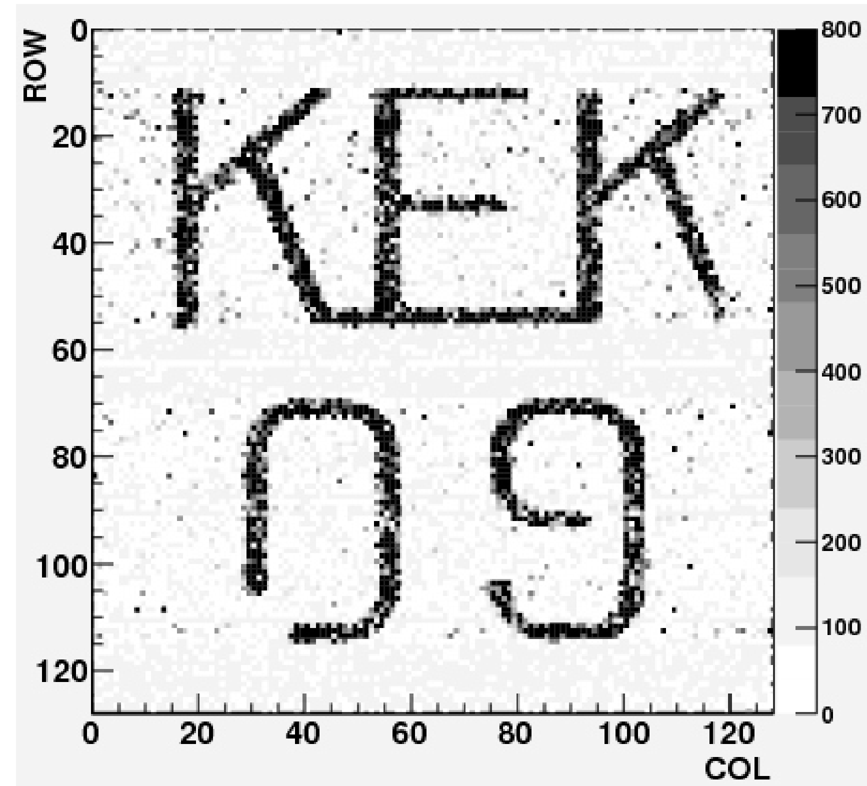
image
120
100
80
60
40
20
0
0
20
40
60
80
100
120
Max Readout Speed ~300 frames/sec (200 ns/pixel)

SOI pixel Laser Image (CNTPIX2)



40kV-40mA
Substracted by background count
Integration time 64ms / vth 350mV
Vback=15V

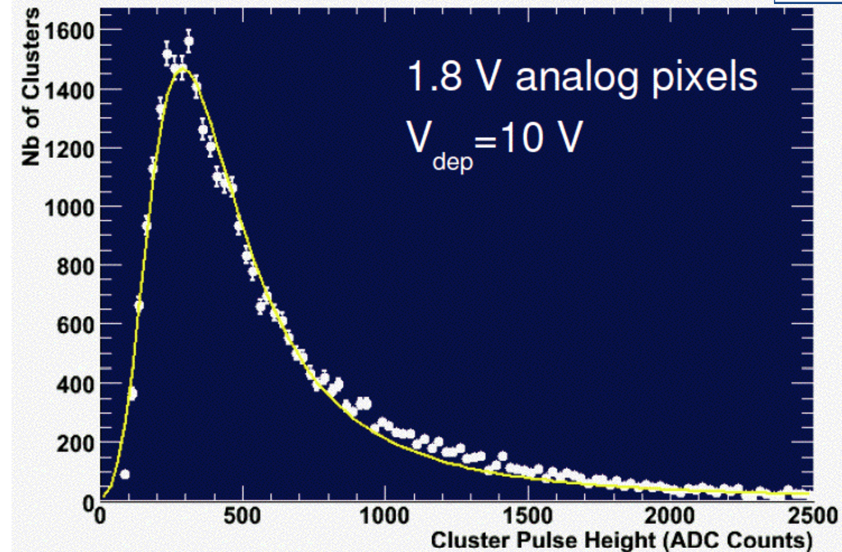
•Image taken by X-ray irradiation



Counter works well

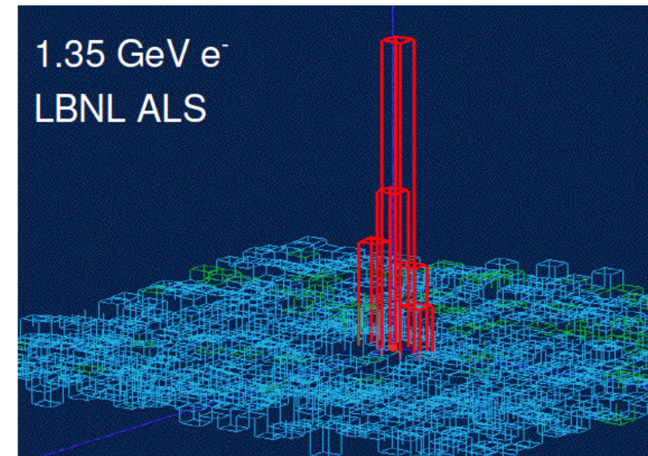
Electron beam-test: analog sectors

- 1.35 GeV e^- beam extracted from the injection booster at the LBNL Advanced Light Source
- First successful high momentum particle beam test on SOI monolithic pixel sensors
- As a function of the increasing V_{dep}: cluster pulse height increases and cluster multiplicity decreases, up to V_{dep}~10 V, consistent with lab tests and back-gating effects becoming important at V_{dep}=10 V



1.8 V Analog Pixels				
V_d (V)	Clusters / Spill (Beam on)	Clusters / Spill (Beam off)	Signal MPV (ADC Counts)	Average Signal/Noise
1	9.7	0.05	132	8.9
5	14.0	0.12	242	14.9
10	7.8	0.20	316	15.0
15	3.9	0.01	301	13.6

[NIM A 583 (2007) 526-528]

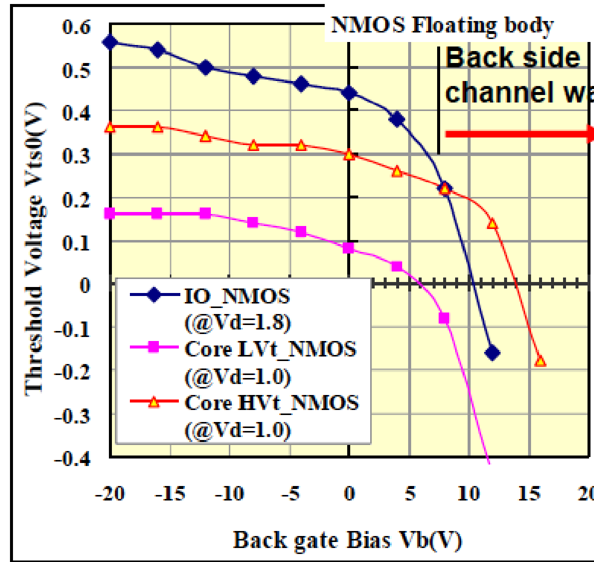


Threshold Variation

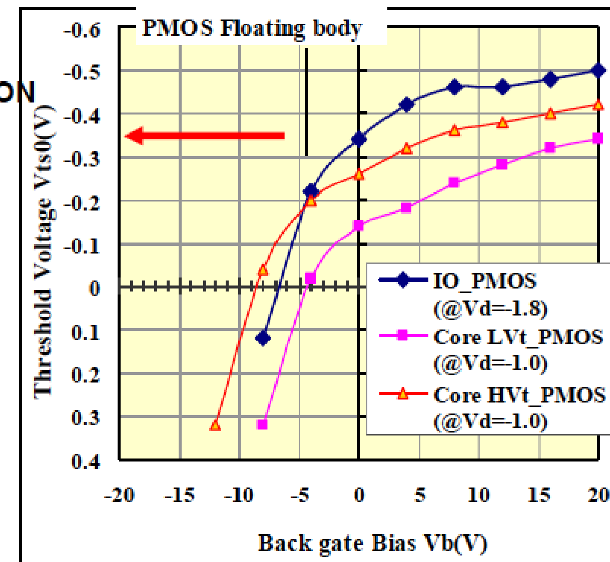
SOI Issue:

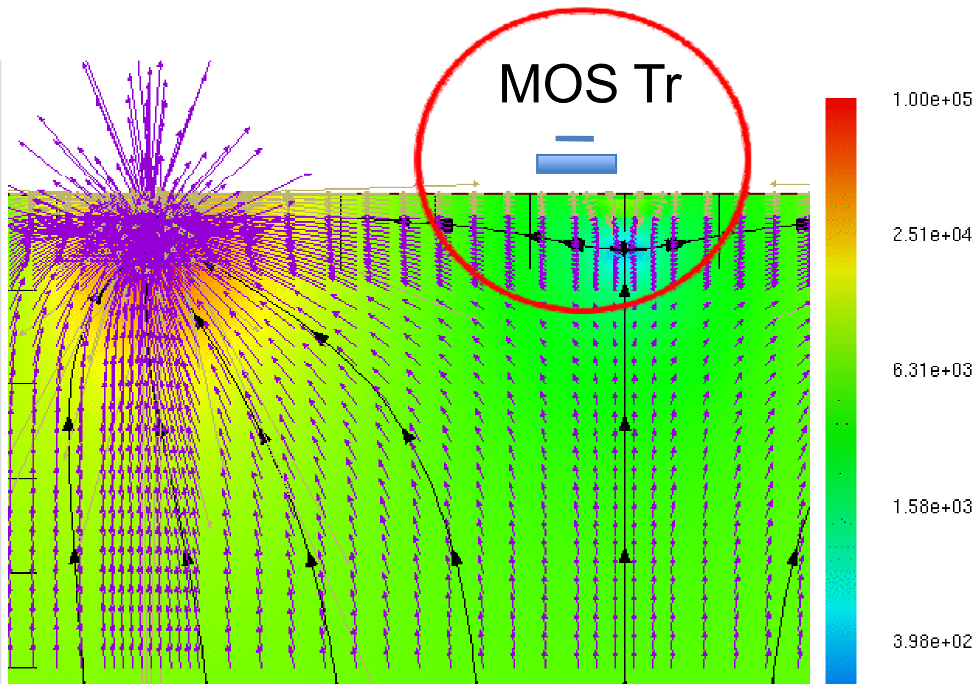
Back Gate Effect

NMOS transistor



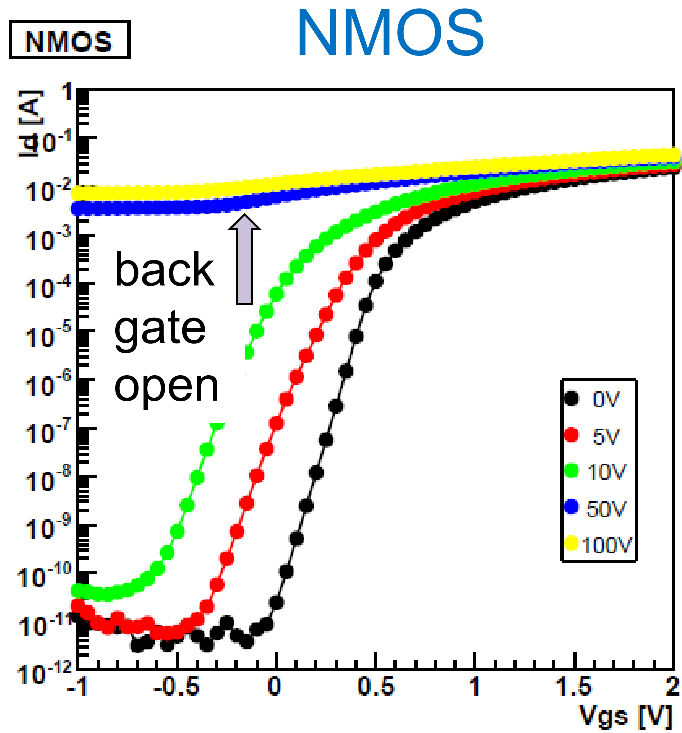
PMOS transistor

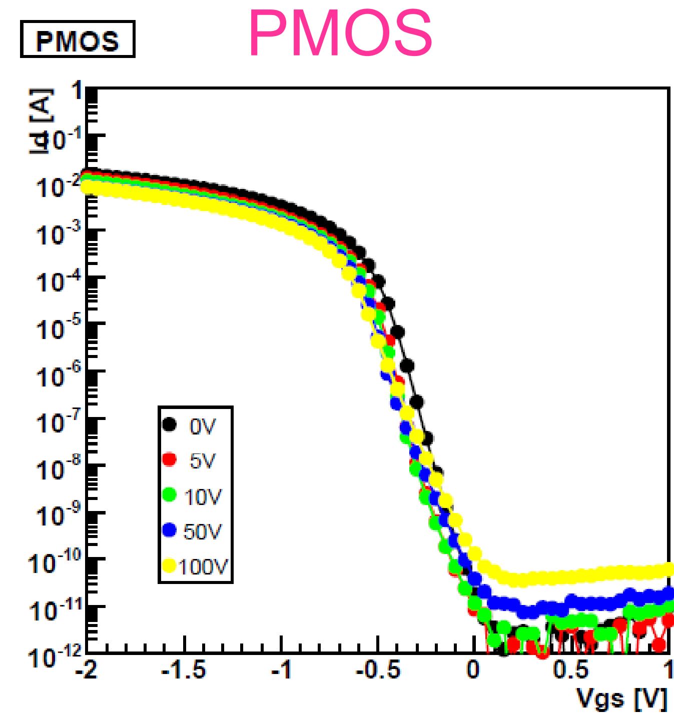




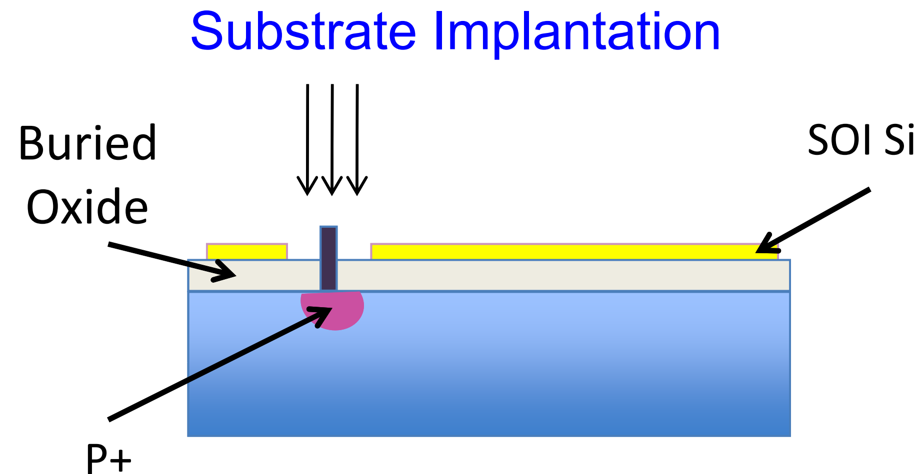
Substrate Potential act as Back Gate, and change transistor threshold, increase leak current of Tr.

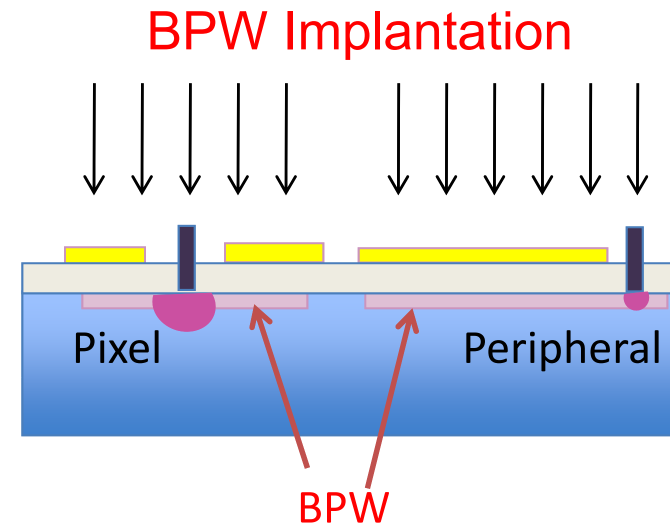
I_{ds}-V_{gs} curve under back bias





Solution to Back Gate isue : Buried p-Well (BPW)





- Cut Top Si
- High Dose

- Keep Top Si not affected
- Low Dose

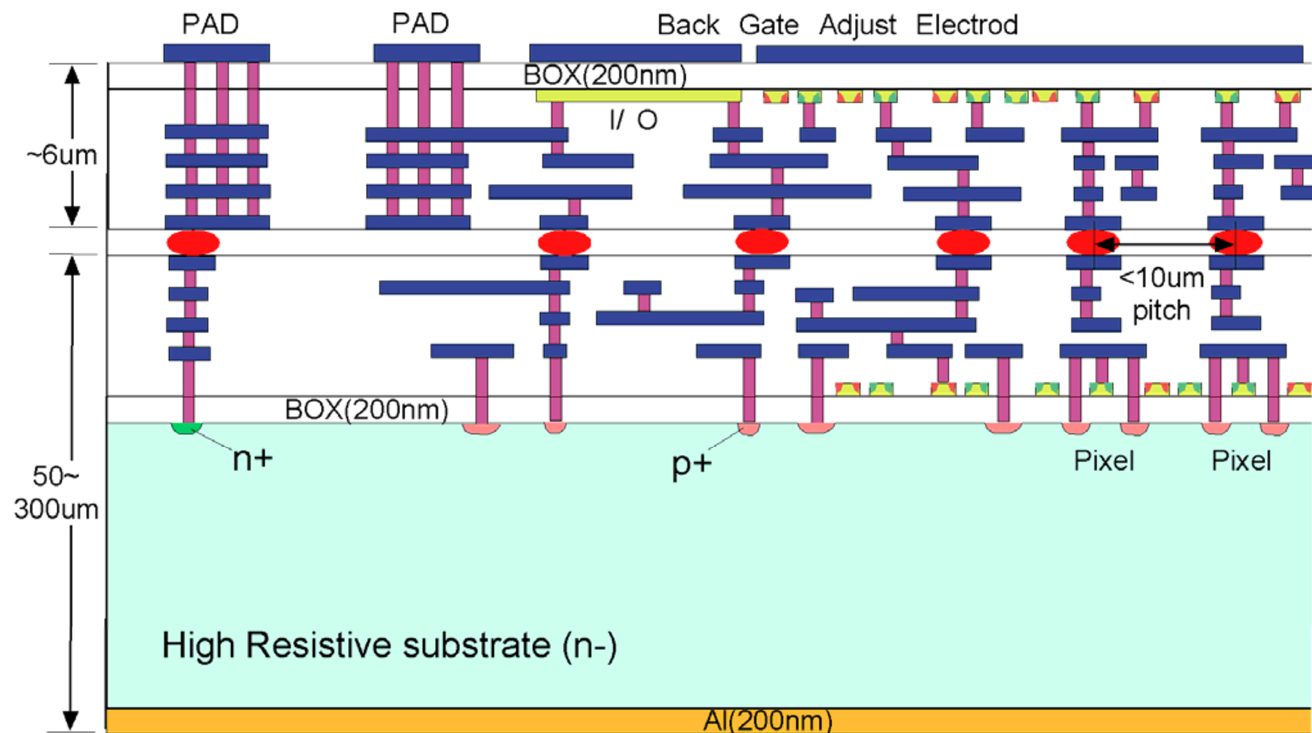
- Suppress back gate effect.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage.
- Less electric field in BOX which may improve radiation hardness.

Vertical Integration

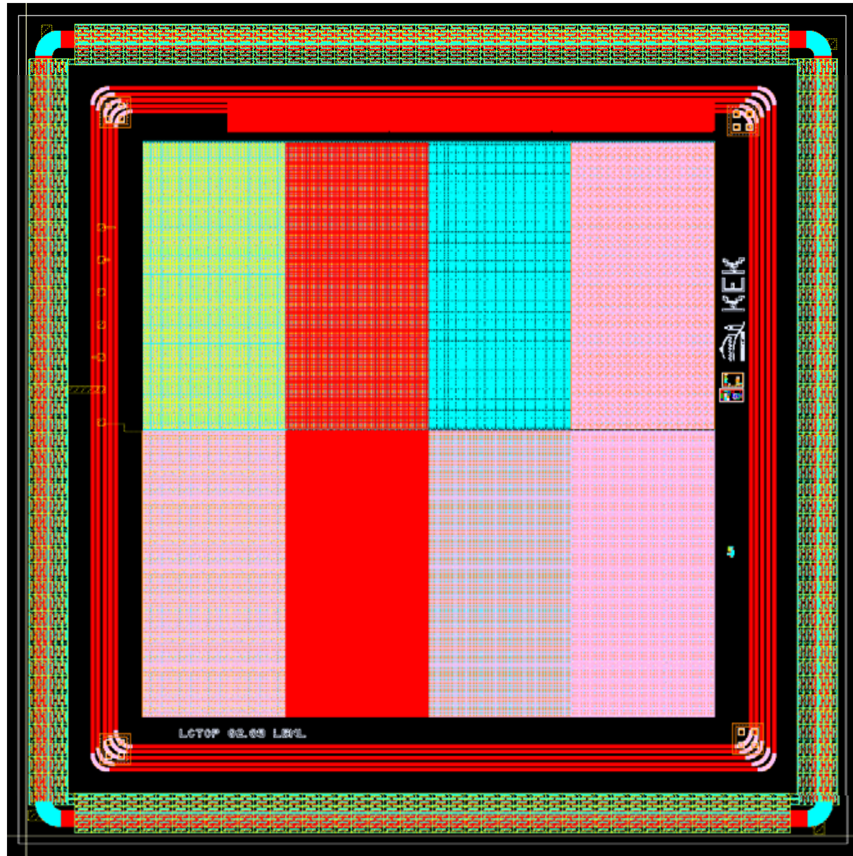
KEK/LBNL+OKI+ZyCube

aiming Higher Integration Density, Increase Radiation Tolerance, Lower Power Consumption, ...

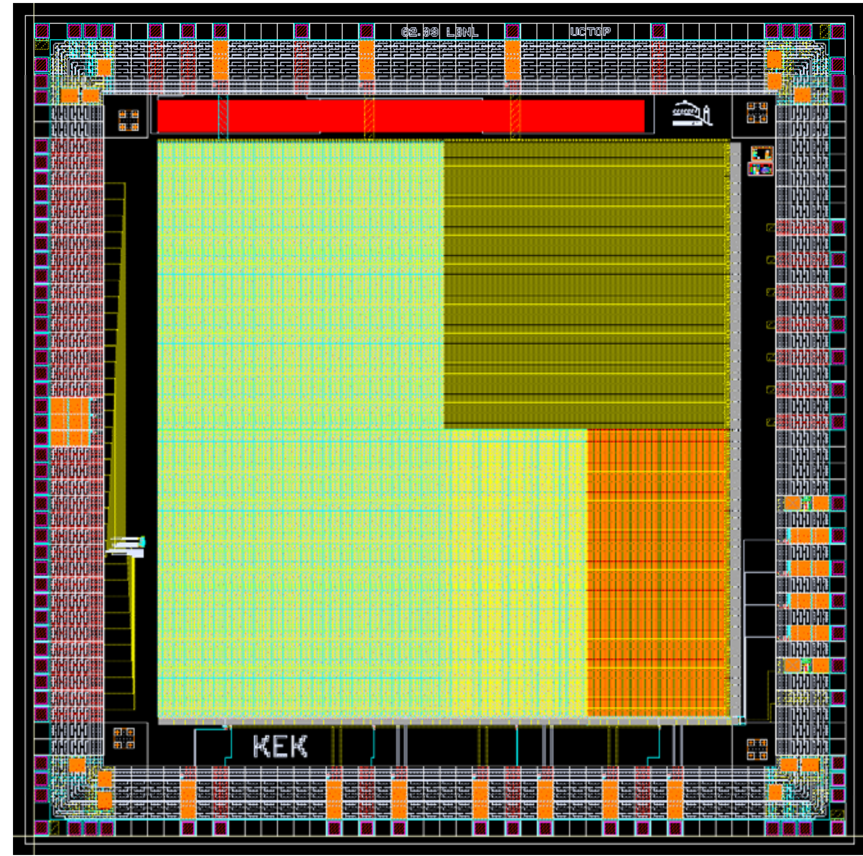
- First test chip designed by LBNL/KEK for Feb. '09 submission.
- Bonded by ZyCube μ-bump bonding (~5 μm pitch) technique.



Vertical Integration



Lower Chip



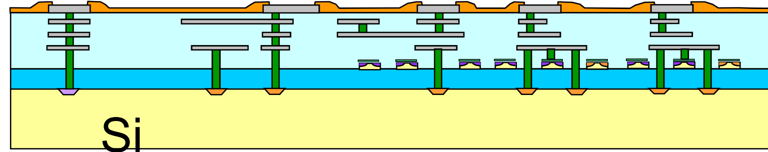
Upper Chip

Process Flow for SOI Pixel Detector

Lower Chip

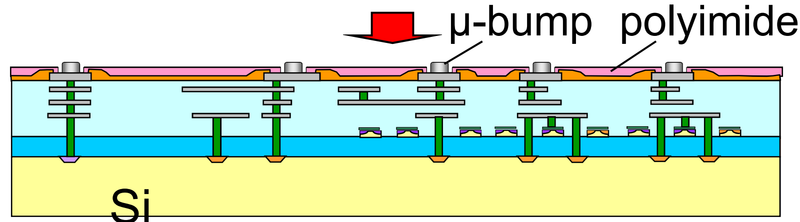
FD-SOI + MIM capacitor +DMOS
1 P4M process
Core (I/O) voltage= 1.8(3.3) V
8”Φ SOI Technology
Si :CZ , p-type 18ohm,tsi=40nm
BOX:tSiO2=200nm

- Starting LSI



μ-bump polyimide

- Form μ-bump

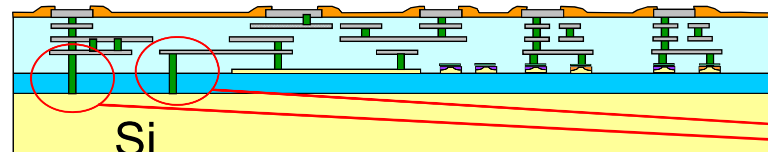


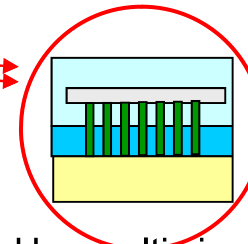
Next page (Stacking)

Upper Chip

(Layout must be done with mirror inverted)

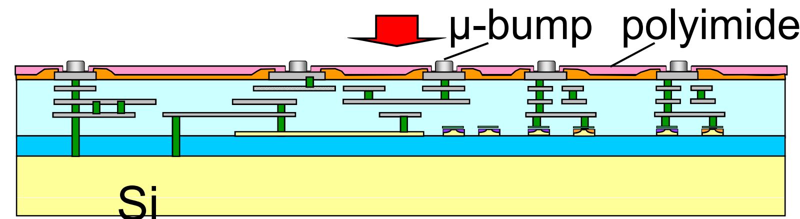
- Starting LSI





μ-bump polyimide

- Form μ-bump



Next page (Stacking)

Use multi via structure for contact path between 1metam and bond pad dia./space 0.32/0.6μm
In left figure, single via is used for simplifying the cross section

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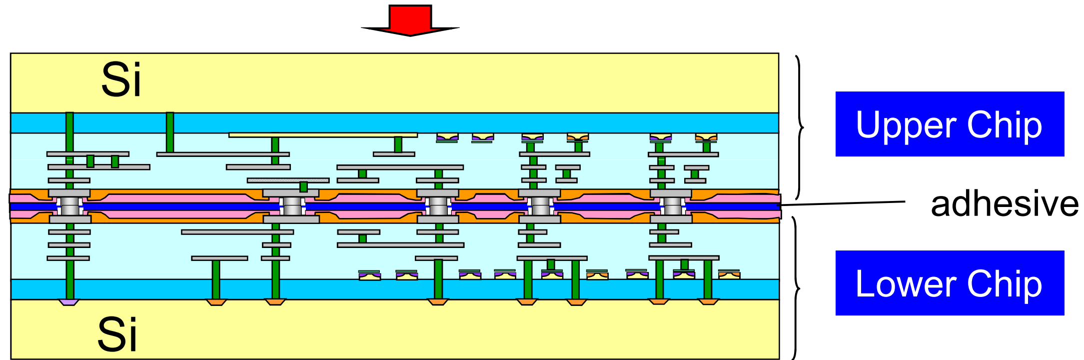
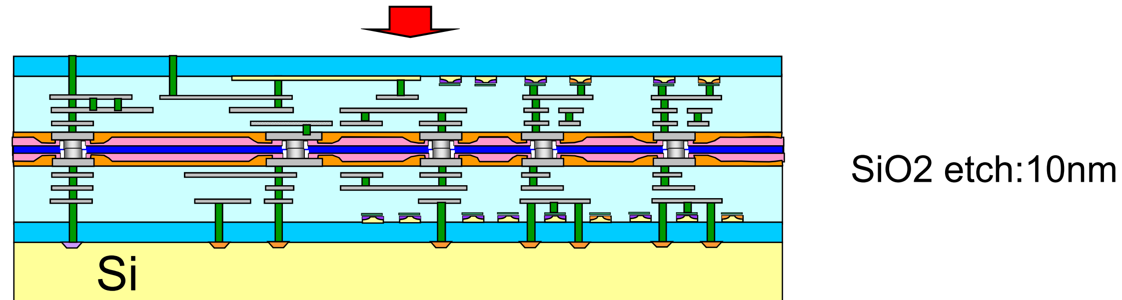
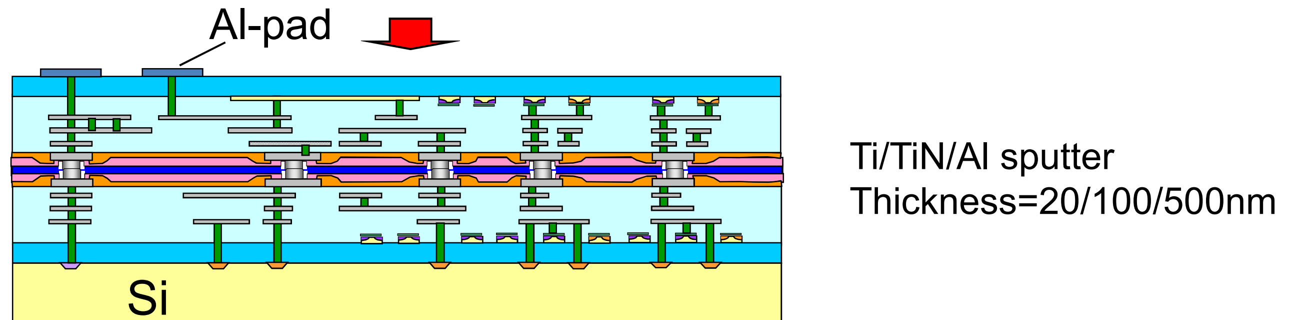
-Stack wafer (Chip) with μ-bump and adhesive



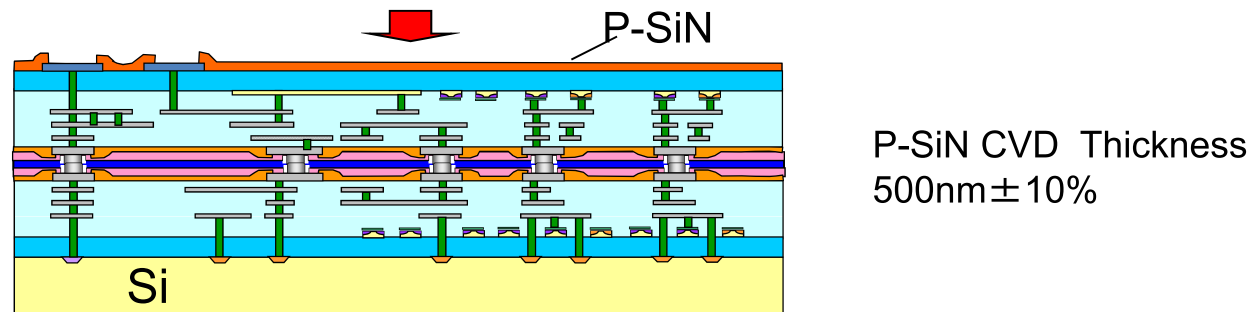
-Si etch
-SiO2 slight etch



-Ti/TiN/Al sputter
-Metal Pad Litho.



-P-SiNd deposition
-Pad Litho.



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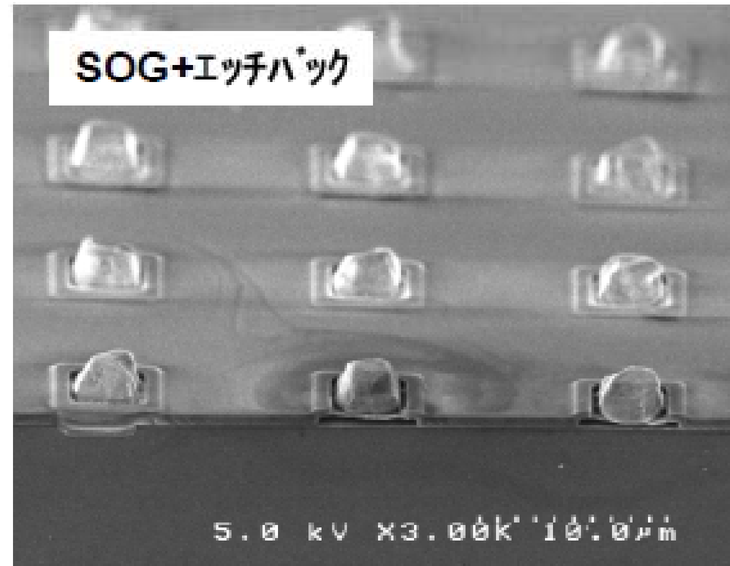
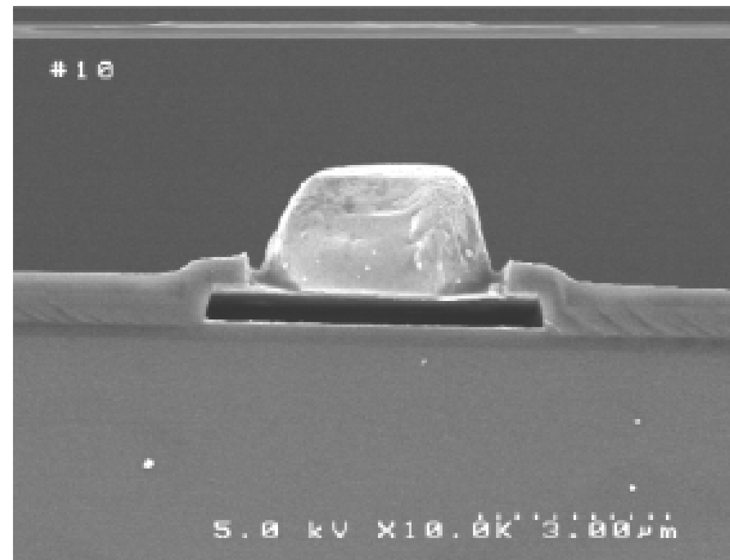
μ-bumps fabrication





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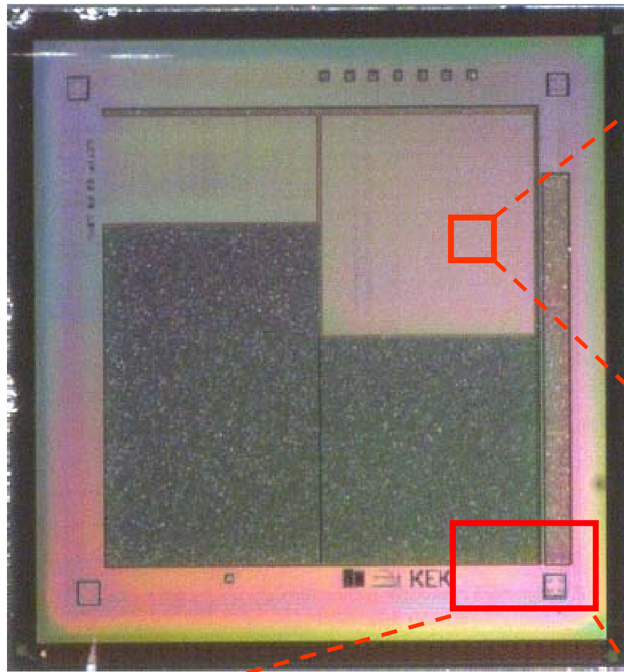
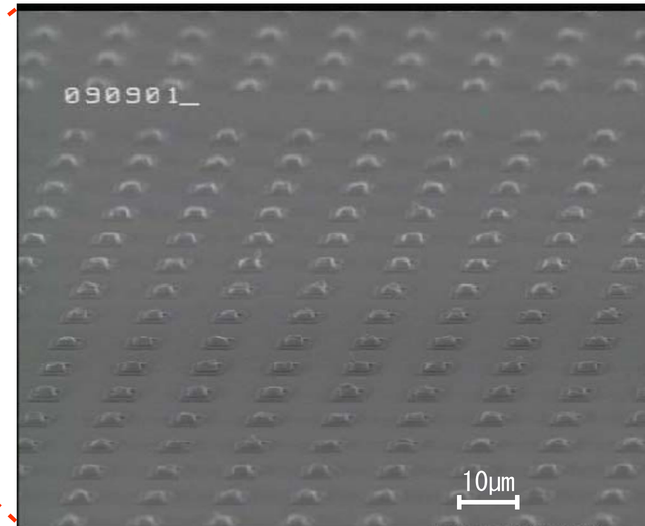
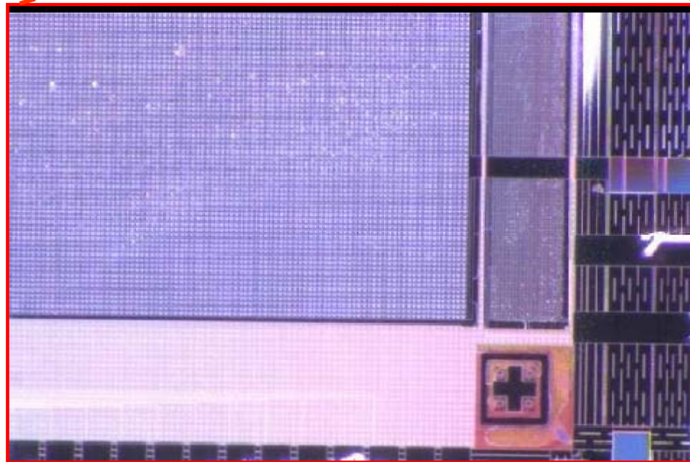
3D-SOI pixel Detector : Stacking



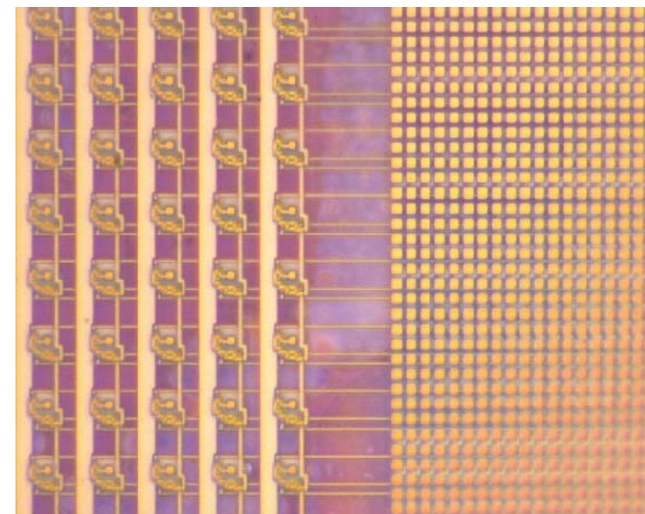
Before stacking (Upper Chip)



Detector Array (before stacking)



After stacking



Detector Array +Peripheral Circuits (After stacking)

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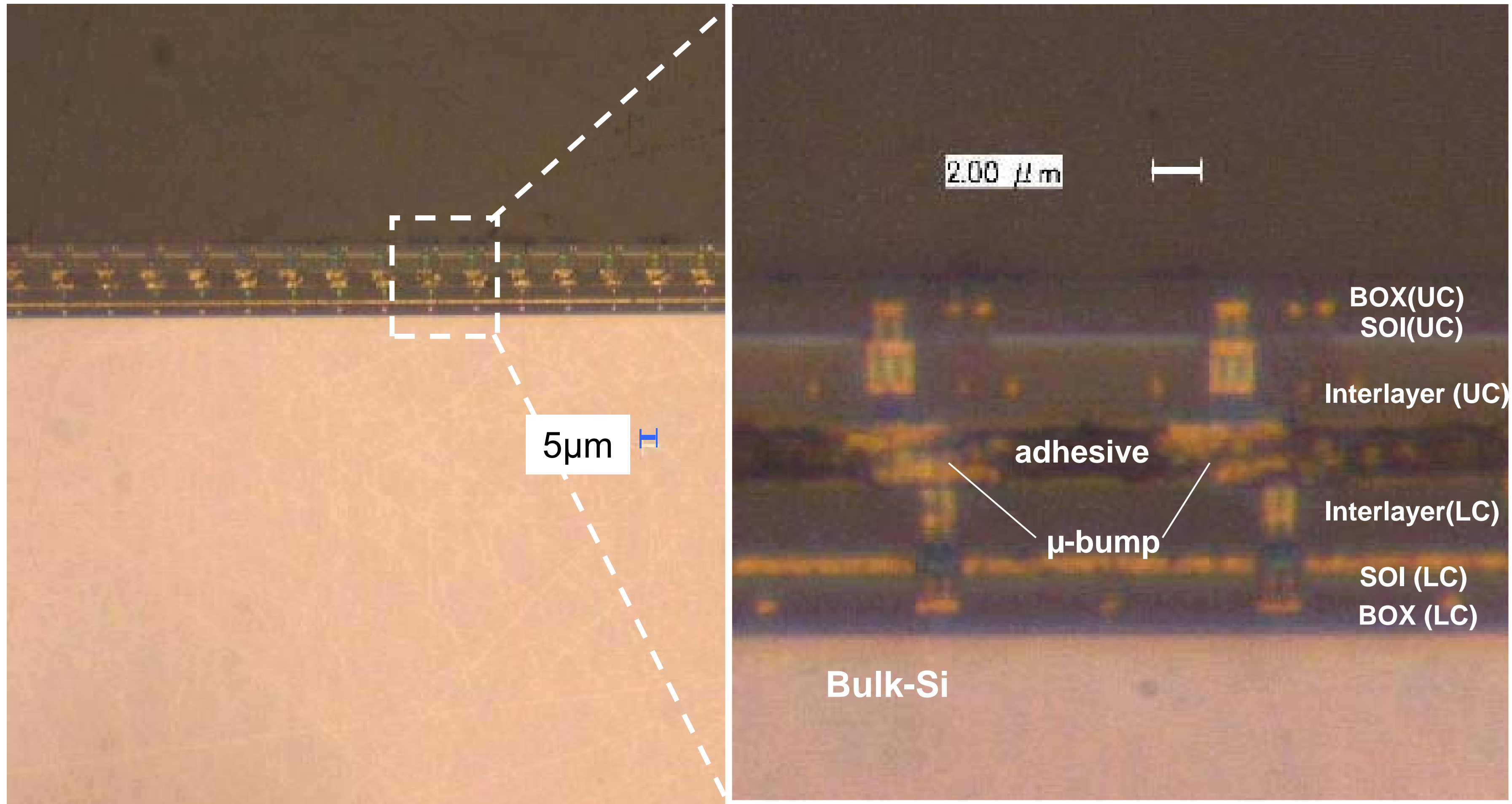
Cross sectional view of detector array (After stacking)



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Summary

- Our SOI pixel process has many attractive features for the Linear Collider applications; Low Material budget, Complex Function in a pixel, Low Power, ...
- Back gate effect exists in SOI pixel is successfully suppressed by introducing Buried P-Well technology.
- We are operating regular MPW runs; there are 3 MPW runs in this year
- Vertical integration is natural extension of the SOI technology and well-suited to the SOI process.
- First vertical integration test chips are bonded by using ZyCube μ-bump technique and will be tested soon.