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Fast Pixel Detectors

CLIC requirements

resolution:
- pitch: 10 µm (binary)
  - 25 µm (analogue)

occupancy: (3 cm)
- frame readout: 10 µm pitch
- or
- 25ns time resolution for 25µm pitch

power: 100 mW/cm²
- duty cycle: 150 ns on every 20ms
- even for 100µs readout time: 1:200
- => 20W/cm² with power cycling

pattern recognition
- time stamp: 25ns

material: <100µm Si

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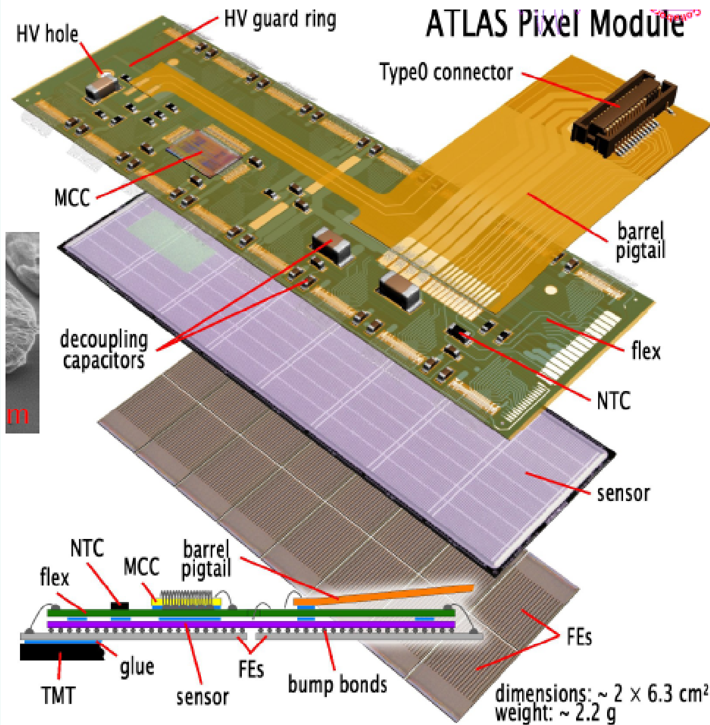
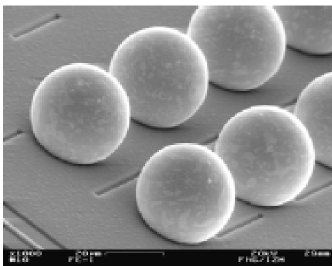
State of the art: hybrid pixels

Face to face interconnection: ASIC - Sensor



Definitely not low mass!



Granularity (resolution, occupancy)
- bump bonding limits pitch to O(50 μm)
- Pixel area 10000 μm²
- (CMOS 0.25μm) 50x400 μm²

Readout speed:
- **25ns BX identification**
- complex processing (pipeline)

Thickness
- Thick! (250 μm Sensor + ASIC + interconnect)
- large signal needed!

Power 200 mW/cm² (liquid cooling)

Fill factor (low mass)
- 71% (ATLAS)

Add functionalities (calibration, 0-suppression, clustering)
- ok, especially going to even smaller DSM

Radiation hardness
- Yes (till 10^{15} n/cm²)

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Monolithic Detectors

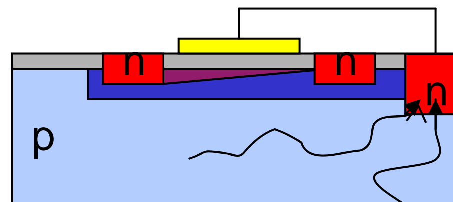
Integrate readout electronics (amplification) into sensor

no interconnection
low mass

Examples:

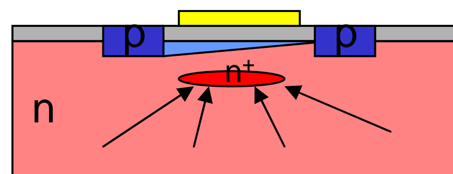
CMOS sensors (MAPS)

'standard CMOS' process
use un-depleted epi layer as sensor
complex CMOS circuit (limited to NMOS)
small signal, slow charge collection



DEPFET

depleted bulk
fast, large signal
limited signal processing



Fairly different detector architectures
In common:

low mass => ideal for high precision detectors
slower than hybrid pixels
moderate radiation hardness
(ok for e*e-, not for pp)

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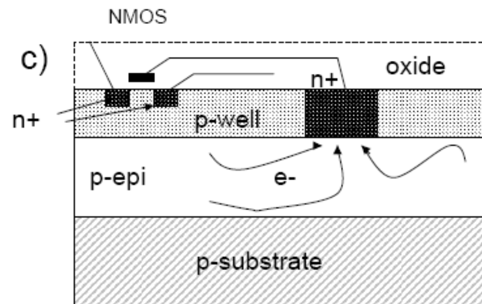
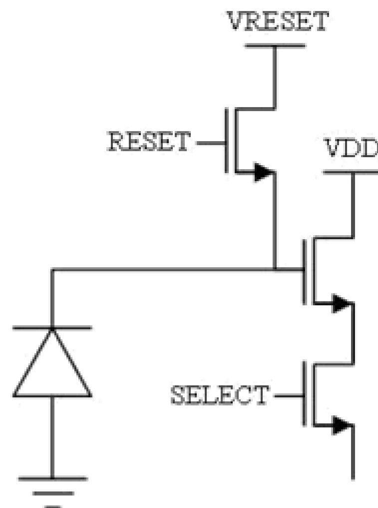
CMOS Sensors

Charge collection by diffusion (in un-depleted epi layer)
CMOS readout electronic integrated. Small signal, yet S/N > 20)



Performance limited by NMOS
Use only:
slow, no complex processing



Granularity (resolution, occupancy)
- 10 µm pitch (MIMOSA18)

Readout speed (complex processing)
- slow charge collection by diffusion
- frame readout (100 µs)

Thickness
- <100µm (small signal anyway)

Power
- low (depends on speed and complexity)

Fill factor (low mass)
- low (periphery), tiling, stitching

Add functionalities (calibration, 0-suppression, clustering)
- difficult (only NMOS transistors)

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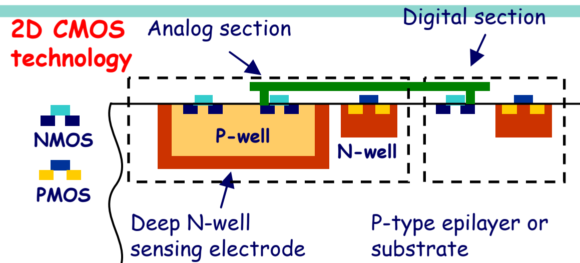
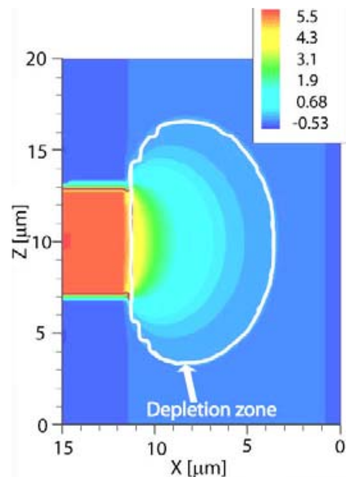
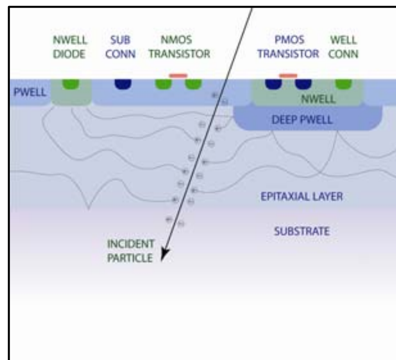
Advanced CMOS sensors



triple well, deep p-well => full CMOS possible (complex, fast) but still suffers from slow collection of small signal (VIPIX)



High resistivity epi (IPHC) using XFAB-0.6 PIN process
1 kΩcm -> ~ 14 μm depleted
Charge collection within 5 ns



INMAPS (RAL): deep p-well shields PMOS completely
High resistivity substrate (1-10 kΩcm)
10-20 μm depleted
Charge collection within 5 ns

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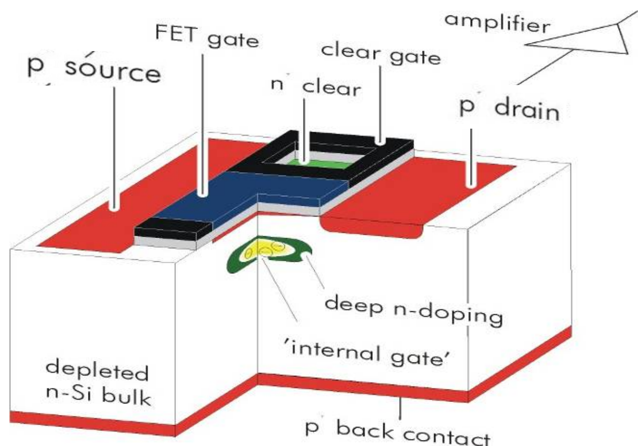
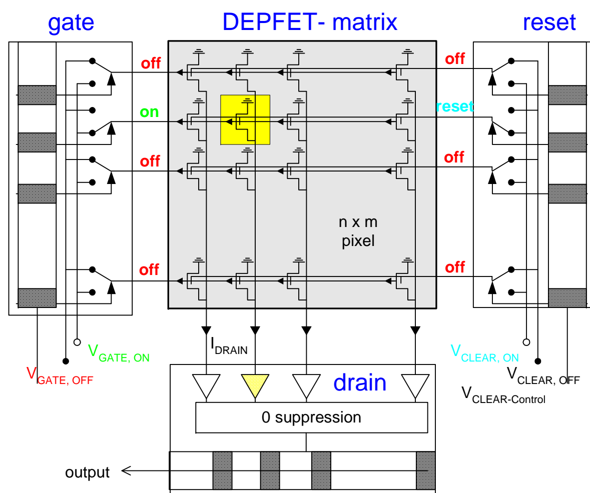
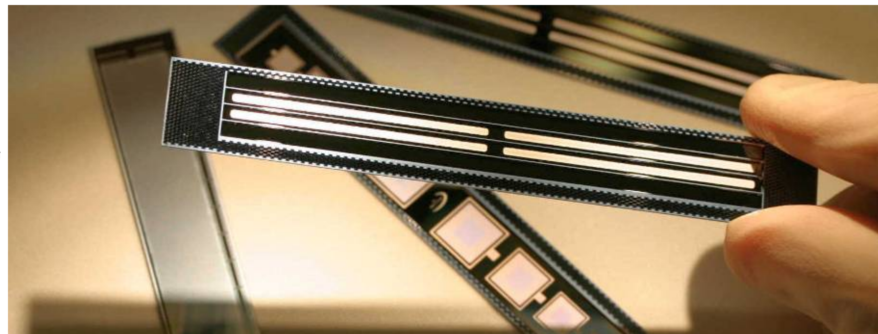
CLIC09
CERN
15. Oct 09

DEPFET

FET on fully depleted silicon
Baseline for Belle II PXD







Granularity (resolution, occupancy)
20µm pitch ok
Readout speed
slow: frame readout O(10 µs)
Thickness
50µm, with good S/N
Power
<100mW/cm² (rolling shutter)
Fill factor
high: monolithic wafer scale sensors
Add functionalities (calibration, 0-suppression, clustering)
No (only in readout ASIC)
Radiation hardness
ok to 10 Mrad

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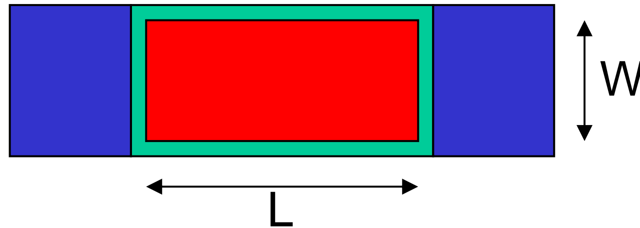
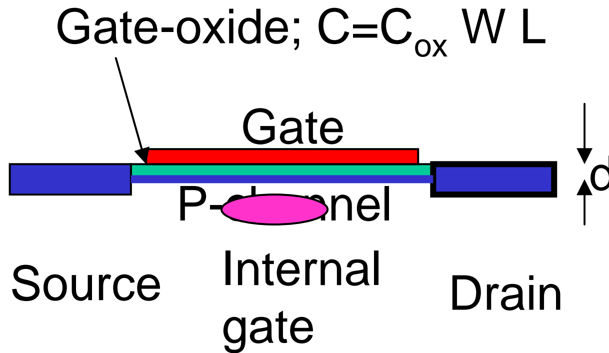
How does it work?





A charge q in the internal gate influences a mirror charge αq in the channel
(α <1, for stray capacitance)
This mirror charge is compensated by a change of the gate voltage:

$\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$

FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G - V_{th}\right)^2$$

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox} W L} - V_{th}\right)^2$$

I_d: source-drain current
C_{ox}; sheet capacitance of gate oxide
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

Transconductance:
Conversion factor:

$$g_m = \frac{dI_d}{dV_G} = \frac{W}{L}\mu C_{ox}\left(V_G - V_{th}\right)$$

$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{ox} W L} - V_{th}\right) = \alpha\sqrt{2\frac{I_d \mu}{L^3 W C_{ox}}}$$

$$g_m = \sqrt{2\frac{W\mu C_{ox} I_d}{L}}$$

$$g_q = \alpha\frac{g_m}{W L C_{ox}} = \alpha\frac{g_m}{C}$$

Intrinsic Noise

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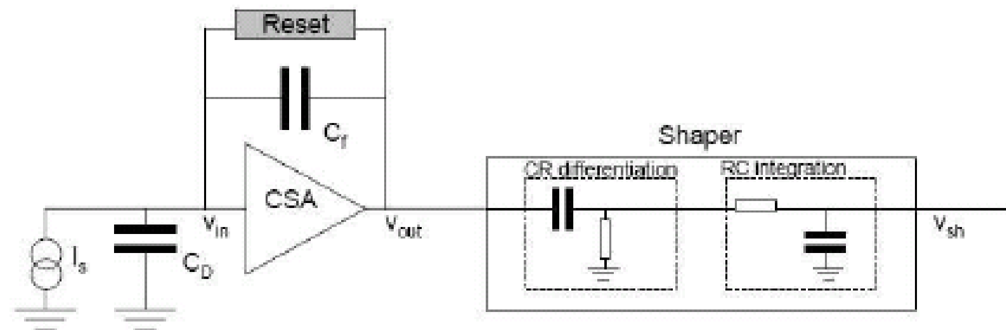
Using: $g_q = \alpha \frac{g_m}{C}$

$$\left\langle ENC^2 \right\rangle = \frac{e^2}{3q^2} kT \frac{g_m}{\left(\alpha \frac{g_m}{C}\right)^2} \frac{1}{\tau} = \frac{\alpha^2}{3q^2} kT \frac{e^2}{g_m} \frac{C^2}{\tau}$$

A similar expression can be deduced for a diode and charge sensitive amplifier (CSA):



$$\left\langle ENC^2 \right\rangle = \frac{1}{3} kT \frac{C_t^2}{g_m} \frac{e^2}{q^2 \tau}$$

However, with C_t: total capacitance (C_D+C_f+….)
(and α = 1, of course)

Achieved: 40e noise at a BW of 50MHz (S/N 100:1 for a 50µm sensor)
However: usually noise dominated by external components

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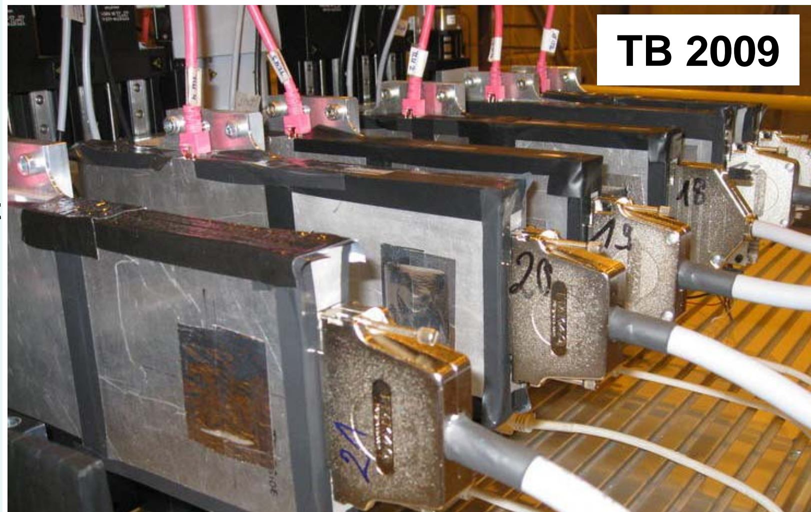
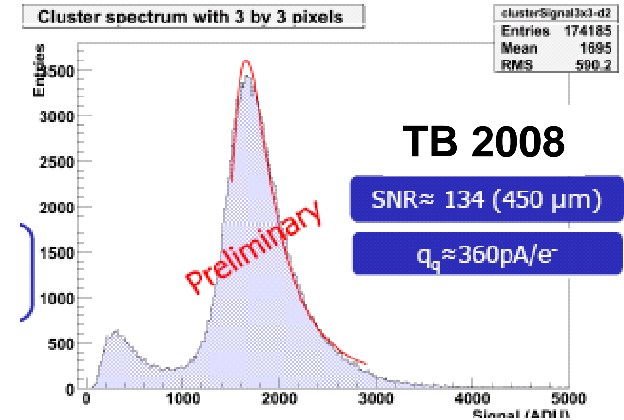
Test Beam





TB 2008	Module 0 CCGME-S90K02 32x24 µm	Module 1 CCGME-90K02 32x24 µm	Module 2 SIMCME-S90K00 32x24 µm	Module 3 CCGME-S90I03 24x24 µm	Module 4 CCGME-S90I00 32x24 µm	Module 5 CCGME-90I00 32x24 µm
X residual [µm]	2.9	2.2	2.3	2.0	3.1	3.4
Y residual [µm]	2.3	1.7	1.7	1.7	2.2	2.6
X resolution [µm]	2.1	1.6	1.9	1.3	2.6	2.4
Y resolution [µm]	1.5	1.3	1.2	1.2	1.8	1.7

Check performance of different designs

32x24 µm²: L=6 µm W=20µm: g_q = 360 pA/e

20x20 µm²: L=5 µm W=10µm:: g_q = 650 pA/e

Results are for ‘ILC’-like pixels (small pitch) and thick detectors

Comparison and tuning of MC simulations => performance at Belle II

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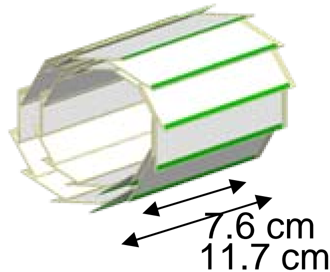
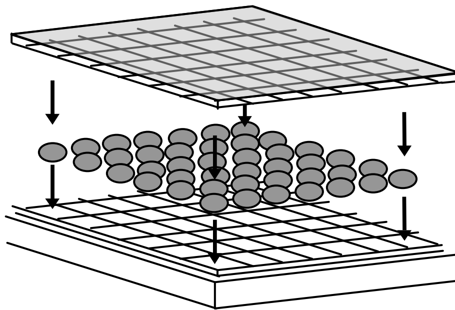
DEPFET Projects



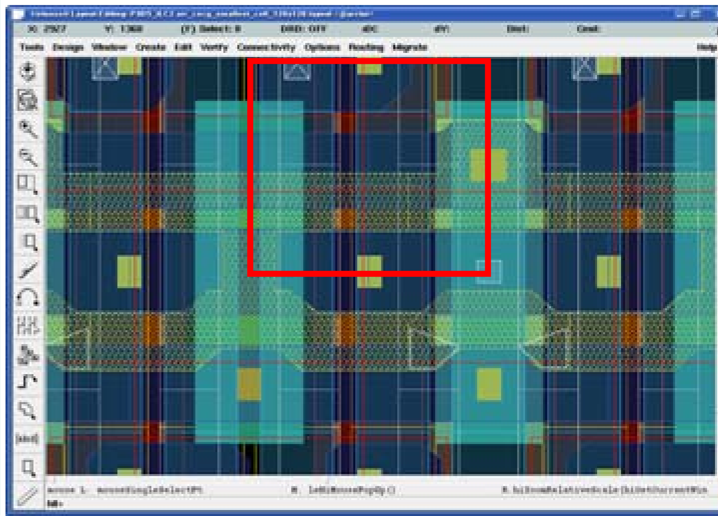
ILC vertex detector: 25x25 µm² pixels, 20µs frame readout, 50µm thick

Belle II vertex detector: 50x75 µm² pixels, 10(20)µs frame readout, 50µm thick



IXO wide field imager (X-ray detector, frame readout)

DSSC x-ray imager for XFEL: 200x200µm pitch, single pixel readout, 200ns time resolution
Bump bonded hybrid technology



Min, size given by Aluminum pitch (8µm)
Smallest cell operated up to now: 20x20µm²
128x128 matrix worked well in TB09

Smaller pixels need improved process technology (plasma etch)

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Intrinsic Speed

File Edit Graph Axis Trace Marker Zoom Tools Help

g20 g21 g22 c00 c01 c02 c10 c11 c12 vids.i

1. row
2. row
3. row

clear
clear
clear

gate
gate
gate

drain current

"1" "0" "0" "0" "1" "0"

V (V)
12.5 10.0 7.5 5.0 2.5 0 -2.5 -5.0 -7.5

I (uA)
25.0 0 -25.0 -50.0 -75.0 -100.0 -125.0

0 50.0 100.0 150.0 200.0 250.0 300.0
time (ns)

48.9906ns | -111.327uA | 91.5929ns | -109.796uA | dx|dy 42.6024ns | 1.53024uA | s 35.9

Rise time ~10ns (@ 40pF drain capacitance!)

3D Interconnection

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Basic Problem:

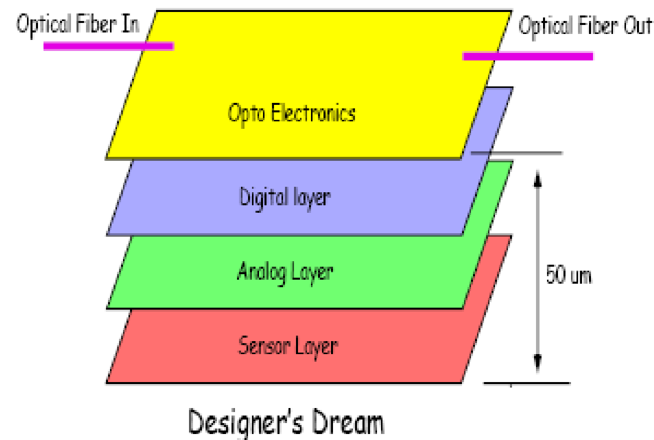
How to integrate good sensors and good electronic circuits?

3D Interconnection:

Two or more layers (="tiers") of thinned semiconductor de
"monolithic" circuit.

▪Different layers can be made in different technology
(high ohmic, BiCMOS, deep sub-μ CMOS, Si

▪3D is driven by industry:
- ▪Reduces R,L and C.
- ▪Improves speed.
- ▪Reduces interconnect power, x-talk.
- ▪Reduces chip size.
- ▪Each layer can be optimized individually.

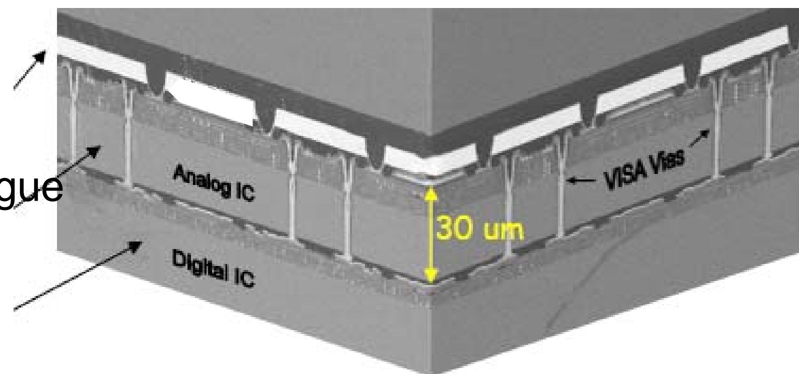


Designer's Dream

Si pixel sensor

BiCMOS analogue

CMOS digital



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Advantages of 3D for HEP detectors

Multilayer electronics:

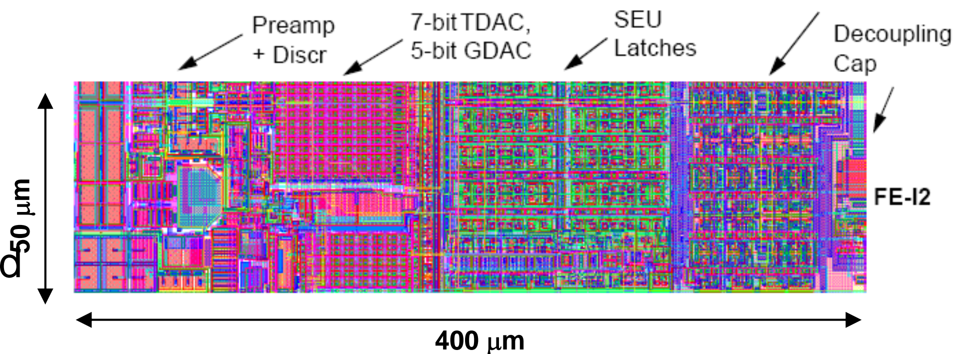
Split analogue and digital part
Use different, individually optimized technologies:

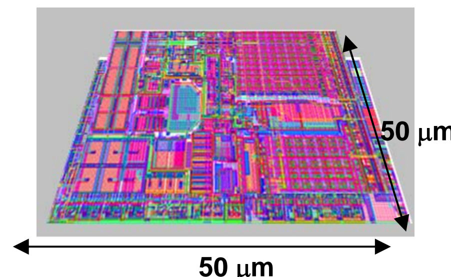
-> gain in performance, power, speed, rad-hardness, complexity.
-> smaller area (reduce pixel size or more functionality).

4-side abuttable devices:

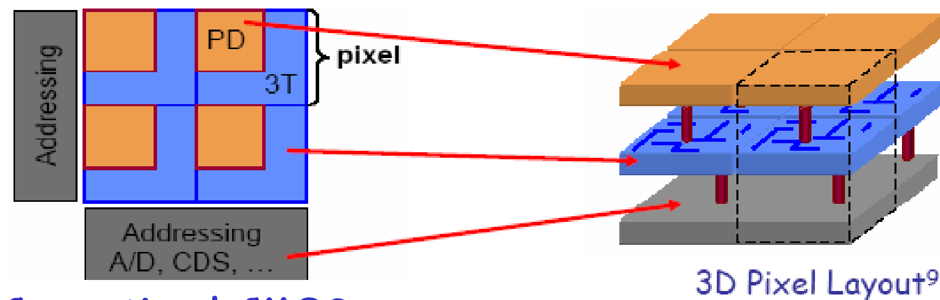
-> no dead space.
-> simpler module layout.
-> larger modules.

(reduce complexity and material)





50 x 400 μm^2 (0.25 μm)
May shrink to ~ 50 x 50 μm^2 (130 nm)



Conventional CMOS sensor (optical, similar: MAPS)

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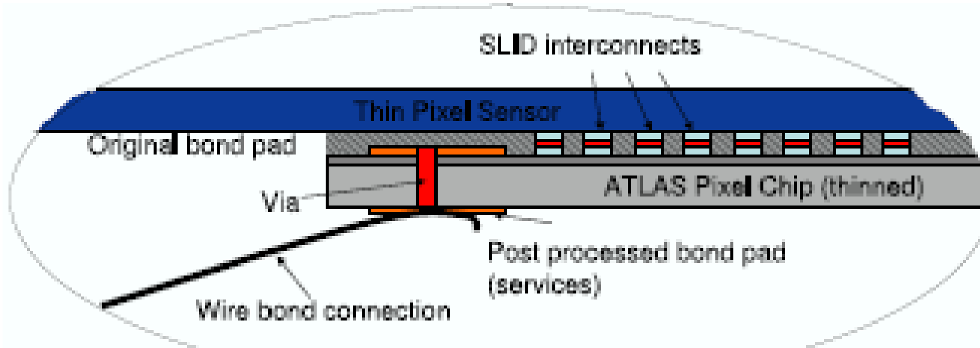
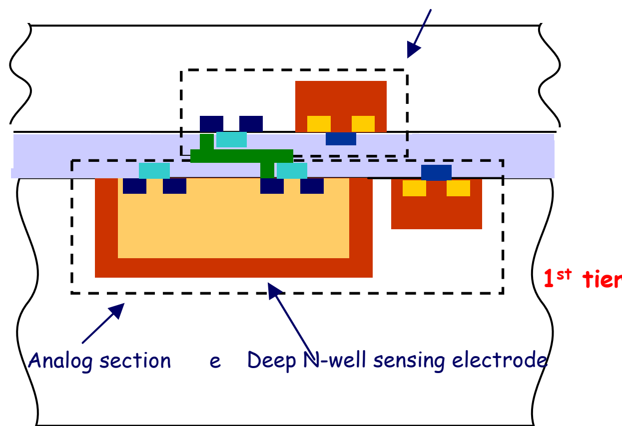
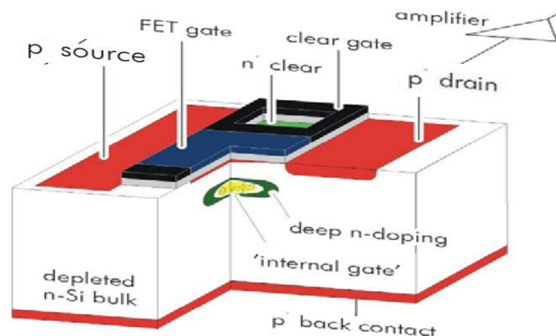
HEP applications



Evolution of hybrid pixels
⇒Thin devices
⇒Smaller pitch
(need good FE-ASIC!)



Improved CMOS sensors
Transfer most (if not all) of the PMOSFETs to 2nd tier (VIPIX)
High CCE
More functionality
Or
Use high resistivity CMOS as 1st tier (IPHC)



Use DEPFET as first tier
(intrinsic amplification, simpler FE-ASIC)
Problem: power: all pixels on 80W/cm²
=> scaling: L ~ 1 µm => 1 W/cm²

Fermilab 3D-IC

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First 3D-IC Tezzaron Multiproject Run

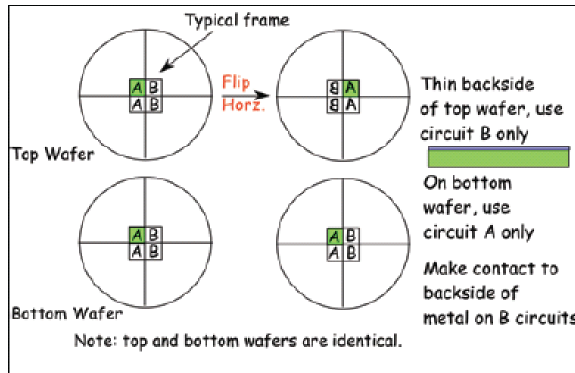
Broad range of architectures and applications:

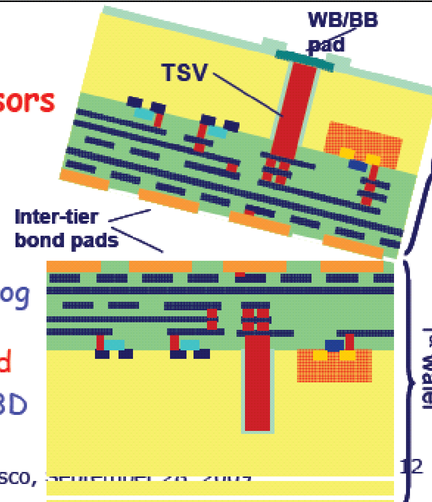
MAPS

- Convert 2D MAPS device to a full CMOS 3D design, with digital readout separated from the sensor and the analog front-end – Italy, France

Readout chips for high resistivity pixel sensors

- Convert MIT LL 3D SOI design to the Tezzaron/Chartered process – Fermilab
- Convert current 0.25 µm readout pixel electronics to a 3D structure with separate analog and digital tiers – France/US
- X-ray imaging/timing chip - Fermilab/BNL/Poland
- 3D chip with structures to test feasibility of a 3D integrated stacked trigger layer. - Fermilab





Valerio Re - IEEE 3D-IC Conference, San Francisco,

Consortium of about 15 institutions from US, France, Italy, Germany, Poland

Silicon Photomultiplier

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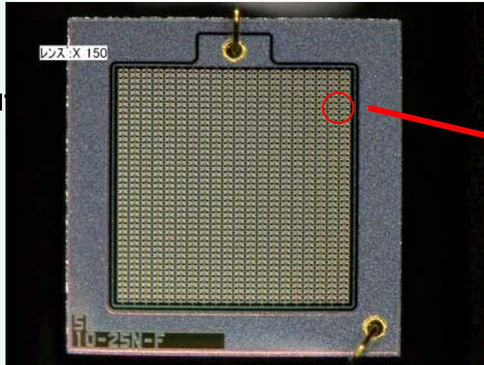
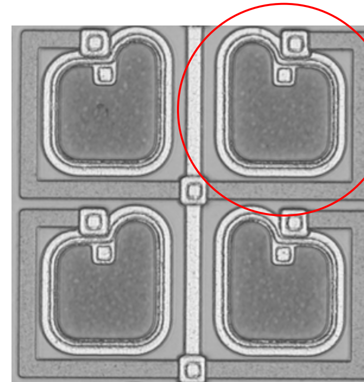
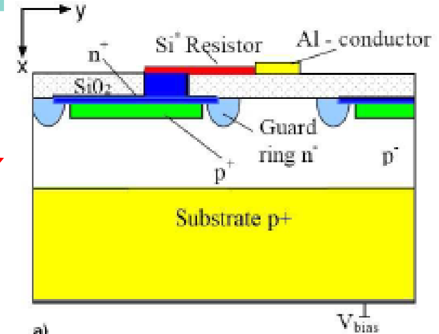
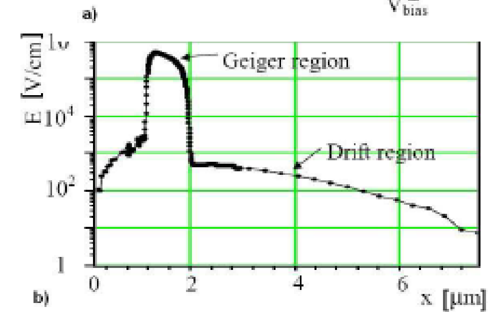
Basic building block: avalanche photodiode operating in Geiger mode





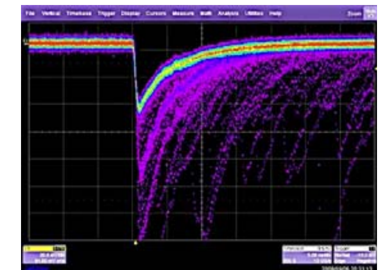




The device is operated above the breakdown voltage
Photons are absorbed in depleted silicon, create e/h pairs

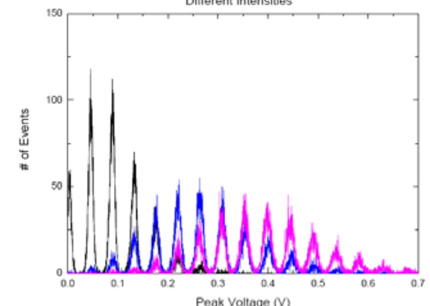
Avalanche amplification (Geiger breakdown) occurs
Passive quenching by integrated resistor (limits current)
The signal size (“amplification”) is given by the overvoltage and the cell capacity

$Q = C \times \Delta U$ (~ 10^6)   binary signal of fixed size!



Array of cells all connected to a single output:
Signal = Σ of cells simultaneously fired

If probability to hit a single cell << 1
=> **Signal proportional to # photons**



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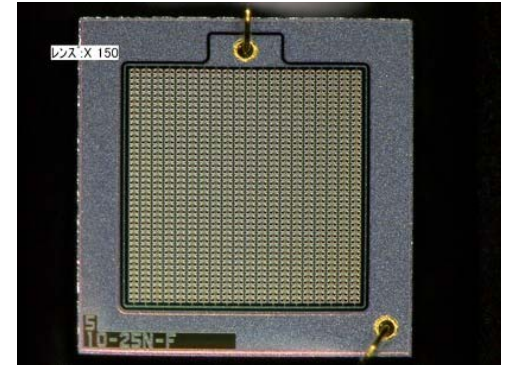
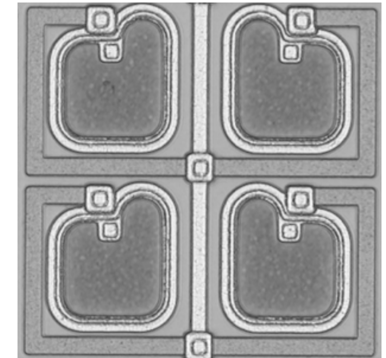
Very good photon detector

- Simple, robust device
- Photon counting capability
- Easy calibration (counting)
- Insensitive to magnetic fields
- **Fast response: < 1 ns (100ps demonstrated)**
- **Large signal (only simple amplifier needed)**
- Good quantum efficiency
- No damage by accidental light
- Cheap
- Low operation voltage (40 – 70 V)
- Many applications possible (replacement of PMTs)
- **But: no position resolution within matrix**





Hamamatsu S10362
1 x 1 mm²
1600 pixel
Pixel size: ~25 x 25 μm² l

8 μm avalanche cell already produce at MPI HLL

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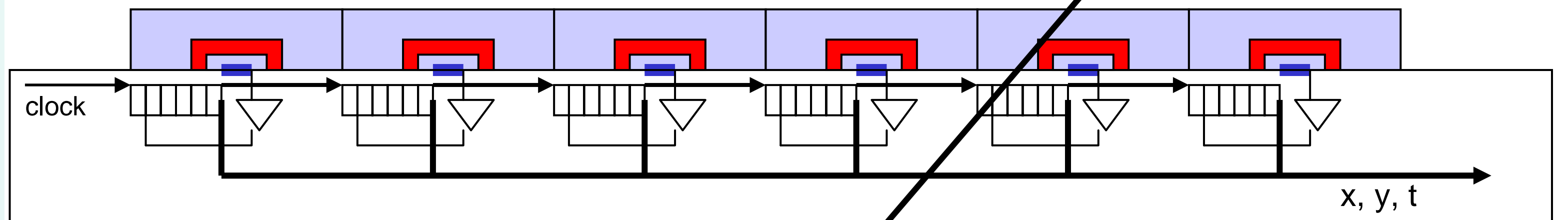
Smart SiPMs as tracker

Connect ASIC chip to SiPM

For each pixel: signal detection & active quenching (optional)

-Fast timing (no stray capacitances)
-Binary device (small pixels needed!)
-High efficiency (80 e+e-/µm for a MPI, one suffient to trigger)
-Large signal: $10^5 – 10^6$ e
-Ultra thin sensitive layer: 2-5 µm



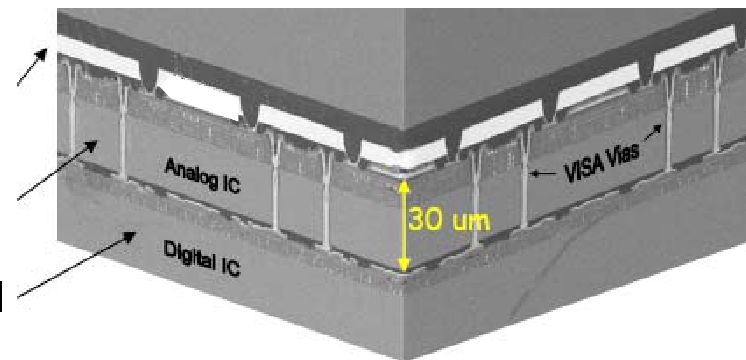
Could be made using

•Bump bonding
(not for 10µm pitch)
•3D integration

SiPM

HV CMOS

CMOS digital



Possible Problems

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Dark rate (noise occupancy)

~ 1 MHz/mm²

Single pixel occupancy (10 x 10 µm² pixel, 150ns integration)

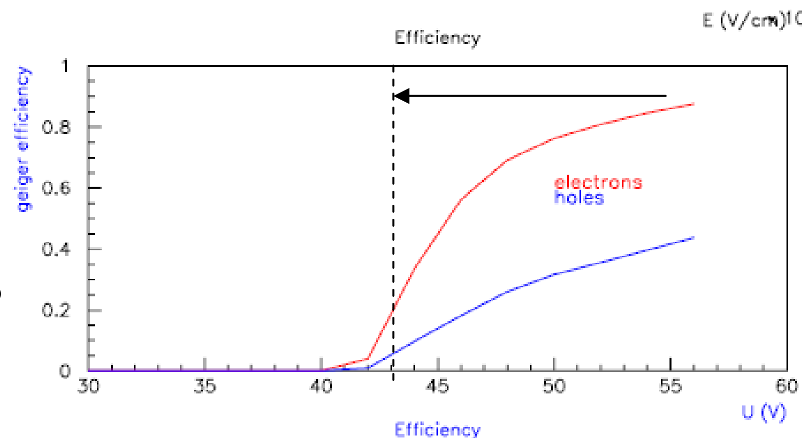
$\Rightarrow$1.5 x 10^{-5} (with 25ns time resolution): 2.5 x 10^{-6}

Cross talk

O(10%) in 1 mm² ??

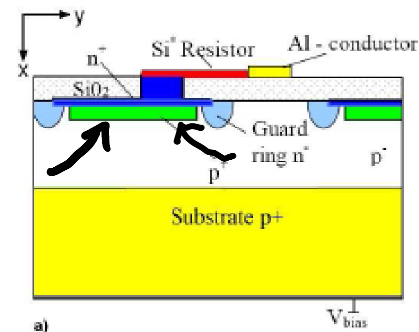
Reduce by operating at lower voltage
MIP: 80 pairs/µm
10% single electron efficiency: >98% for a MIP

=>Lower dark rate
=>Lower cross talk



Fill factor:

- 80% for large pixels (but including structures)
- drift region underneath HF may help
- double layer sensor?



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Conclusions

Fast Pixel Detectors:

Hybrid Pixels (LHC-like): too much material, large pixels
CMOS Sensors: too slow
DEPFET: too slow (frame readout)

Advanced CMOS: very interesting. Key: PMOS & high resistivity epi

3D integration: solves many problems:
evolution/combination of hybrid pixels, MAPS or DEPFETs
$\Rightarrow$Most promising way to go!

Avalanche arrays (SiPMs with single pixel readout)
ultrafast timing (< 1 ns) possible
needs 3D technology
potential drawback: fill factor (dead areas)

SiMPL: Undepleted bulk as resistor

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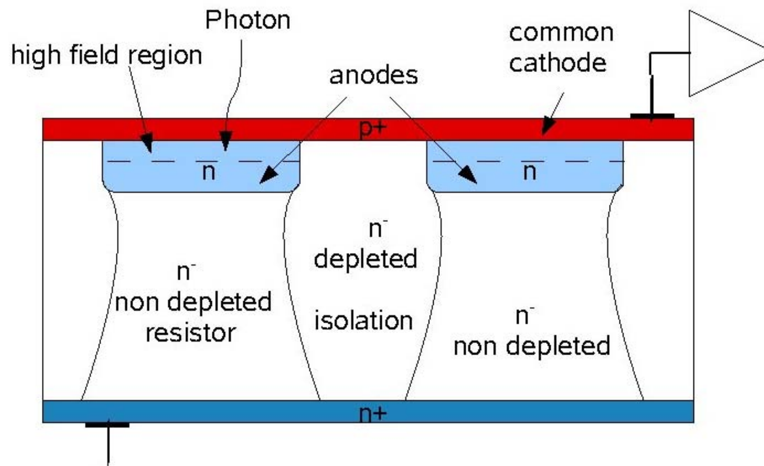
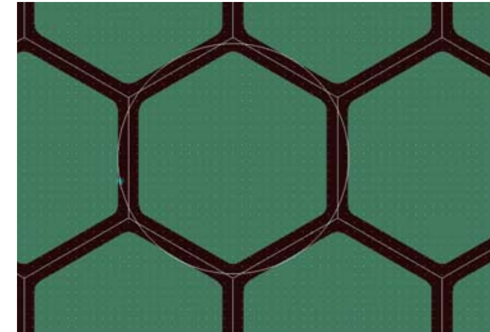
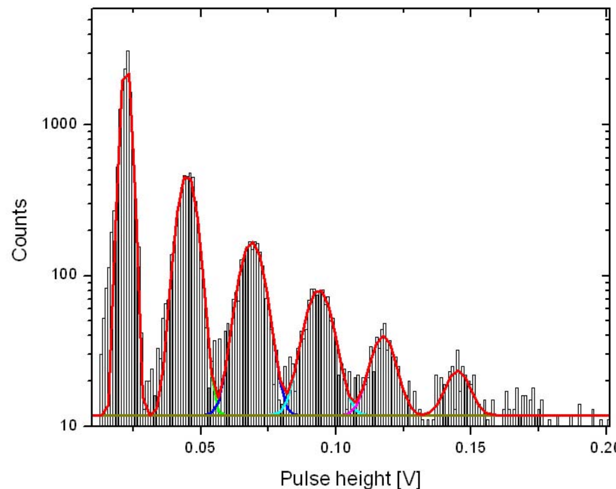




Shaping of electrical field (naturally du to implantation profile)
Bulk under HF region remains un-depleted, acts as resistor
Bulk in between HF region is depleted (isolates the pixels from each other)



No structures needed (poly, Al)
-> small pitch possible