Round Table
on Pixel Time Stamping

Panel

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Round Table on Pixel Time Stamping

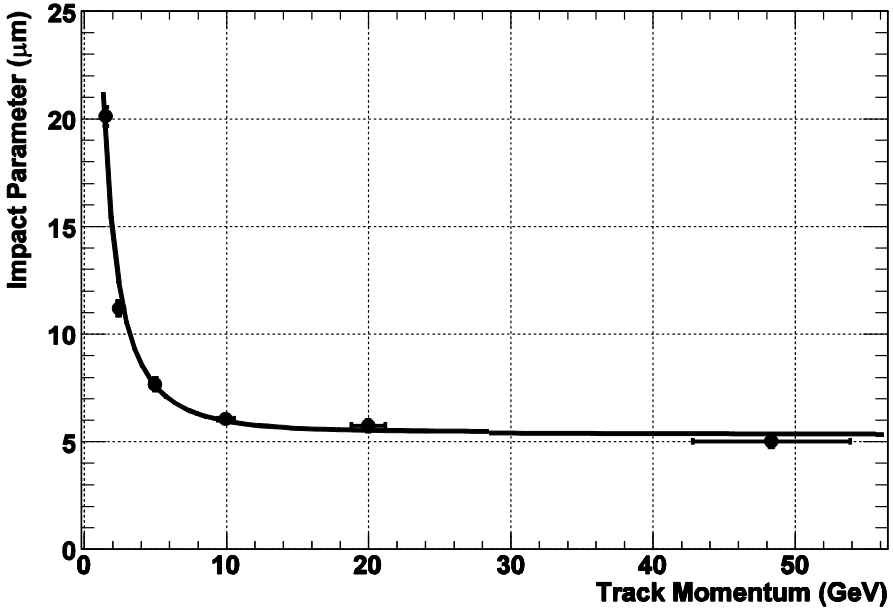
Physics and Detector Requirements

M Battaglia

Main Requirement & Constraints for Pixel Sensors at CLIC

- Pixel Size
  - track extrapolation resolution & spatial granularity
- Time stamping
  - time granularity
- Sensor Thickness
  - material budget
- Power Dissipation
  - material budget

Space Granularity
Track Extrapolation Resolution

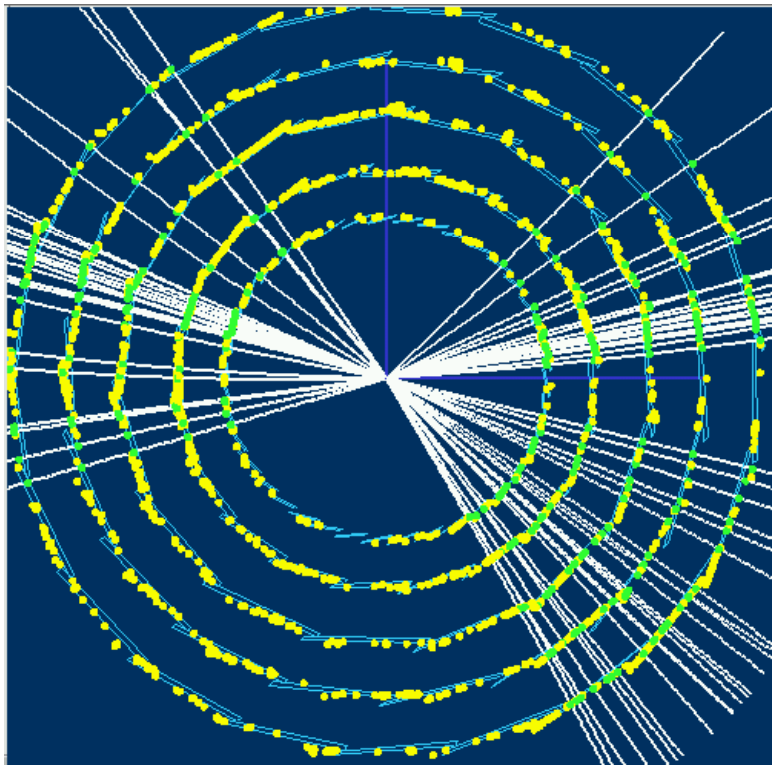


$$\sigma_{IP} \simeq 5\ \mu\mathrm{m} \oplus \frac{15\ \mu\mathrm{m}}{p_t(\mathrm{GeV})}$$

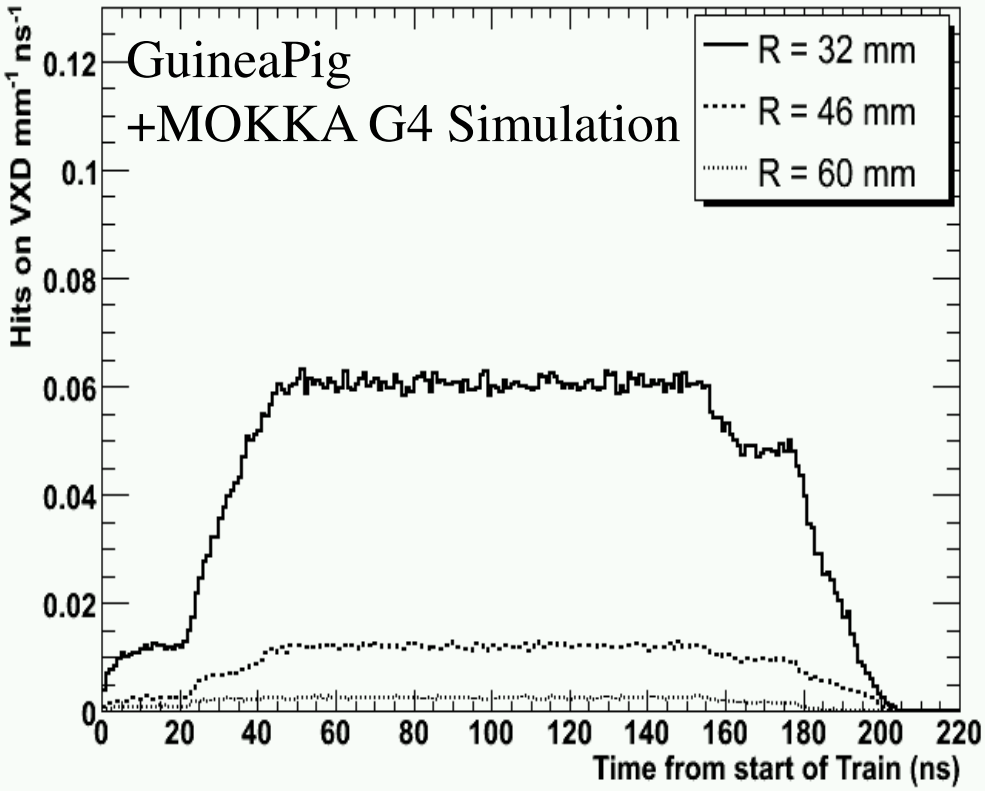
Given CLIC constraints this can be achieved with a multi-layered VTX with single point resolution ~ 3 μm, i.e. a ~ 10 μm binary pixel or a 15-20 μm analog pixel with charge interpolation

5-20 μm pixel pitch appears feasible for CCDs and monolithic active pixels in various technologies and architectures, is/will be possible to implement fast time-stamping capabilities in such small footprint ?

Space and Time Granularity
Occupancy from Pair Background

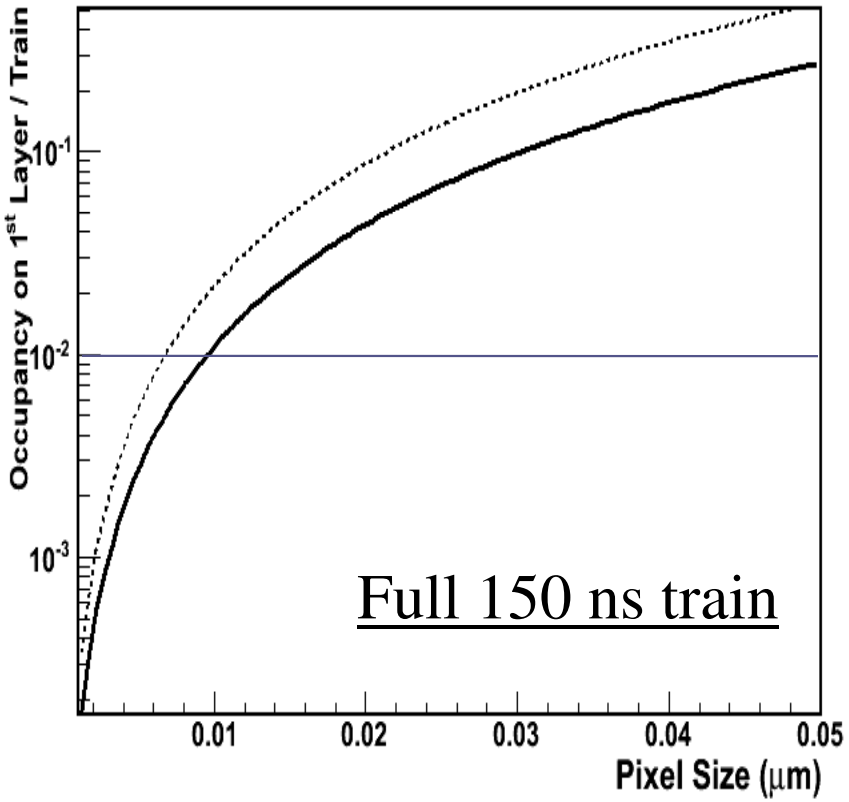


Hit Density on VTX vs time from start of train

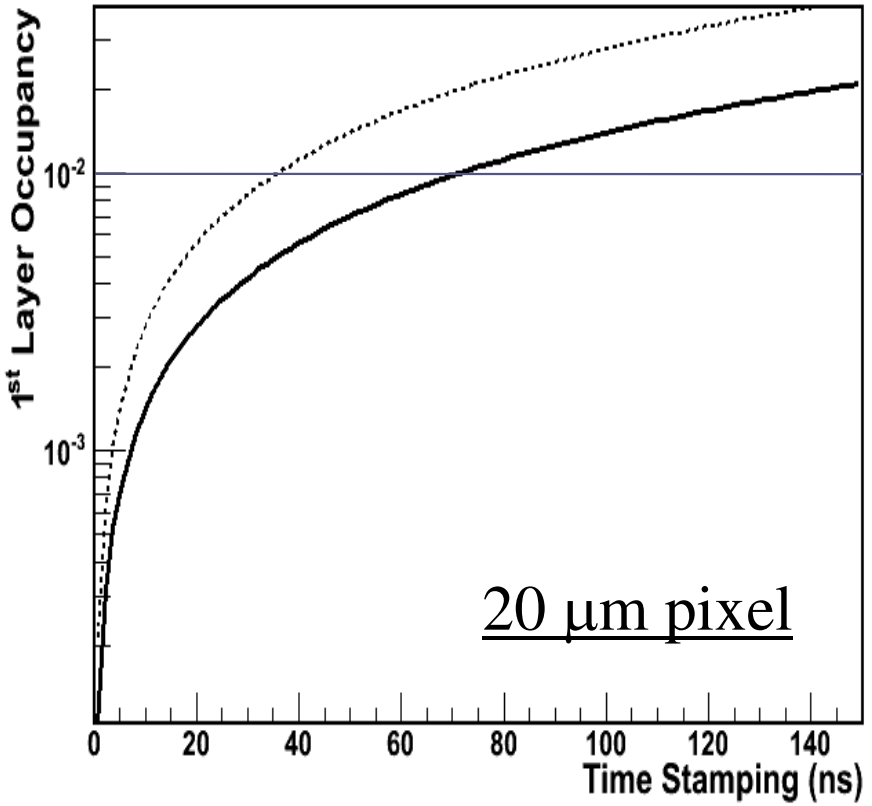


Space and Time Granularity
Occupancy from Pair Background

Train Occupancy vs. Pixel Size

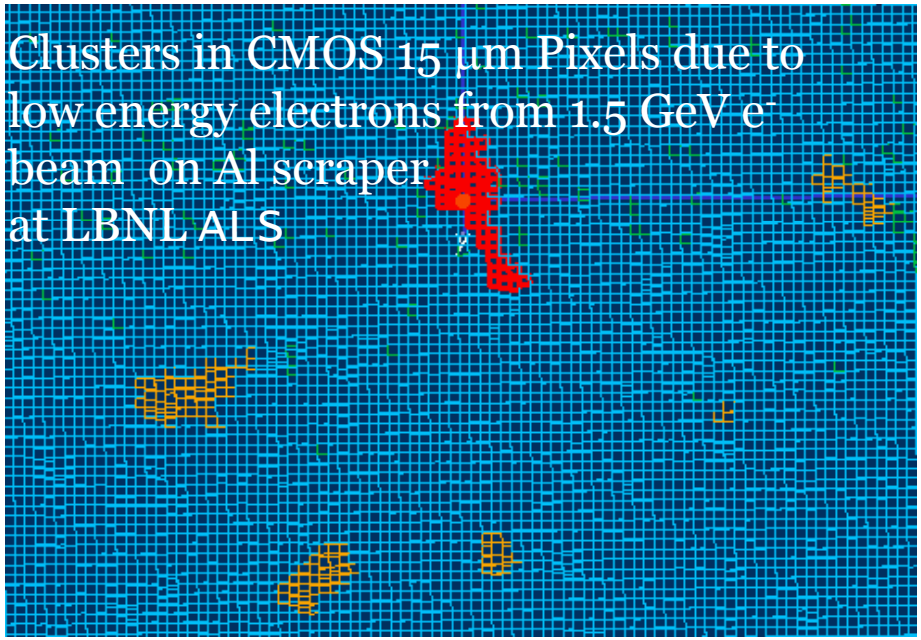


Occupancy vs. Time Stamping



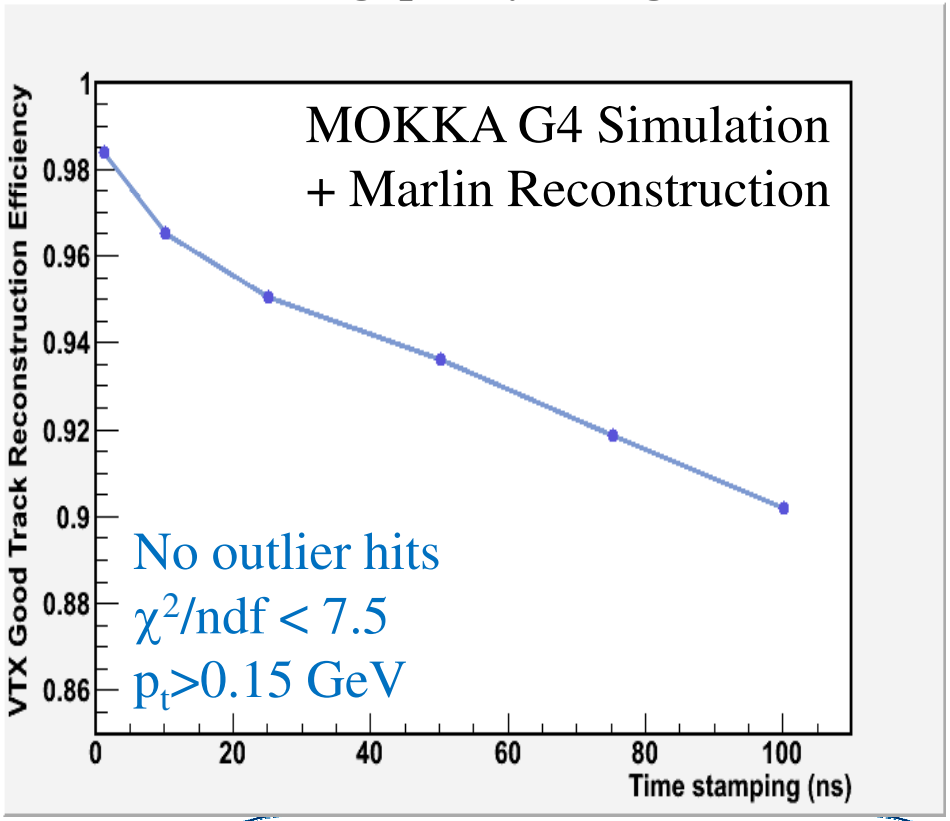
Space and Time Granularity
Occupancy from Pair Background

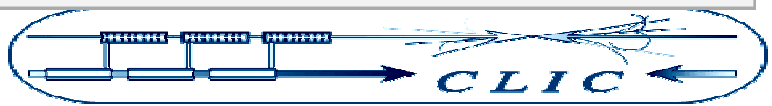
Expect 0.06 hits/mm²/BX, but depending on technology and layout each hit involves few to > 10 pixels



Overlay pair hits to 3 TeV e+e- events and study standalone VTX pattern recognition efficiency/purity vs time stamping.

20 μm pixel, depleted sensitive volume w/ average cluster size 2.5 pixels, single hit efficiency 99.5%. Plot efficiency for reco tracks fulfilling quality cuts given below:

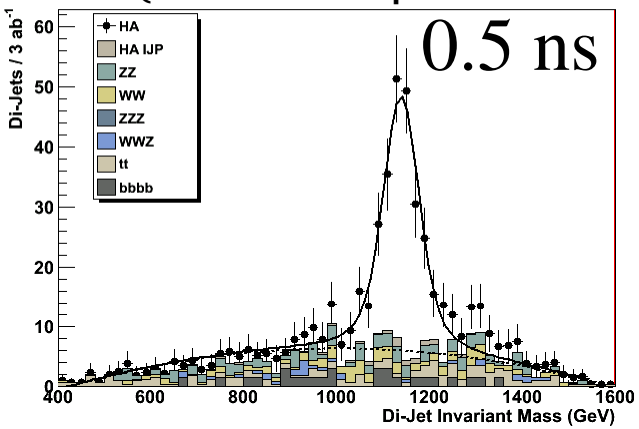


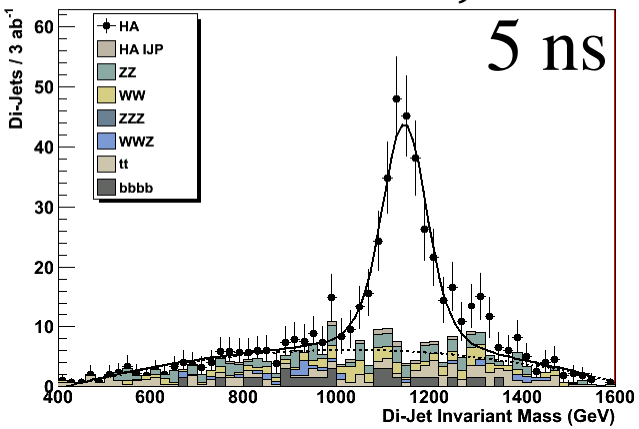


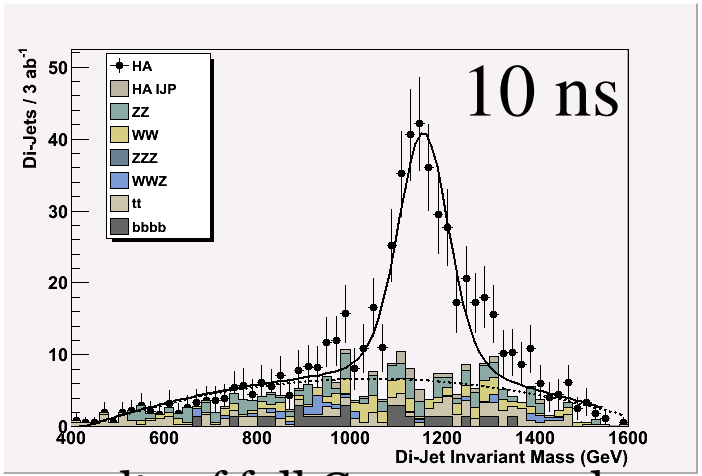
Time Granularity:

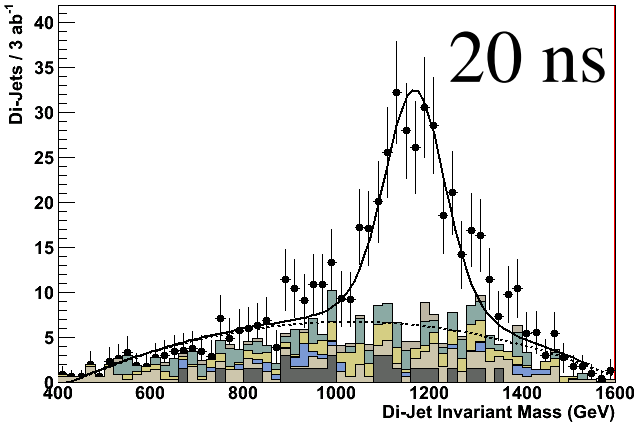
Energy in e^+e^- event from $\gamma\gamma \rightarrow$ hadrons background

Degradation of physics signal as function of background integrated in the detector (MOKKA G4 Simulation + Marlin Reconstruction)







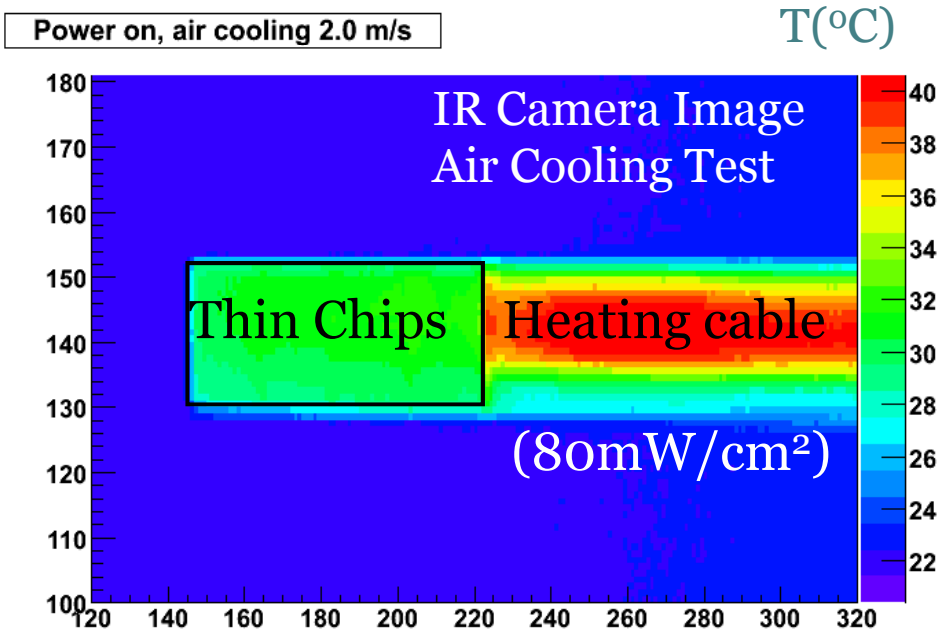


Preliminary results of full G4+reco analyses indicate physics performance impacted for $\Delta t > 10$-15 ns

Material Budget: Power Dissipation and Cooling

Material minimisation dictates passive cooling,

Preliminary tests with thin monolithic CMOS sensors on CFC ladder support structure in collaboration with STAR HFT indicate that 1-3 m/s airflow removes 70-100 mW/cm² without inducing large vibrations.



Assuming power dissipation to be concentrated at the end of column, 20 μm pixels and 1 cm column height, this corresponds to a limit of ~0.15 mW/column

This power budget appears to be realistic for a variety of monolithic pixel sensor technology, but is/will this be feasible when including time-stamping capabilities ?
Is power pulsing at 50 Hz an option ?