Upgrade of the CMS Barrel Electromagnetic Calorimeter for the LHC Phase-2 UNIVERSITE PARIS-SACLAY

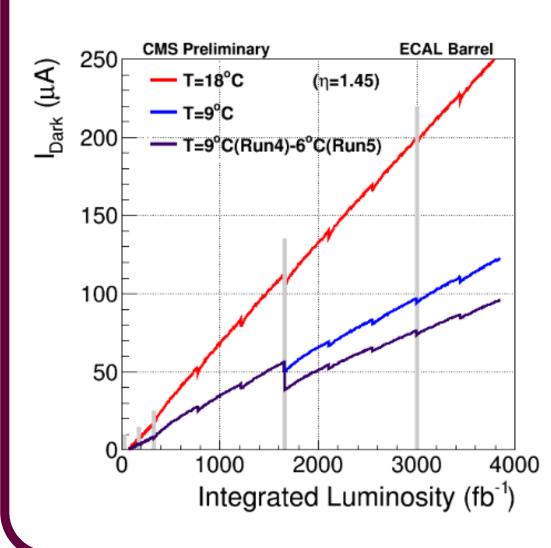
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Introduction

The CMS electromagnetic calorimeter (ECAL) consists of 75848 lead tungstate (PbWO4) crystals, arranged in a barrel (EB) and two endcaps (**EEs**), and a silicon-sensor **preshower**. It serves a crucial role in the successful CMS physics program with precise time and energy measurements of electromagnetic particles from high-energy collisions of the LHC at CERN.



Cez

In 2029, the LHC will start its High-Luminosity Phase-2 era, providing an instantaneous luminosity of 5×10^{34} cm⁻²s⁻¹ with an average of 140-200 simultaneous collisions to reach an integrated luminosity of 3000 fb $^{-1}$.

The CMS ECAL will need to be upgraded to operate in such

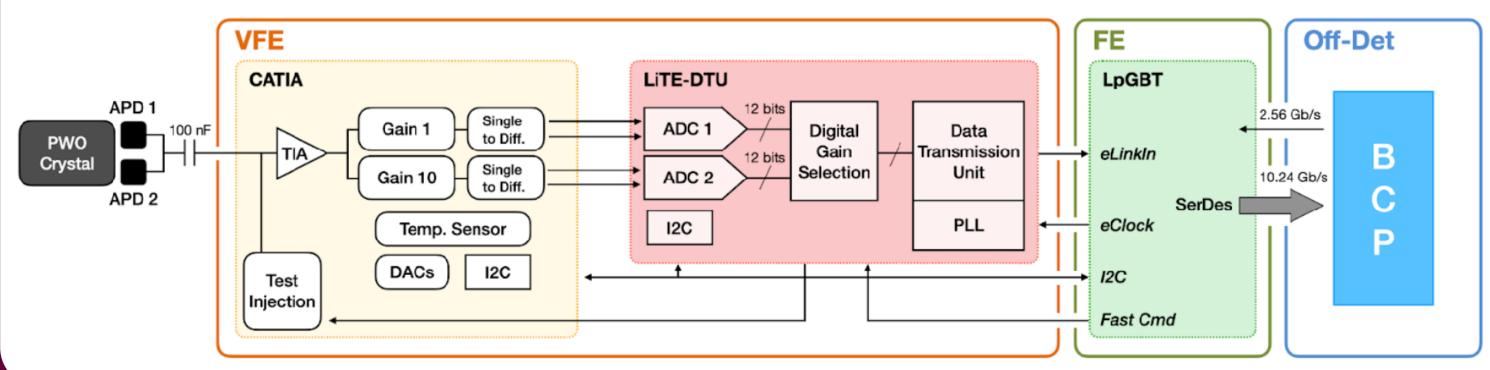
Front-end ASICs

CATIA

- Calorimeter Trans-Impedance Amplifier
- radiation tolerant 130 nm CMOS technology
- dual gain outputs ×1 and ×10
- range from tens of MeV to 2 TeV
- signal shaping time $\mathcal{O}(20)$ ps

LITE-DTU

- Lisbon-Torino ECAL Data Transmission Unit
- radiation tolerant 65 nm CMOS technology
- two commercial 12 bits 160 MS/s ADCs
- Iossless data compression
- 1.28 Gb/s serial link

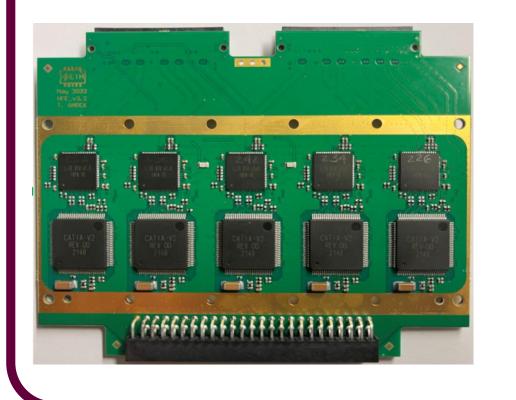


conditions. The endcaps will by replaced by the High Granularity detector.

In the **EB**, the crystals and their APDs will be retained, but operated at 9℃ to reduce the APDs noise. The electronics will be fully upgraded to cope with the 7.5 fold increased CMS ⁴⁰⁰⁰ trigger rate with the goal of achieving a timing resolution of 30 ps for particles with energy E > 50 GeV.

VFE

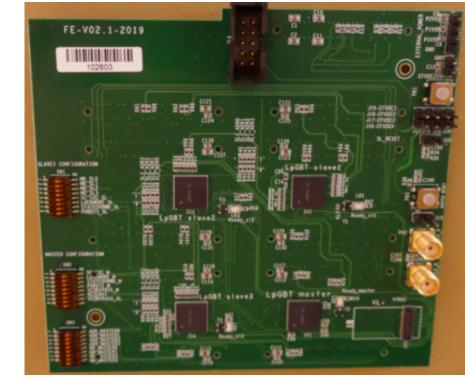
The Very Front-End board (12240 units) is connected to the crystals APDs through a motherboard retained from the current ECAL. Each VFE houses five CATIA and LiTE-DTU chips to **read**, **amplify**, digitize and transmit the **signals** from five crystals.



FE The Front-End board (2448

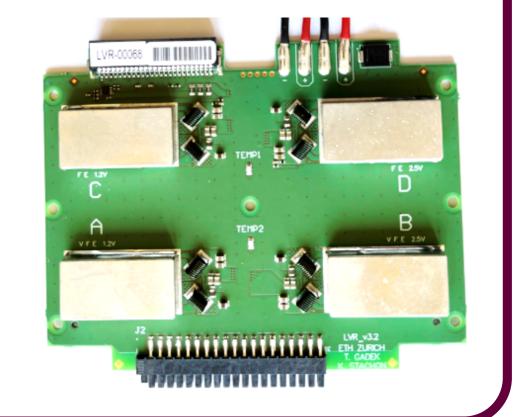
Front-end boards

units) collects the signals of five VFEs and sends the data to the back-end system via 10 Gb/s optical links. The clock and control signals are managed by four **CERN Low-power Gigabit** Tranceiver (LpGBT) chips.



LVR

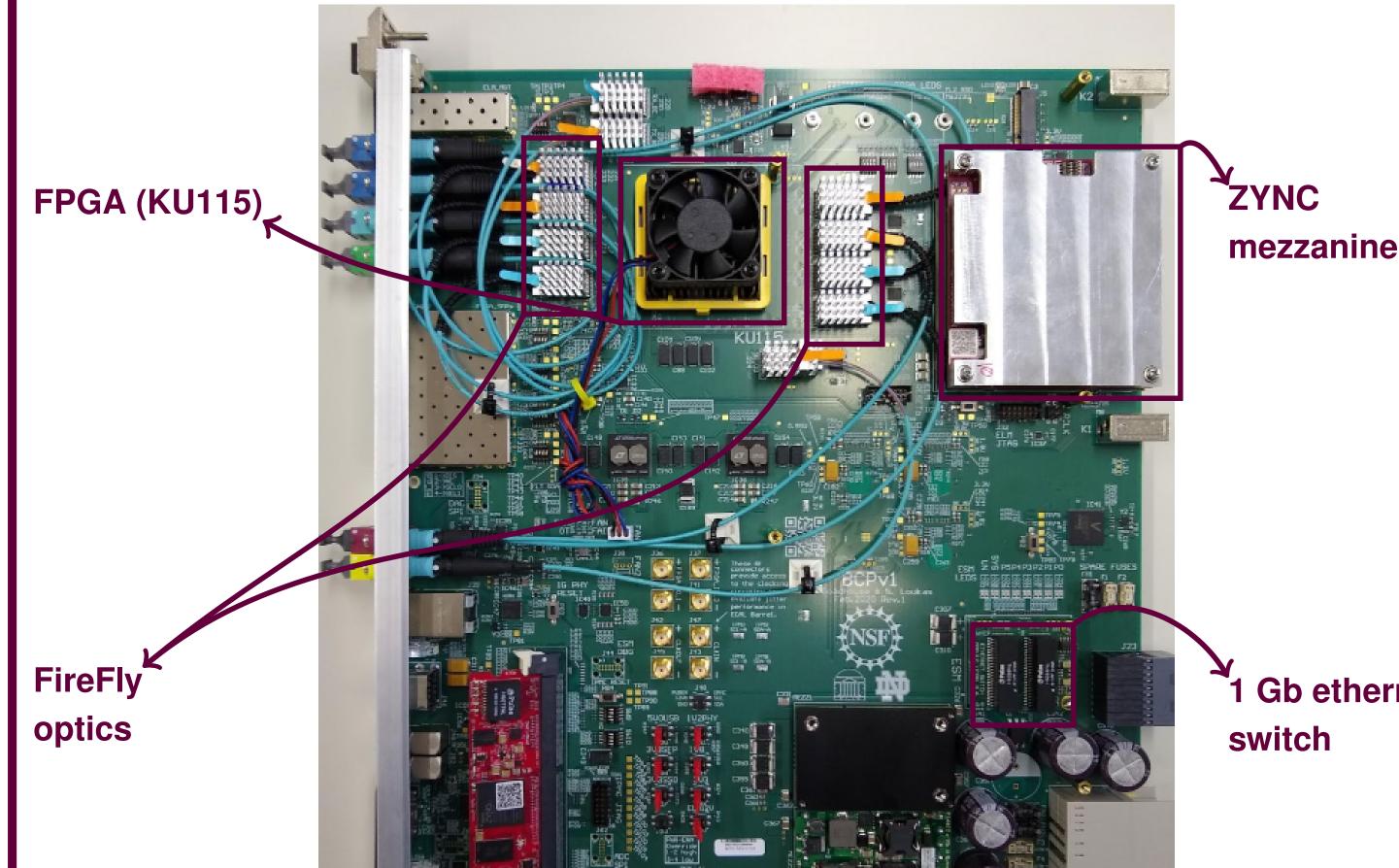
The Low Voltage Regulator (2448 units) distributes the power to the VFEs and FE. It houses radiation hard DC-DC converters to supply the required voltage to the ASICs. The power consumption is halved w.r.t to the current ECAL.



Back-end board

The back-end electronics consists of the new the **Barrel Calorimeter Processor (BCP)** board. It is located in the CMS service cavern, thus not requiring a radiation tolerant design. Each card handles 600 channels, with a total of 108 units required to cover the whole ECAL. It is a custom designed Advanced Telecommunications Computing Architecture (ATCA) board embedded with a large Xilinx Virtex Ultrascale Plus VU13P FPGA. The prototype board BCP v1 with the Xilinx Kintex Ultrascale KU115 FPGA is used to develop

the firmware and test the interface with the FE and the DAQ.



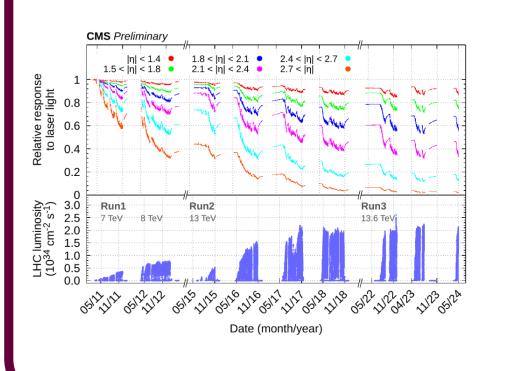
Laser monitoring system

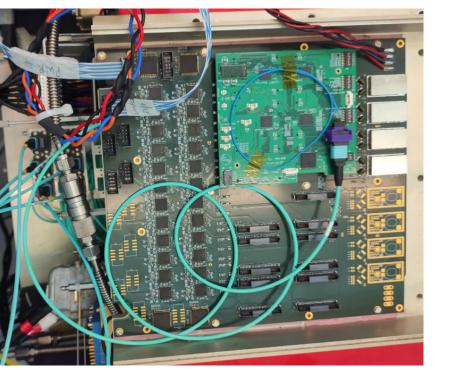
The Laser monitoring system constantly monitors crystals transparency changes using PN diodes as reference.

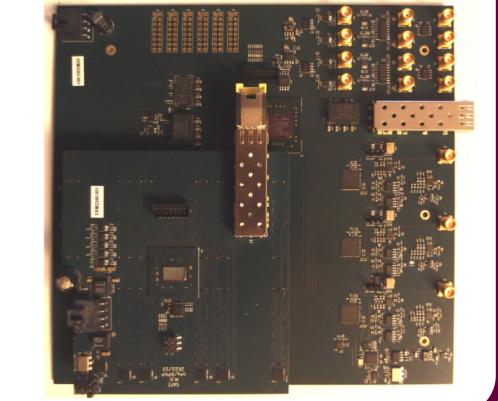
For **Phase-2**, the number of **PN diodes is doubled** (864 units). They are hosted in the HL-**Front** End Module (FEMs) (422 units) with the new charge pre-amplifier MONACAL ASIC.

The HL - Monitoring Electronics read-out Module (36 units) receives the analog signals from the FEMs, digitizes them with the LiTE-DTU at 80 MS/s and sends data to the back-end electronics through standard FE boards.

The interface with the trigger and DAQ is managed by the single new Laser Monitoring Board employing a commercial FPGA.







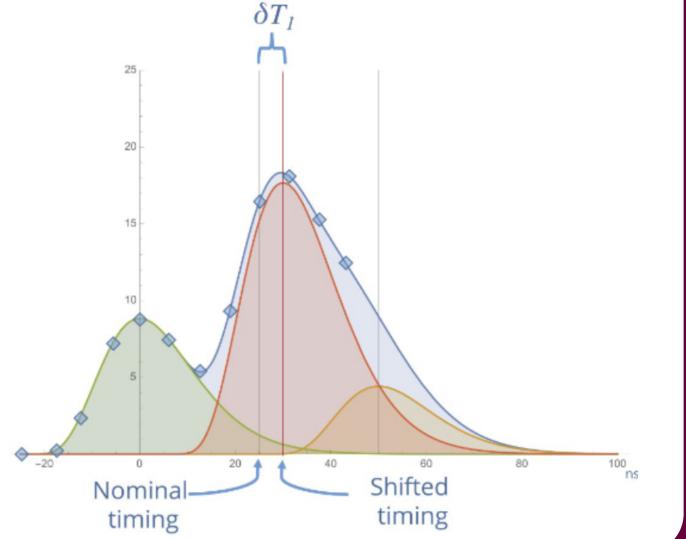
1 Gb ethernet

It **provides the clock and control signals** for the front-end electronics, receives the signal of each crystal via optical fibres and generates two sets of trigger primitive (TP) for the L1 trigger, one for single crystals and one for clusters.

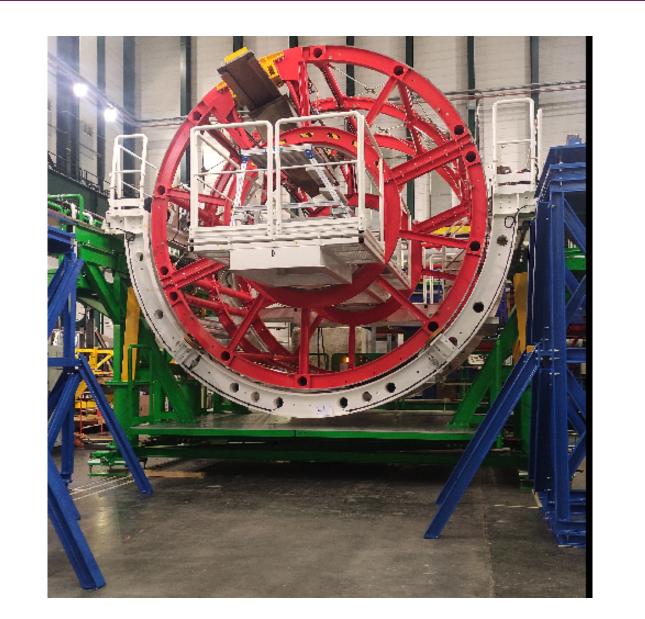
Each TP contains the **position**, the **transverse** energy and the time measured with a linearized multifit-timing algorithm. A spike flag bit is added using the differences in the pulse-shape and energy topology discrimination. The connection to the DAQ and the FE electronics is made with SAMTEC FireFly optics transmitting up to **25 Gb/s**.

The board is controlled via a Xilinx ZYNC FPGA mezzanine running Linux.

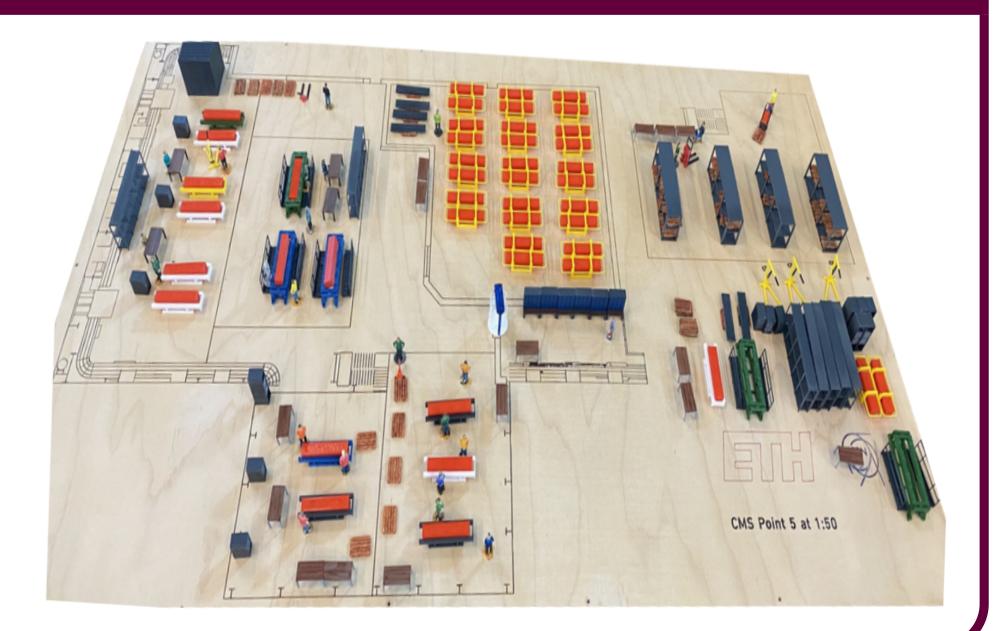
The CMS hadronic calorimeter will use the same back-end board.



Current status and future plans



- pre-production batch of the final version of the front-end ASICs under evaluation
- design of the front-end boards near completion
- excellent preliminary results from beam tests with near-to-final version of all the components of the upgraded readout
- firmware and layout of the BCP final version v2 board almost finalized
- the **Enfourneur2**, the upgraded version of the extraction and insertion tool of the ECAL 36 supermodules (SMs) weighting 3 t each, is **under commissioning**
- first prototypes of upgraded laser monitoring components fully operational, defining placement and cabling
- the extraction of the SMs is foreseen to start in the second half of 2026, the **electron**ics refurbishment and the re-insertion are planned to be completed by mid 2027, with ECAL commissioning in 2028
- definition of service requirements for the upgrade integration area (mockup)



Main references

- [1] CMS Collaboration, "The CMS electromagnetic calorimeter project". Technical Design Report CMS. CERN, Geneva, 1997.
- CMS Collaboration, "The Phase-2 Upgrade of the CMS Barrel Calorimeters". Technical Design Report CMS. CERN, Geneva, 2017.
- T. Reis on behalf of the CMS Collaboration, "CMS ECAL upgrade for precision timing and energy measurements at the High Luminosity LHC", J. Phys. Conf. Ser. 2374 (2022) 012072, doi = 10.1088/1742-6596/2374/1/012072

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