Technical challenges and performance of the new ATLAS LAr Calorimeter Trigger

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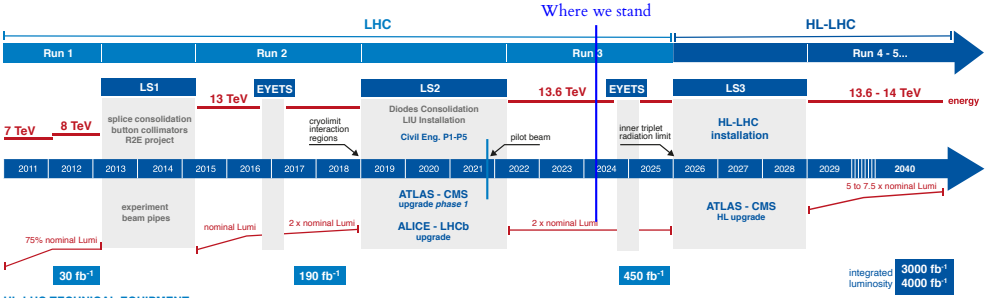
the ATLAS Liquid Argon Calorimeter Group

University of Toronto

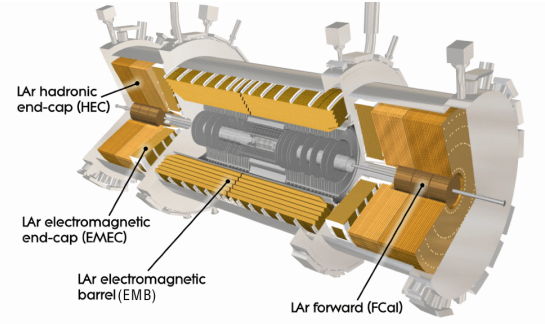
21 May 2024

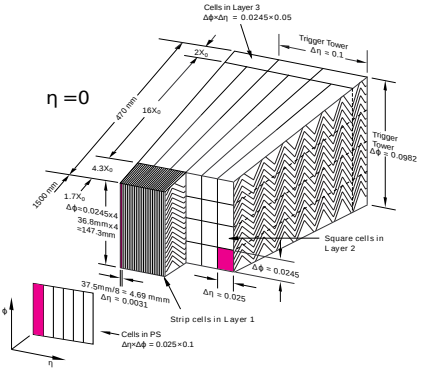
LHC Run 3



- Run 3 started in early 2022, pileup almost doubled with respect the Run 2 conditions
- New **LAr Digital Trigger** electronics installed during LS2 as part of the ATLAS Phase-I upgrades to **cope with the higher pileup and keep same L1 rate** as Run 2
- The rest of the LAr readout electronics will be upgraded during LS3 (HL upgrades)
  - LAr digital trigger will remain for HL-LHC as well
  - See next talk by Lauren for the details!

- Sampling calorimeter with Liquid Argon ($\sim$ 88 K) as active medium, while Lead (EM), Copper (Had) or Tungsten (FCAL) for passive medium
- **Longitudinally segmented** with different granularities
- Accordion geometry EM Barrel and EndCap, Pad design for HEC and ROD design for FCAL
- Coverage $|\eta| < 4.9$





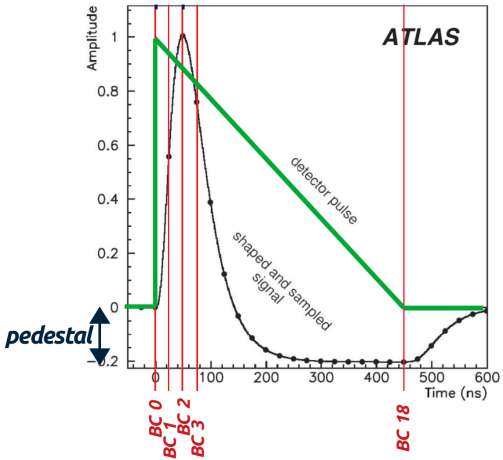
Main readout

- 180k cells are the smallest readout units
  - Cells η-ϕ dimensions and depth depends by layer and position
  - Electric field across cells with the application of High Voltage (from 250 V to 2500 V)
- Particle showers produce a triangular ionization signal
- Signal is **amplified, shaped, and buffered waiting for L1Accept** in the front-end
- Energy and timing are computed by the back-end electronics with Optimal Filter Coefficients

Trigger

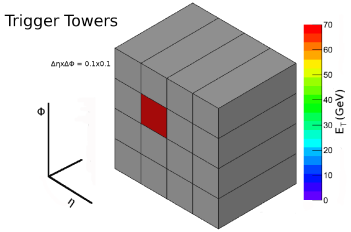
- Signals from **close-by cells are summed to form Trigger Towers (TT) or Super Cells (SC)**
  - Feed L1 Calorimeter Trigger (L1Calo)

Main readout pulse

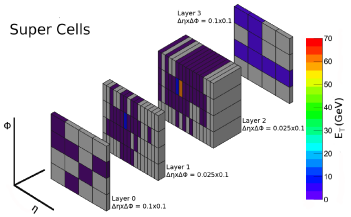


LAr Digital Trigger

Run 2 ↔ Trigger Tower (TT)



Run 3 ↔ Super Cell (SC)



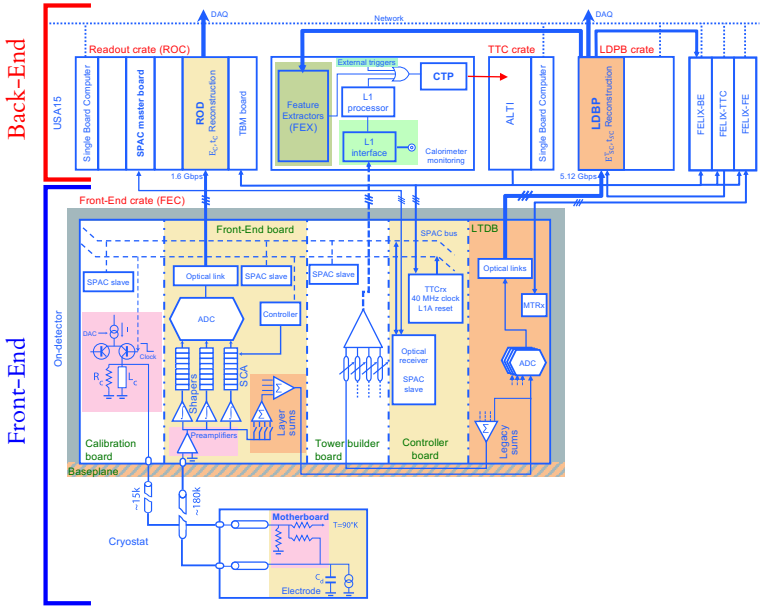
Simulation for a **70** GeV electron

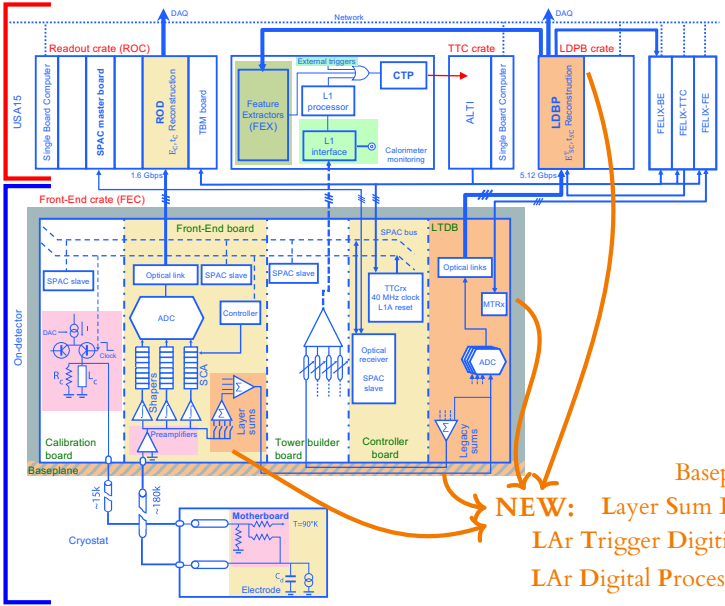
- No longitudinal segmentation
- Fixed size in $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$
- Only 5.4k TT from 180k cells

- Longitudinally segmented as calorimeter
- Increased granularity in Front and Middle to $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$
- 34k SCs from 180k cells

Use more information at trigger level to better reject background

- ∼10x more cells and increased precision and range of the energies transmitted to L1Calo
- Using shower shape information (similar to offline identification) for better pileup rejection


Back-End
Front-End
DAQ
Network
DAQ
Readout crate (ROD)
TTC crate
LDPB crate
USA15
Single Board Computer
SPAC master board
ROD
E_T,η,φ Reconstruction
TBM board
Feature Extractors (FEX)
External triggers
CTP
L1 processor
L1 interface
Calorimeter monitoring
ALTI
Single Board Computer
LDBP
E_T,η,φ Reconstruction
FELIX-BE
FELIX-TTC
FELIX-FE
1.6 Gbps
5.12 Gbps
Front-End crate (FEC)
On-detector
Front-End board
SPAC bus
LTDB
SPAC slave
Optical link
SPAC slave
SPAC slave
Optical links
TTCrx
40 MHz clock
L1A reset
MTRx
ADC
Controller
DAC
Clock
R
C
Shapers
SCA
Preamplifiers
Layer sums
Optical receiver
SPAC slave
ADC
Legacy sums
Calibration board
Tower builder board
Controller board
Baseplane
~15k
~180k
Cryostat
Motherboard
T=90°K
C_d
Electrode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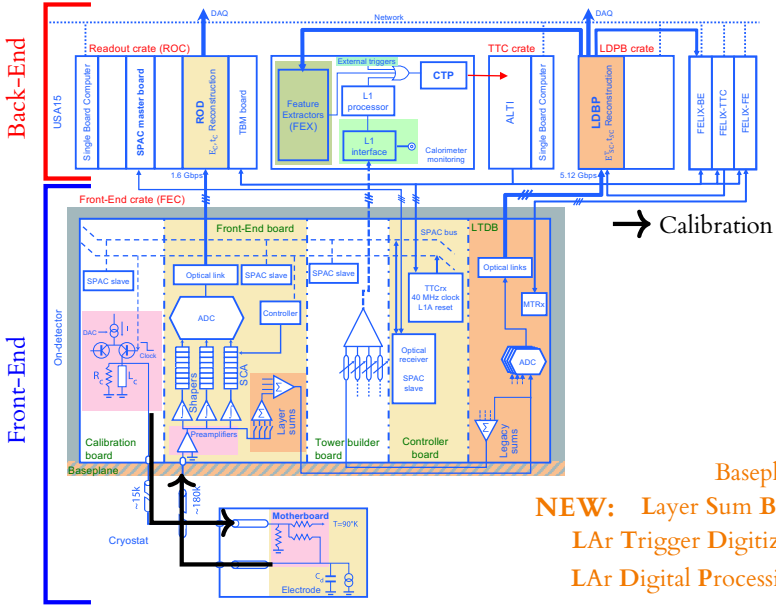
Optical links
TTCrx
40 MHz clock
L1A reset
MTRx
Controller
ADC
DAC
Clock
Shapers
SCA
Preamplifiers
Layer sums
Optical receiver
SPAC slave
ADC
Legacy sums
Calibration board
Tower builder board
Controller board
Baseplane
~15k
~180k
Cryostat
Motherboard
T=90°K
Electrode
C_d
Baseplane
NEW: Layer Sum Board (LSB)
LAr Trigger Digitizer Board (LTDB)
LAr Digital Processing Blade (LDPB)



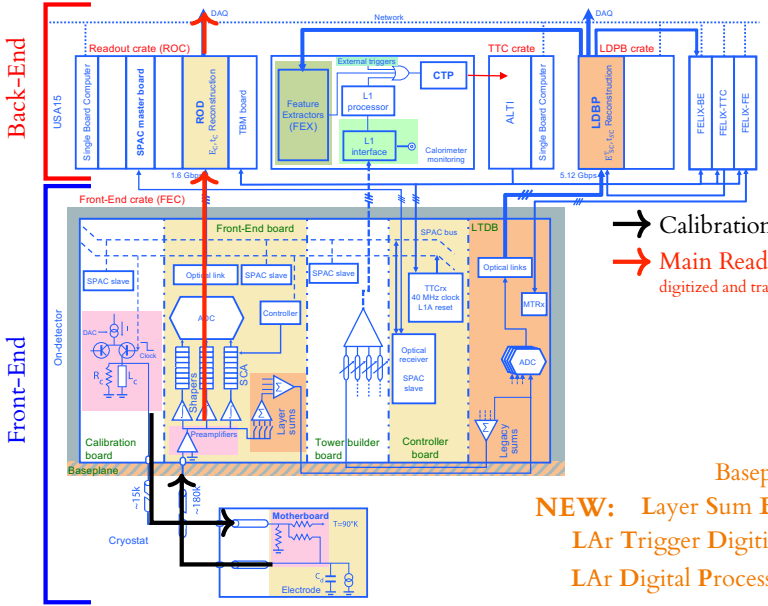
Baseplane

NEW: **L**ayer Sum **B**oard (LSB)

LAr **T**rigger **D**igitizer **B**oard (LTDB)

LAr **D**igital **P**rocessing **B**lade (LDPB)

Digital Trigger electronics overview



→ Calibration

→ Main Readout (Samples buffered then digitized and transmitted at L1A rate **100** kHz)

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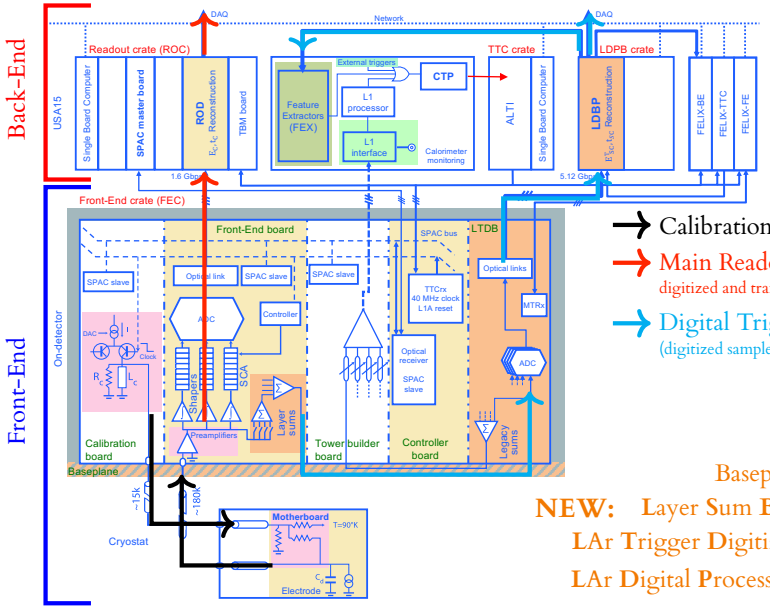

→ Calibration

→ Main Readout (Samples buffered then digitized and transmitted at L1A rate **100** kHz)

→ Digital Trigger (SC) (digitized samples streamed at **40** MHz)

Baseplane

NEW: **L**ayer Sum **B**oard (LSB)

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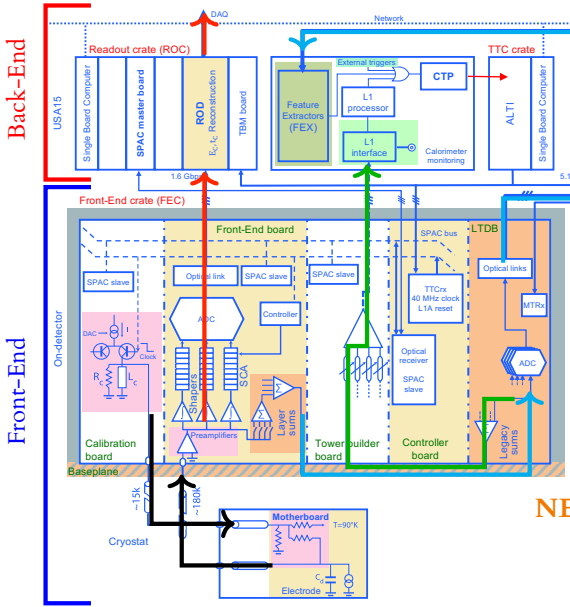
Digital Trigger electronics overview



→ Calibration

→ Main Readout (Samples buffered then digitized and transmitted at L1A rate **100** kHz)

→ Digital Trigger (SC)
(digitized samples streamed at **40** MHz)

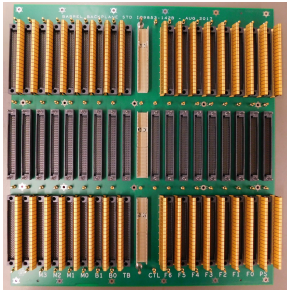
→ Legacy Trigger (TT)
(analog sums digitized in the back-end)

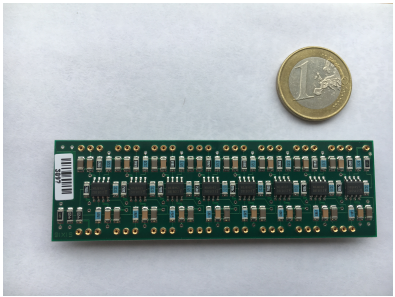
Baseplane

NEW: **L**ayer Sum **B**oard (LSB)
LAr Trigger **D**igitizer **B**oard (LTDB)
LAr **D**igital **P**rocessing **B**lade (LDPB)

Baseplane

- Connect various boards in the **F**ront **E**nd **C**rate
- Replaced to operate and commission digital trigger
  - **Allow concurrency for digital and analog trigger**
  - Additional slots for LAr Trigger Digitizer Board
  - Additional routing for both systems
- Installed 114 baseplanes

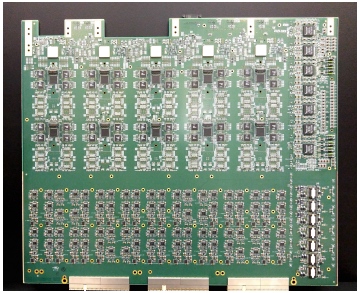




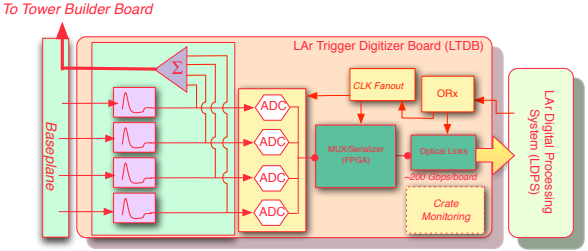
Layer Sum Board (LSB)

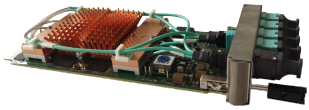
- Plug-in card for Front End Board, 6 different types installed
- Provide **signals for LTDB by analog sums of calo cells**
- Replaced 2968 LSBs to provide finer sum segmentation for SCs in the front and middle layers

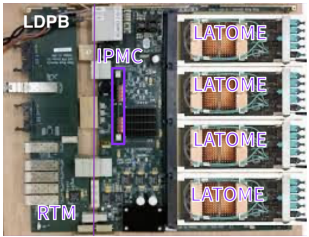
LAr Trigger Digitizer Board (LTDB)



- Custom-designed 12 bit ADC at 40 MHz, in 130 nm TSMC
  - Least significant bit of the ADC is $\sim$ 150 (300) MeV in Front (Middle) layer
- **Perfoms shaping, sampling, and digitization of the summed signal of up to 320 SCs**
  - Also recreates the legacy layer sums for the TT builder board
- Transmits to LDPB via optical fiber links
  - 8 SCs per fiber at 5.12 Gb/s
  - Custom serializer (LOCx2) and laser drive (LOCld), using 250 nm SOI process
- 124 LTDBs in total, 7 different flavours
- Required to be **operational for HL-LHC** too
  - After exchange of power mezzanines

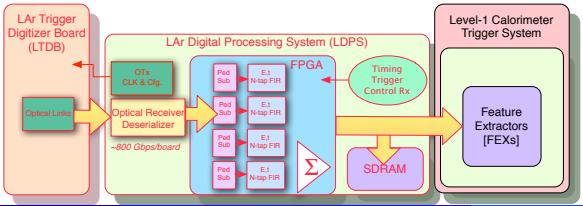




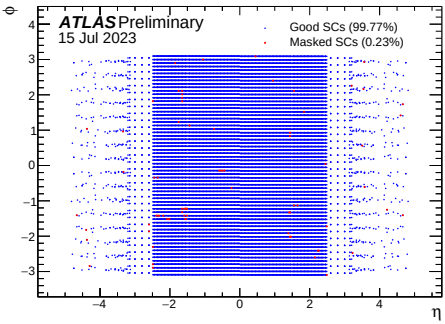


LAr Digital Processing Blade

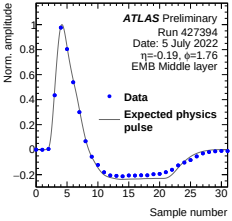
- System **receives pulse samples** from LTDB (∼25 Tbps, 40 MHz) and **transmits energies** to L1 Calo Trigger (∼41 Tbps, 40 MHz)
- Main goals: **reconstruct E_T and identify bunch cross**
  - Strict latency limit for E_T and pulse phase algorithms (5 to 6 bunch crossing)
- System composed of 30 Blades, each hosting 4 **LA**r **T**rigger pr**O**cessing **ME**zzanines (LATOMEs) over one **LA**r **C**arrier (LArC)
  - LATOME and LArC use commercial FPGAs
    - Intel Arria-10 and Xilinx Virtex 7 respectively
- System distributed in 3 ATCA crates

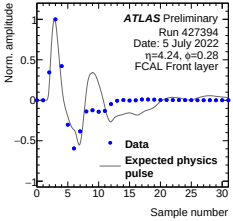


LAr DT Performance



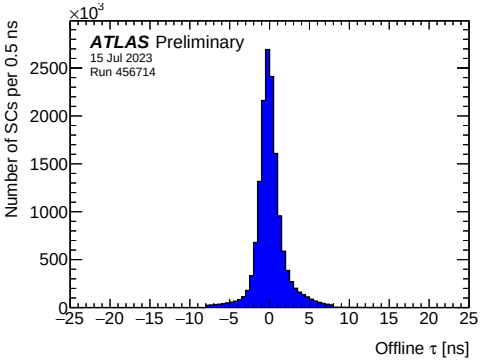
- $>$ 99.7% **coverage** during high luminosity *pp* runs in 2023

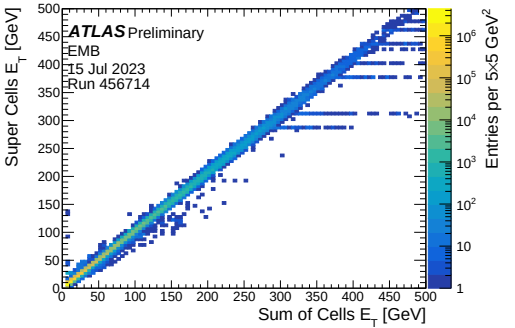




- Pulse shape is consistent with expected pulse from calibration
- In FCAL, working on improving the SC pulse shape modelling
  - Known FCAL pulse from calibration different from physics
  - Obtain the shape from collision data with special runs with higher effective sampling frequency ($<$ 25 ns)

SC energy and timing





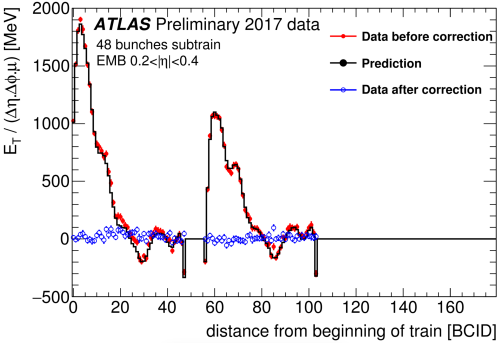
- Very narrow timing distribution for the SCs
- Used only for bunch cross identification → avoiding late or early triggers

- **Excellent agreement between cells** (main readout) and **SC energy** (DT)
  - Saturation at high energy expected and visible
  - Special bit transmitted to L1Calo for them

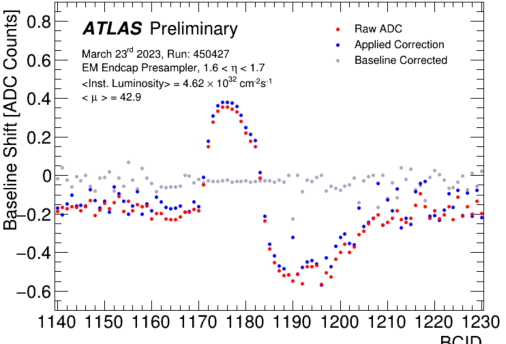
Pileup mitigation technique: LAr pulse is significantly longer than a bunch crossing

- OOT pileup raises the baseline ⇒ effect of overall higher reconstructed energy level
- Bipolar shaping partially compensates IT with OOT pileup
  - With trains, the cancellation is never perfect in particular at the start of the train
- Correction applied both in Main readout and Digital Trigger
  - Calculated and updated regularly per SC and Bunch Crossing ID (BCID)

Main readout

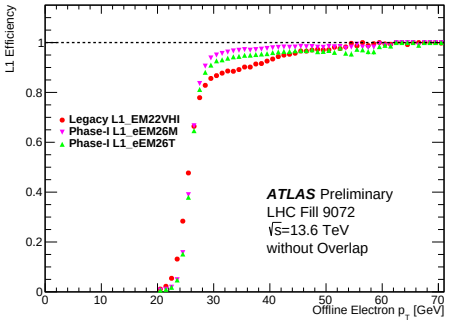


DT readout

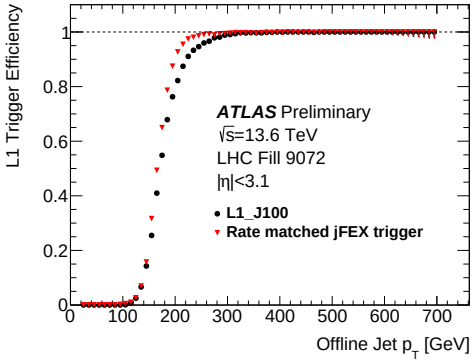


- **New L1Calo trigger system exploits fine granularity information** from the LAr SCs
- L1Calo uses Feature EXtractor (FEX) processors: electromagnetic, jet and global (eFEX, jFEX and gFEX)

Electromagnetic FEX



Jet FEX



- **Sharper turn-on curves with the same thresholds** for electrons and jets
- L1 rate **reduction around 10%** for the same thresholds

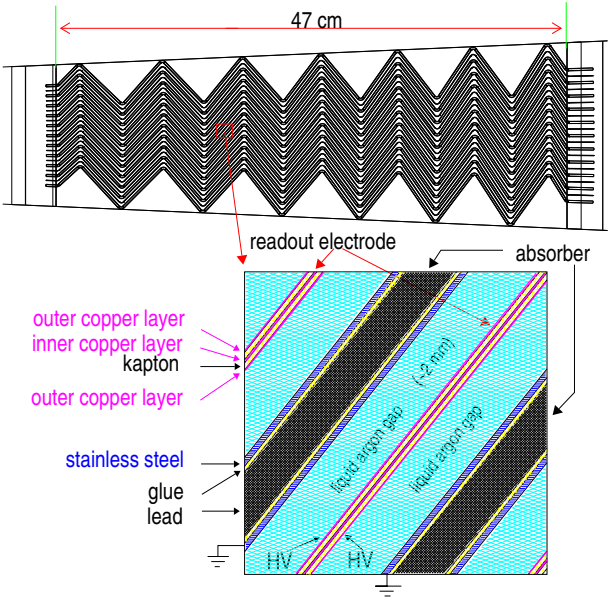
Conclusion

For Run 3, the ATLAS Liquid Argon calorimeter has been equipped with new electronics to implement a new Digital Trigger system to cope with harsher pileup conditions

- The new LAr Digital Trigger electronics system is **fully operational and performing well**
- The new system provides the L1Calo trigger with 10x more granularity, better precision and larger range than legacy
- The Legacy analog trigger has been decommissioned for EM and Jet items
- LAr Digital Trigger will still be in use for HL-LHC (next talk by Lauren!)

Backup

- 2.1 mm gap with ∼2 kV applied
- Particles interact with the absorber creating secondary particles ⇒ shower
- Secondary particles ionize LAr ⇒ collected by electrodes, drift time ∼450 ns,
- Current is read out, amplified and shaped (CR-RC^2)
- Signal then sampled and stored in analog memory on the Front End waiting for L1 trigger decision

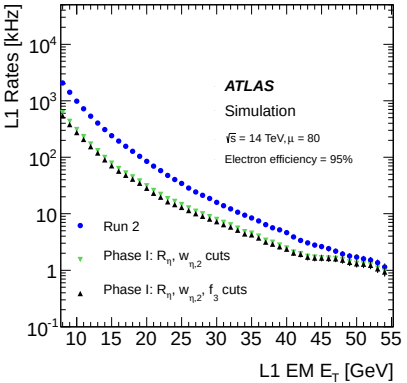


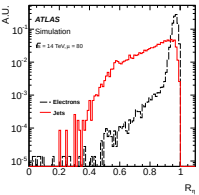
$$E_{\text{cell}} = F_{\text{DAC}\to\mu\text{A}} \cdot F_{\mu\text{A}\to\text{MEV}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \cdot G_1 \cdot \sum_{i=1}^{N^{\text{samples}}} a_i \left(s_i - p\right)$$

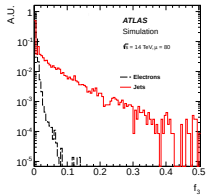
$F_{\text{DAC}\to\mu\text{A}}$	=	sampling fraction, converts calibration board DAC counts to current
$F_{\mu\text{A}\to\text{MEV}}$	=	factor which converts ionisation current in the calorimeter to total deposited E, from test-beam studies
$\frac{M_{\text{phys}}}{M_{\text{cali}}}$	=	ratio of maxima of physical and calibration pulses with the same input current
G_1	=	cell gain - ADC to DAC from calibration pulse
a_i	=	Optimal Filtering Coefficients (OFCs), derived from predicted pulse shape & noise autocorrelation
s_i	=	samples of the shaped signal digitised in a given electronic gain, measured in ADC counts
p	=	read-out electronic pedestal, measured for each gain

Three types of electronic calibration runs, **pedestals**, **ramps** and **delays** provide many of the inputs required for cell energy computation (as well as timing & quality factor).

➟ **Taken for both DT and main readout path.**



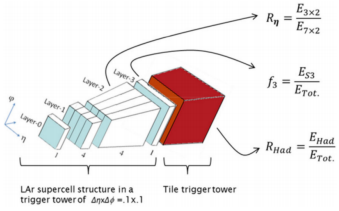




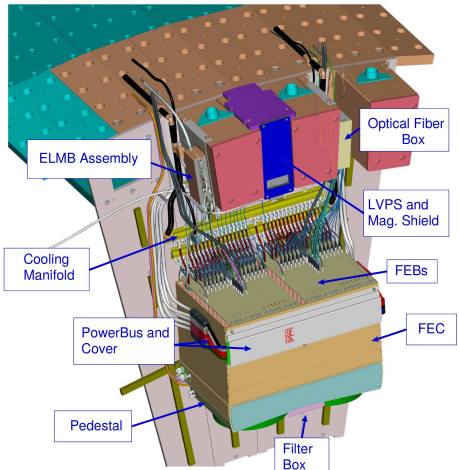
Use shower information as done in offline analysis to improve background rejection

Example 95% efficiency on electrons from $Z \rightarrow ee$ events with Run 3 conditions

- assuming Run 2 trigger algorithms: to have L1 rate 20 kHz need $E_T = 28.5$ GeV threshold
- Using shower shapes from SCs, lower to $E_T = 21$ GeV threshold



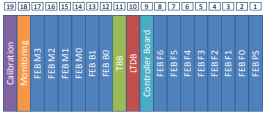
Moreover, improved L1 EM resolution $\Rightarrow$ substantially sharpen the trigger turn-on curves $\Rightarrow$ reduction offline E_T threshold and increase acceptance



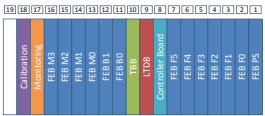
Front End crates contains most of the FE electronics for readout and trigger

- 1524 Front End Boards, each reading 128 channels
- Calibration boards
- Trigger Builder Boards (for TT building)
- From now on also LTDBs

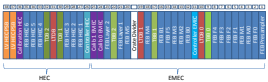
EMB



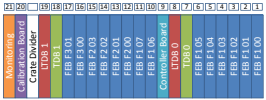
EMEC



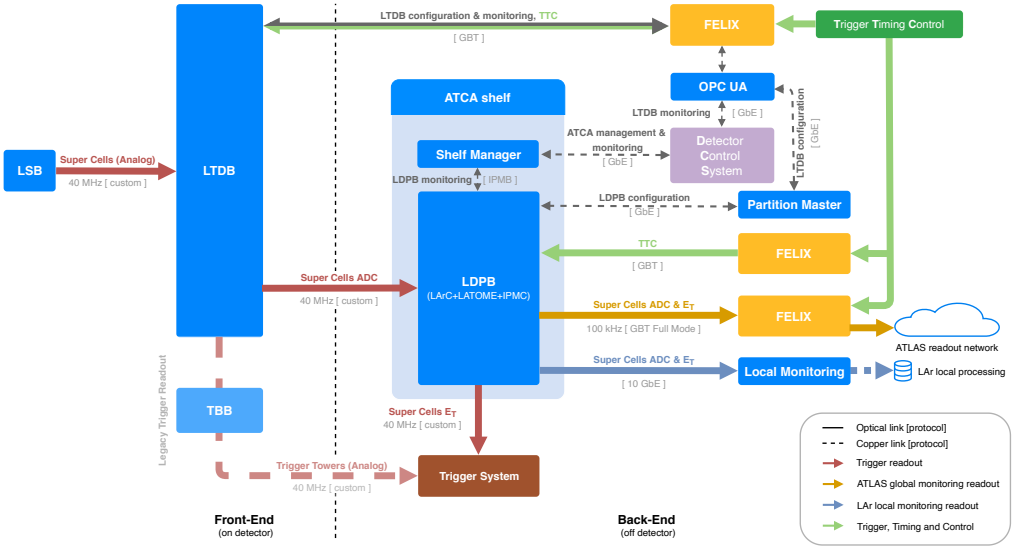
HEC and EMEC Special

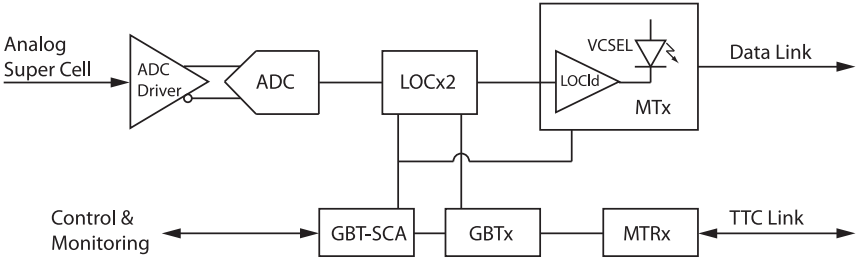


FCal



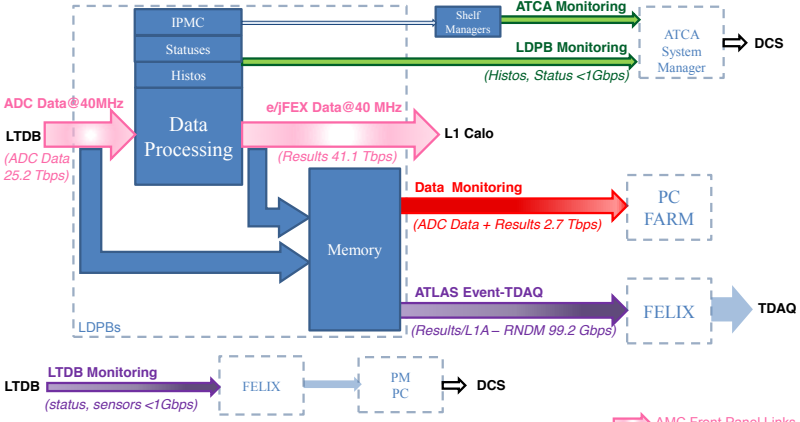
Digital trigger integration





LTDB digital section includes two signal flow paths: the data link and the control (TTC) link.

- data link: SC signals are digitized by the ADC, reorganized and serialized by LOCx2, and transmitted via the MTx over fiber optical links
- control link: the TTC link is responsible for clock distribution, slow control and monitoring; it is composed of the GBTx, GBT-SCA and MTRx
  - GBTx interfaces to the back end of the TTC system via MTRx over duplex fiber optical
  - GBTx and GBT-SCA chipset is used to provide clock distribution, slow control and monitoring on the LTDB.



LTDB: 124 Modules LDPB: 31 Blades

Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps