HKROC: an integrated front-end ASIC to readout photomultiplier tubes for large neutrino experiments.

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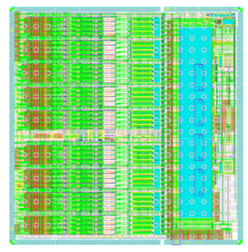
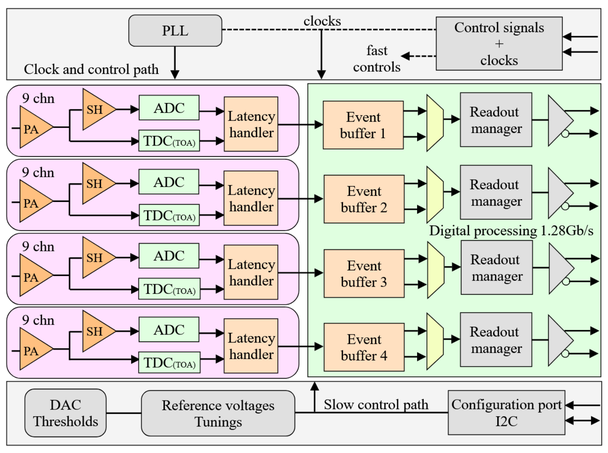
Abstract

The HKROC ASIC was originally designed to readout the photomultiplier tubes (PMTs) for the Hyper-Kamiokande (HK) experiment. HKROC is a very innovative ASIC capable of readout a large number of channels satisfying stringent requirements in terms of noise, speed and dynamic range. Each HKROC channel features a low-noise preamplifier and shapers, a 10-bit successive approximation Analog-to-Digital Converter (SAR-ADC) for the charge measurement (up to 2500 pC) and a Time-to-Digital Converter (TDC) for the Time-of-Arrival (ToA) measurement with 25 ps binning. HKROC is auto-triggered and includes all necessary ancillary services as bandgap circuit, PLL (Phase-locked loop) and threshold DACs (Digital to Analog Converters). This presentation will describe the ASIC architecture and the experimental results of the last prototype received in January 2022.



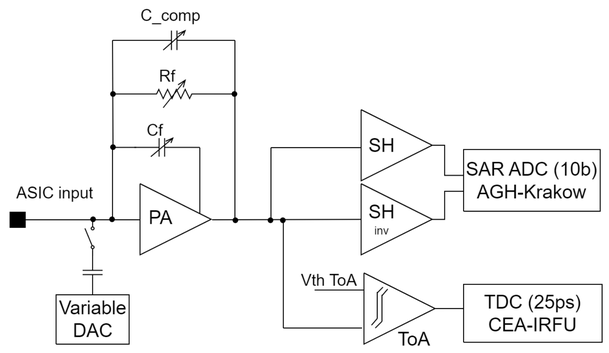
HKROC layout design.

HKROC Architecture



- ASIC developed in 130 nm CMOS technology (1.2 Volts).
- 36 input channels, possibly grouped by 3 to cope with large dynamic ranges.
- Embedded charge and time measurements provided by ADC and TDC.
- 4 readout high-speed links (1.28 Gbps).
- Auto-triggered waveform digitizer.
- I2C protocol to load ASIC parameters.
- 10 mW / channel during acquisition phase.

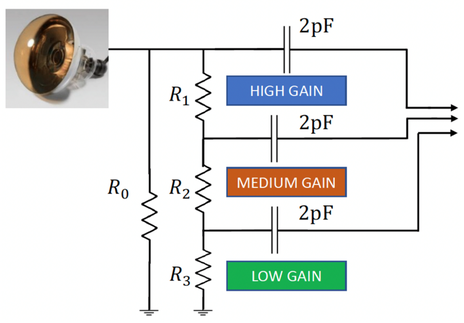
Front-end architecture of one channel of HKROC



- Preamplifier (PA) gain configurable with R_f (25 kΩ to 7.5 MΩ) and C_f (100 fF or 200 fF), C_{comp} (50 fF to 750 fF).
- Feedback capacitor split into C_f and C_{comp} to improve preamplifier stability.
- 10-bit SAR-ADC and 10-bit TDC per channel (25 ps resolution).
- Ajdustable TOA threshold per channel.
- Embedded calibration input DAC.
- Charge measurement up to 1250 p.e. (2500 pC) when channels grouped by 3.

Waveform digitizer

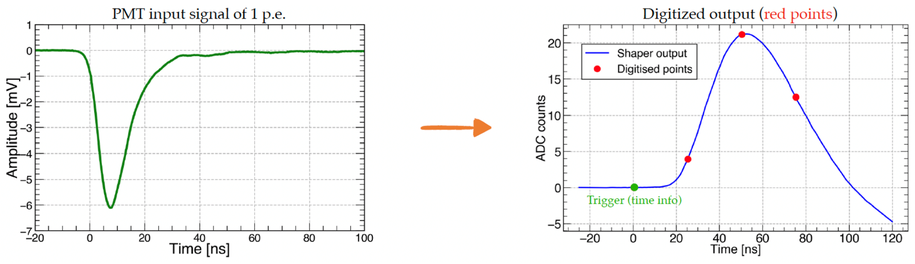
- On-board analog 3-gain splitter:



- HKROC has 3 operating mode for hit-rate optimization (normral, Supernova and ultra-fast).
- Each channel is readout with its ADC and TDC samples.

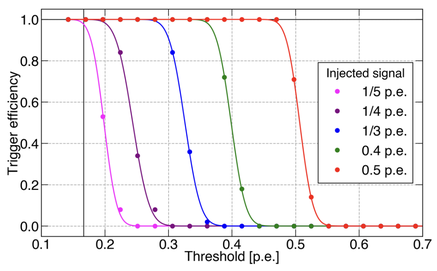
4b D header	2b Mode	24b Timestamp (TS)		2b CRC
4b D header	6b hit map Q+T	10b Time	10b Charge HG	2b CRC
4b D header	6b hit map Q+T	10b Time	10b Charge MG	2b CRC
4b D header	6b hit map Q+T	10b Time	10b Charge LG	2b CRC

- For each autotrigger, HKROC samples N points (1 to 7) on the waveform.



Charge measurements

- Trigger efficiency S_{curves} versus threshold:

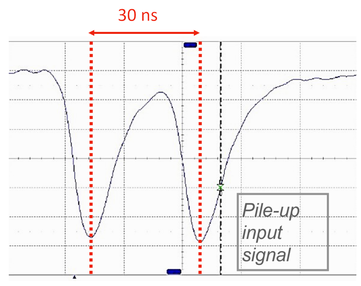


- Charge reconstruction is based on reference waveforms stored in an FPGA. The digitized points are used to find the associated charge.

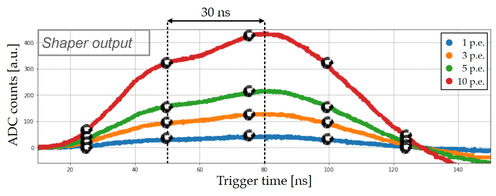
$$\chi^2(\alpha) = \sum_{i=1}^{N} \left(\frac{y_i - \alpha w_i}{\sigma_i} \right)^2$$

$$\rightarrow \frac{d\chi^2}{d\alpha} = 0 \Leftrightarrow \alpha = \frac{\sum_{i=1}^{N} \frac{y_i w_i}{\sigma_i^2}}{\sum_{i=1}^{N} \frac{w_i^2}{\sigma_i^2}} \Rightarrow q = \alpha q_{ref}$$

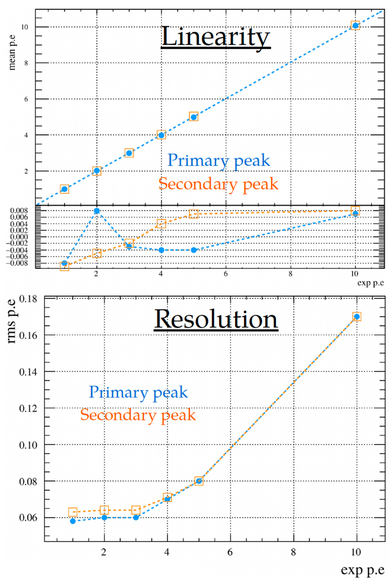
- Pile-up event (30 ns separation) can be reconstructed with a joint fit.



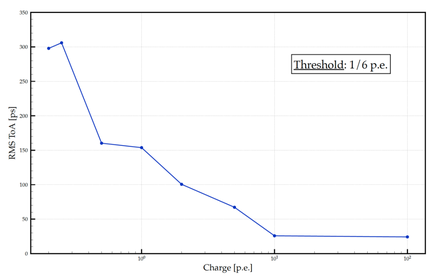
- Acquisition windows is dynamically extended to capture the full event (charge shaper output below).



- Capability to reconstruct both peaks of the event with 1% linearity and resolution less than 0.1 p.e. up to 5 p.e.

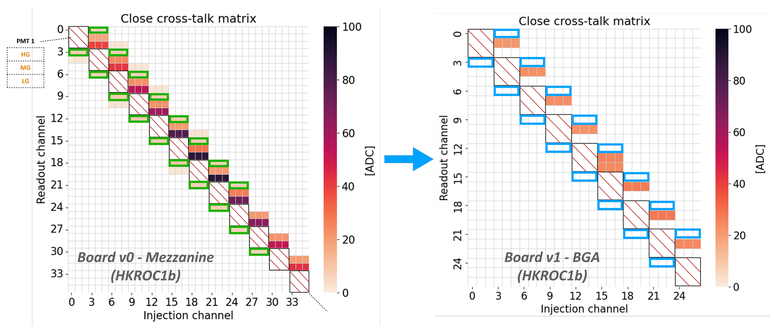


Time measurement



- Noise of 150 ps measured for a 1 p.e. charge (2 pC).
- Noise of 25 ps for charge greater than 10 p.e. (20 pC).
- One global 10b-DAC to adjust the discriminators' thresholds.
- One local trimming 6b-DACs to reduce the dispersion per channel.

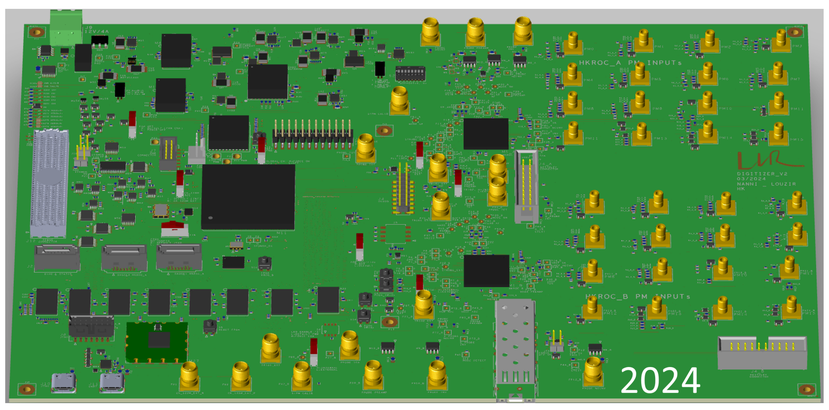
Close crosstalk measurements



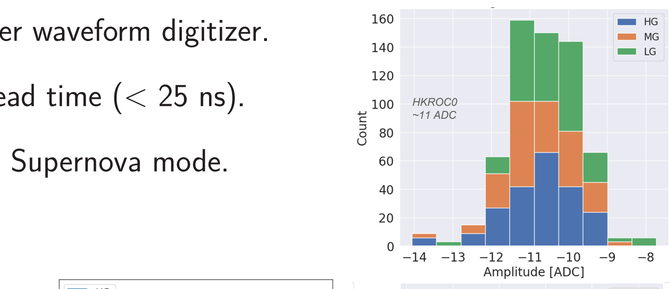
- HKROC crosstalk measurements made on 2 setups: mezzanine board and testboard.
- By optimizing input routing layers on the PCB, high-gain channels are immune to coupling.
- Different PCB layer were used to mitigate HG coupling (2 on right side plot).
- Production front-end board will use 3 routing layers to further improve the results.

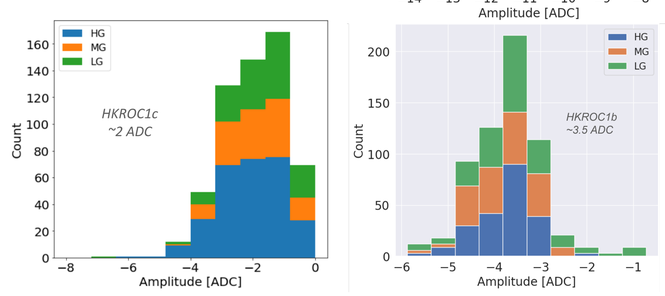
Conclusion and prospects

- An HKROC-based acquisition board (21 x 29 cm) is being produced including two HKROCs and an FPGA to perform the DAQ and the charge reconstruction.



- HKROC is an extremely versatile and low-power waveform digitizer.
- It features a 10 mW per channel with a low dead time (< 25 ns).
- Hit-rate capability up to 1 MHz in the specific Supernova mode.
- Time measurement noise of 25 ps.
- Reconstruction algorithm are sensitive to diffuse crosstalk (for t0 reconstruction). It has been reduced by a factor of 3 in HKROC1b compared to the first ASIC iteration. Then HKROC1b meets all the requirements.
- HKROC1c (received in May 2024) further improve it by 30 % and will open the possibility to simplify the charge reconstruction algorithm (t0 reconstruction).





20^{th} International Conference on Calorimetry in Particle Physics