Beam test of a baseline vertex detector prototype for CEPC

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On behalf of CEPC vertex detector group

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Circular Electron Positron Collider (CEPC)

➡ Higgs/Z/WW factory proposed at 2012

- 100 Km long accelerator rings
- $\sqrt{s}$ = 240/91/160 GeV for Higgs/Z/WW

➡ Lots of physics program

- ZH run: 1×10^{6} Higgs
- Z pole: > 7×10^{11} Z
- WW: 2×10^{7}

CEPC Operation mode		ZH	Z	W^+W^-	ttbar
$\sqrt{s}$ [GeV]		~ 240	~ 91.2	~ 160	~ 360
Run time [years]		7	2	1	-
CDR (30MW)	L / IP [$\times10^{34}$ $cm^{-2}s^{-1}$]	3	32	10	-
	$\int L\,dt$ [ab^{-1}, 2 IPs]	5.6	16	2.6	-
	Event yields [2 IPs]	1×10^{6}	7×10^{11}	2×10^{7}	-

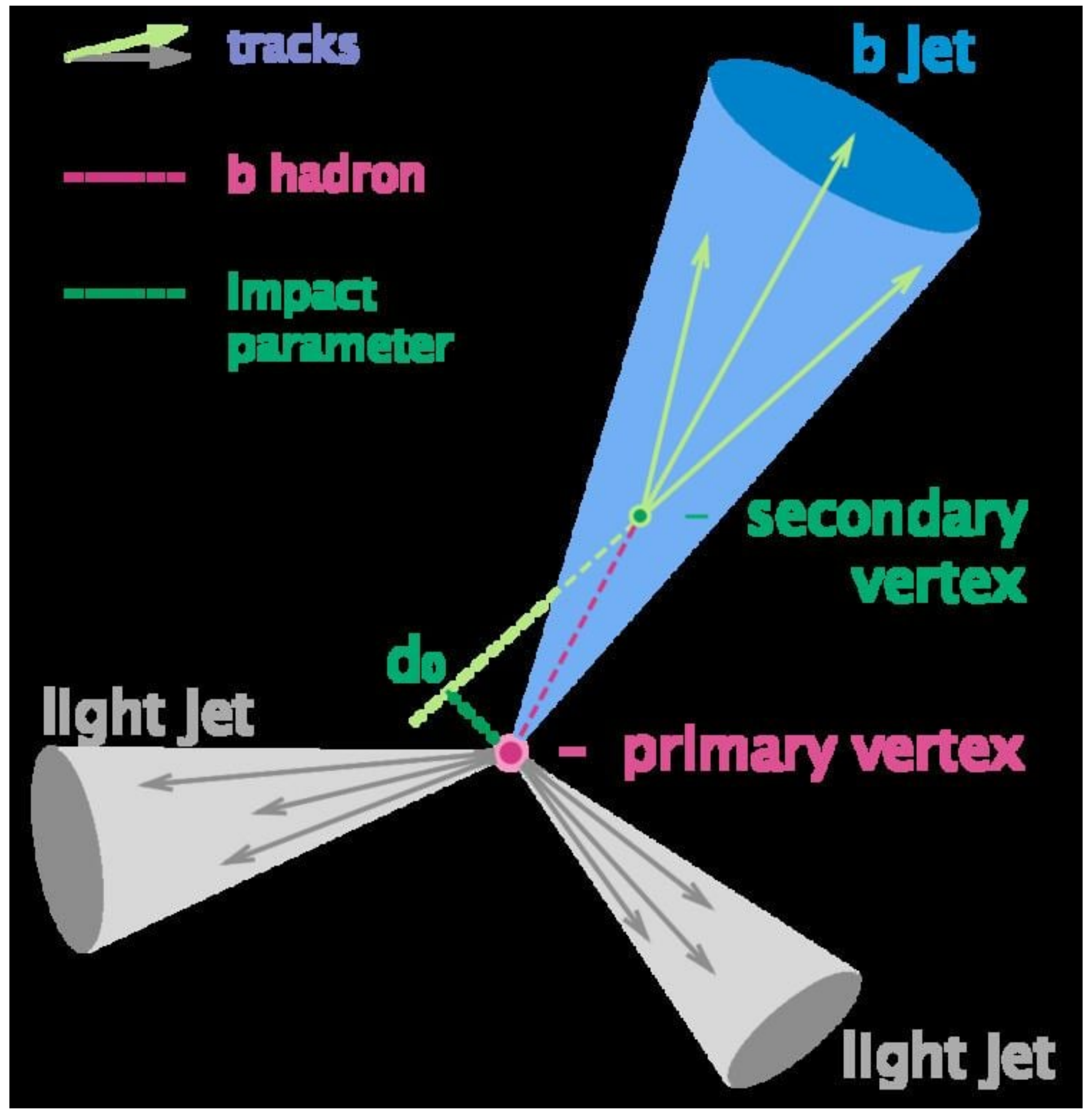
Vertex detector for CEPC

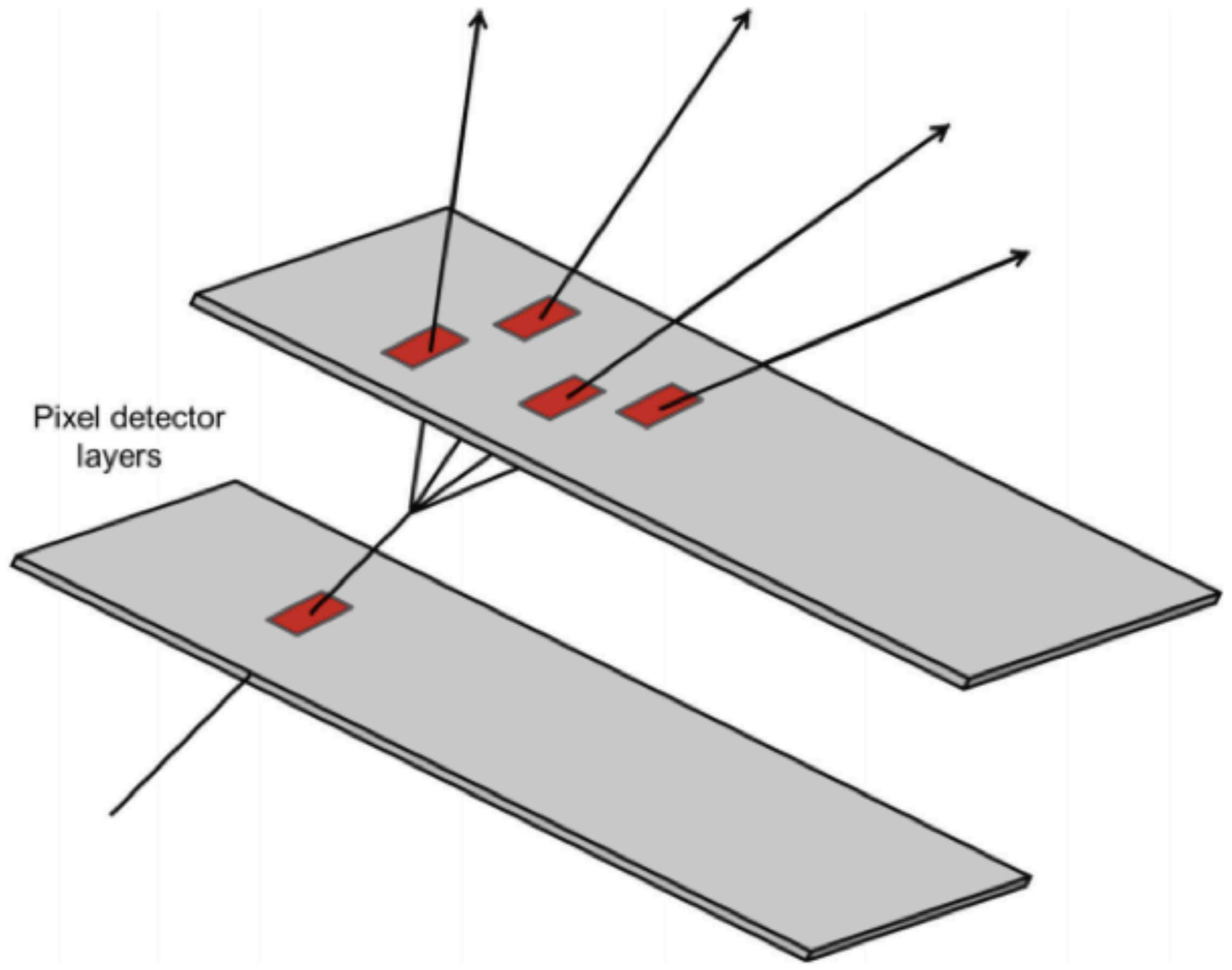
➡ High-precision vertex detector essential

- Flavor physics (b/c-quark jets, τ leptons)
- Higgs physics (H->bb/cc/gg and H->$\tau\tau$)

➡ Main requirements from CDR

- Single-point resolution: < 3 μm (~16 μm pixel pitch)
- Material budget: < 0.15 % X_0/layer
- Power consumption: < 50 mW/cm^2, if air cooling used



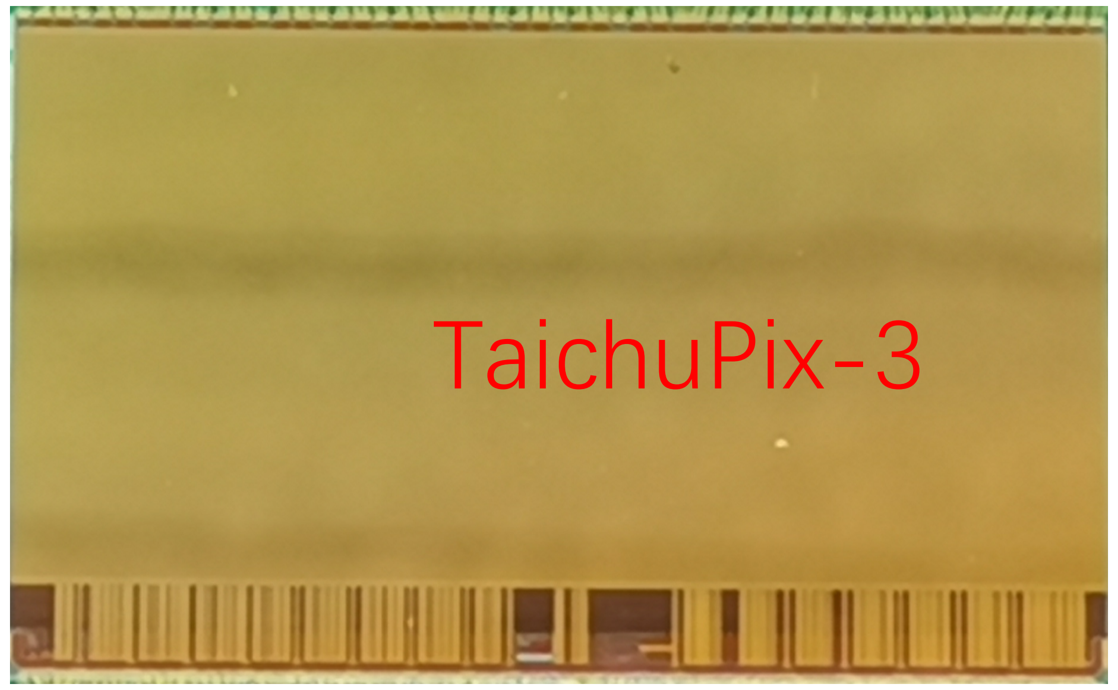


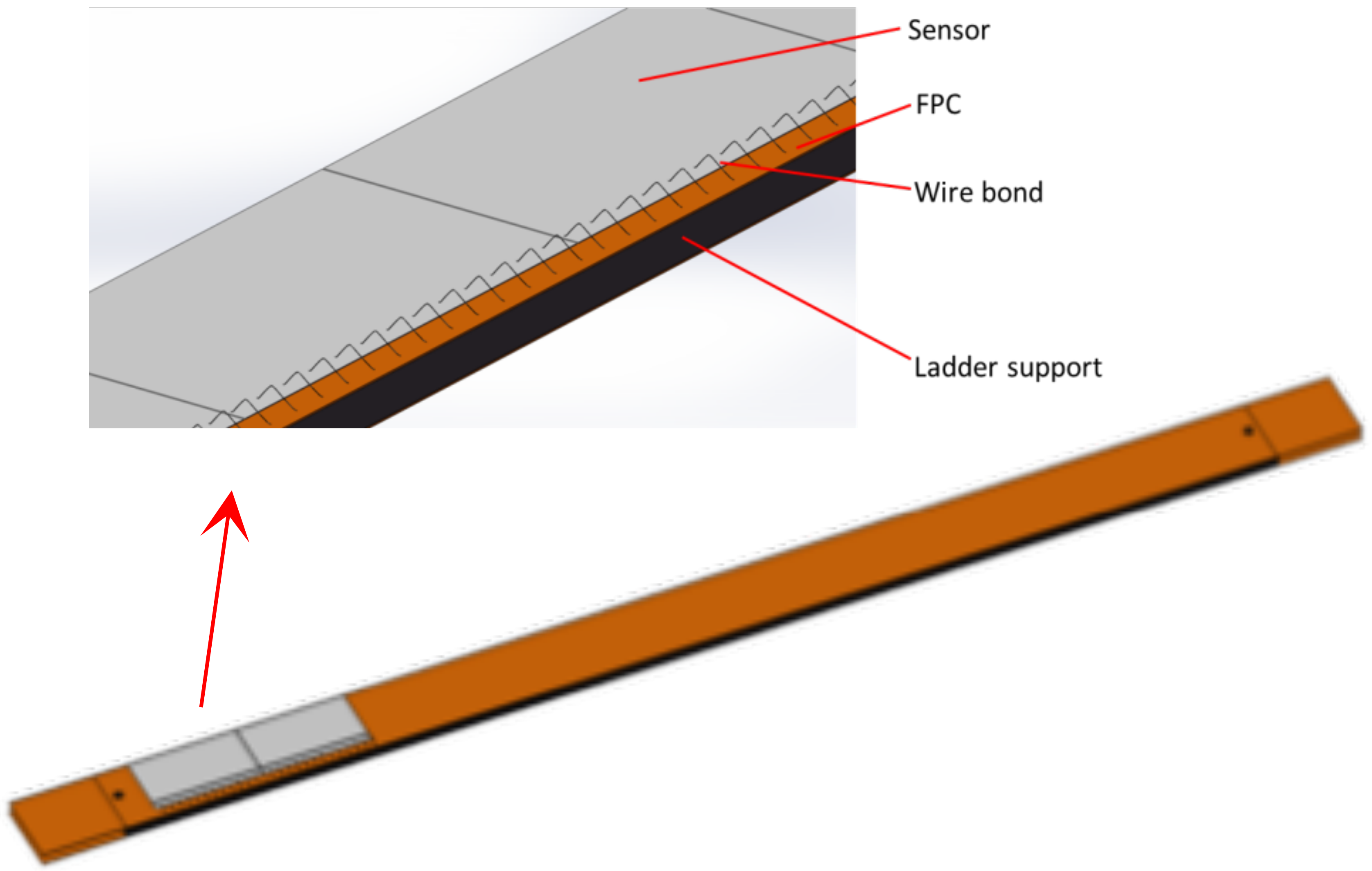
Overview of a baseline vertex detector R&D

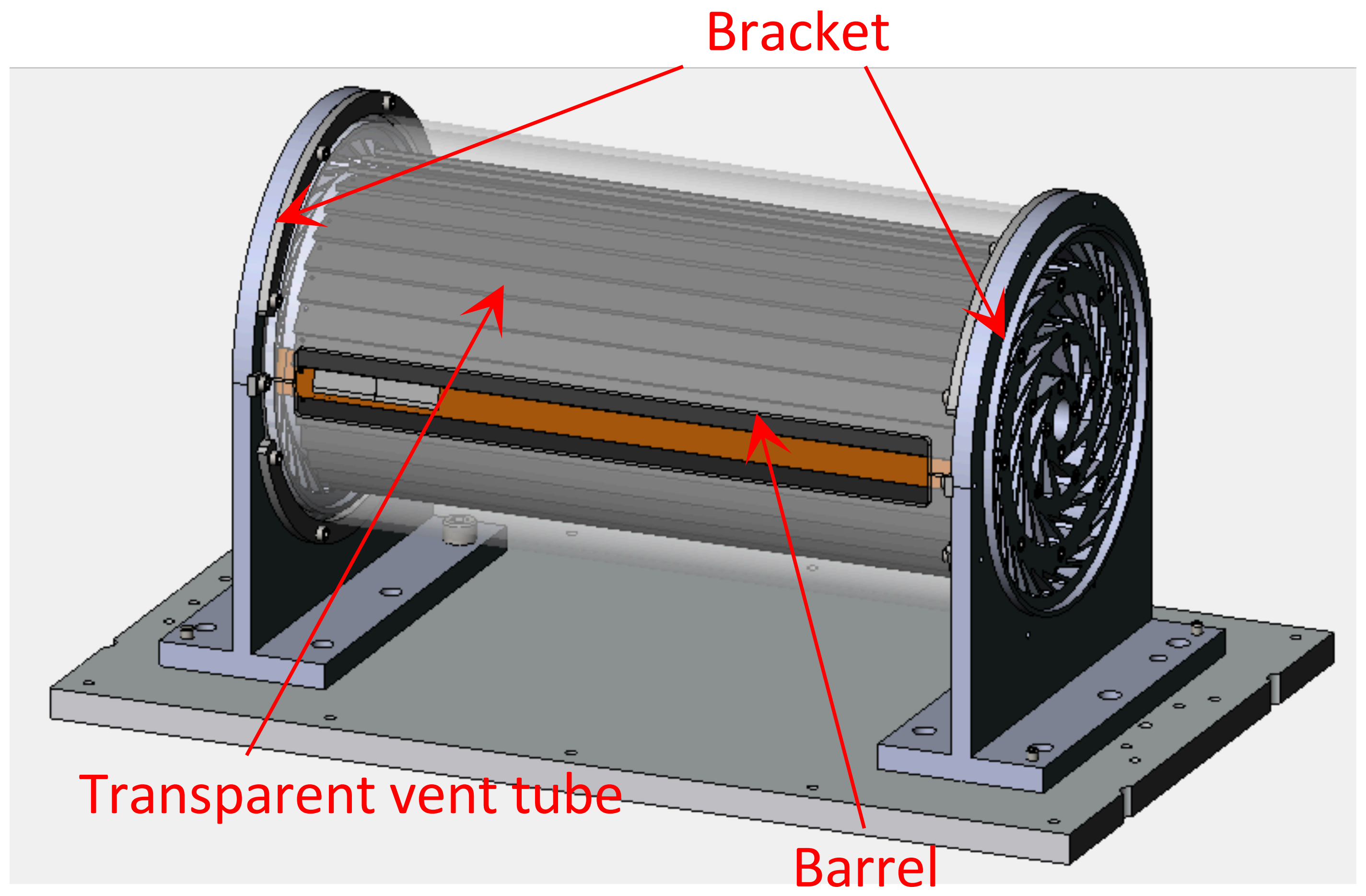
➡ Sub-projects

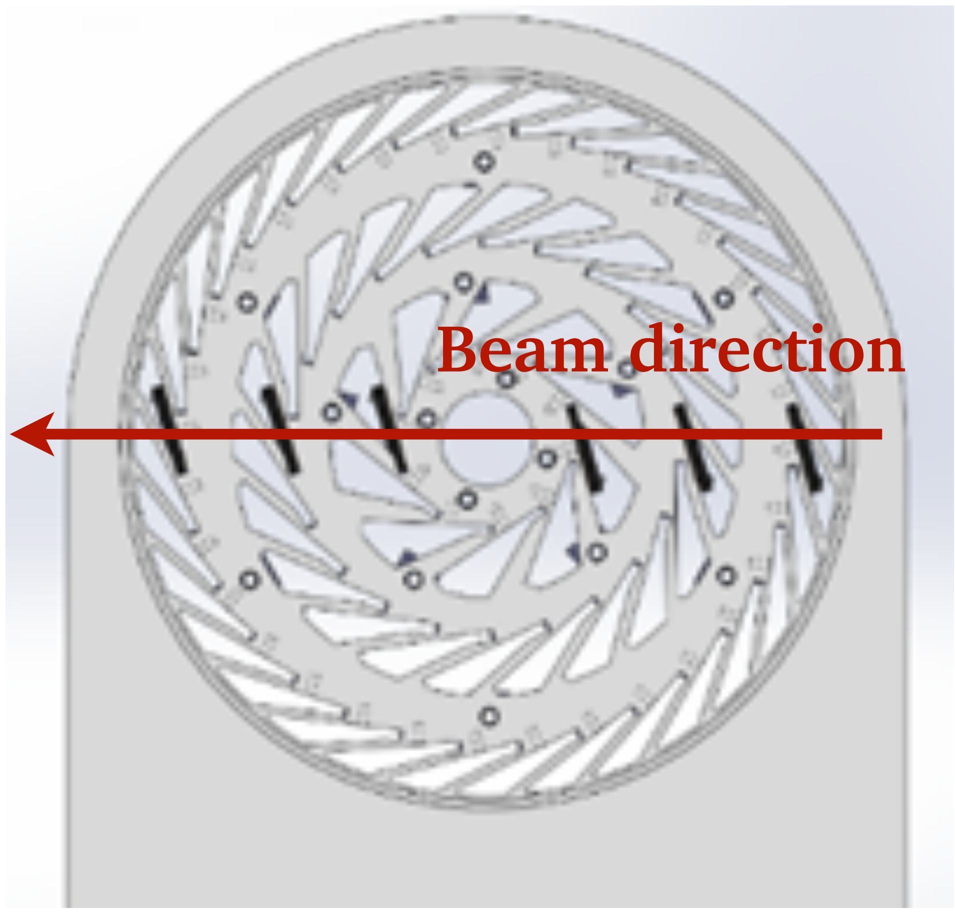
- CMOS pixel sensor R&D
- Detector module prototyping
- Detector assembly

CMOS pixel sensor prototyping









CMOS pixel sensor — TaichuPix

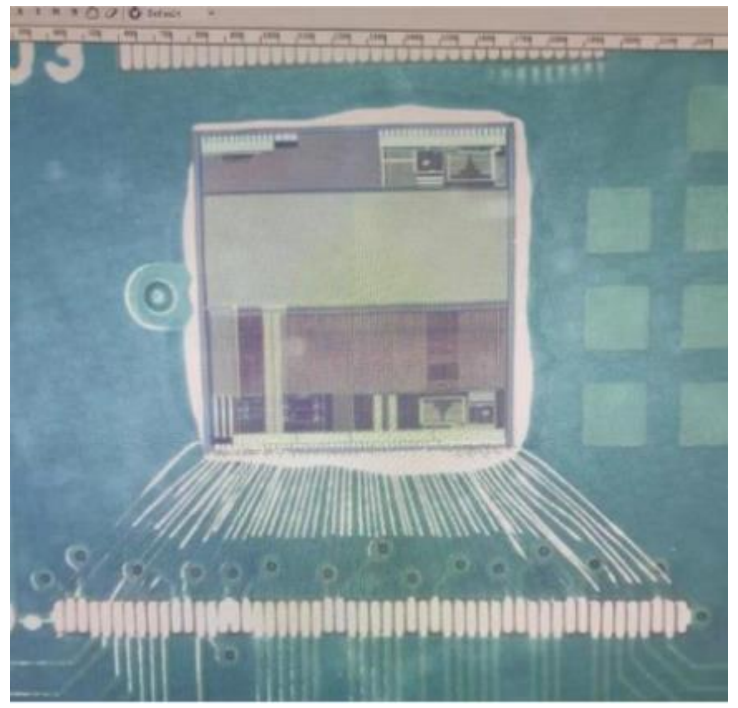
- More details about the TaichuPix chip design and readout architecture can be found in these papers: TaichuPix-1, TaichuPix-2, readout architecture

➡ A Monolithic Active Pixel Sensor (MAPS) prototype

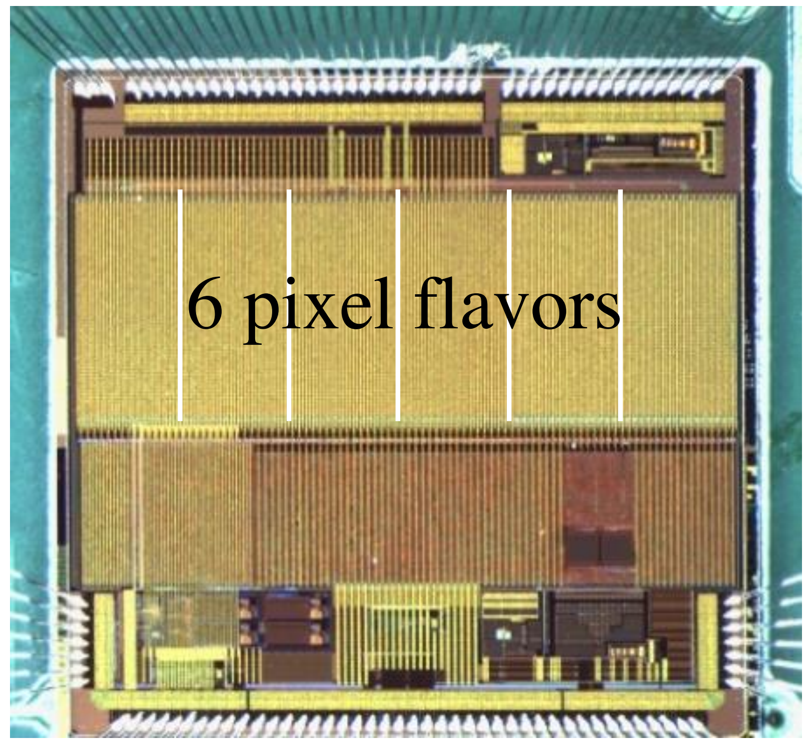
- 180 nm CMOS Imaging Sensor (CIS) technology
- pixel pitch: 25 μm
- 25 μm high-resistive epitaxial layer

➡ The evolution of the TaichuPix sensor

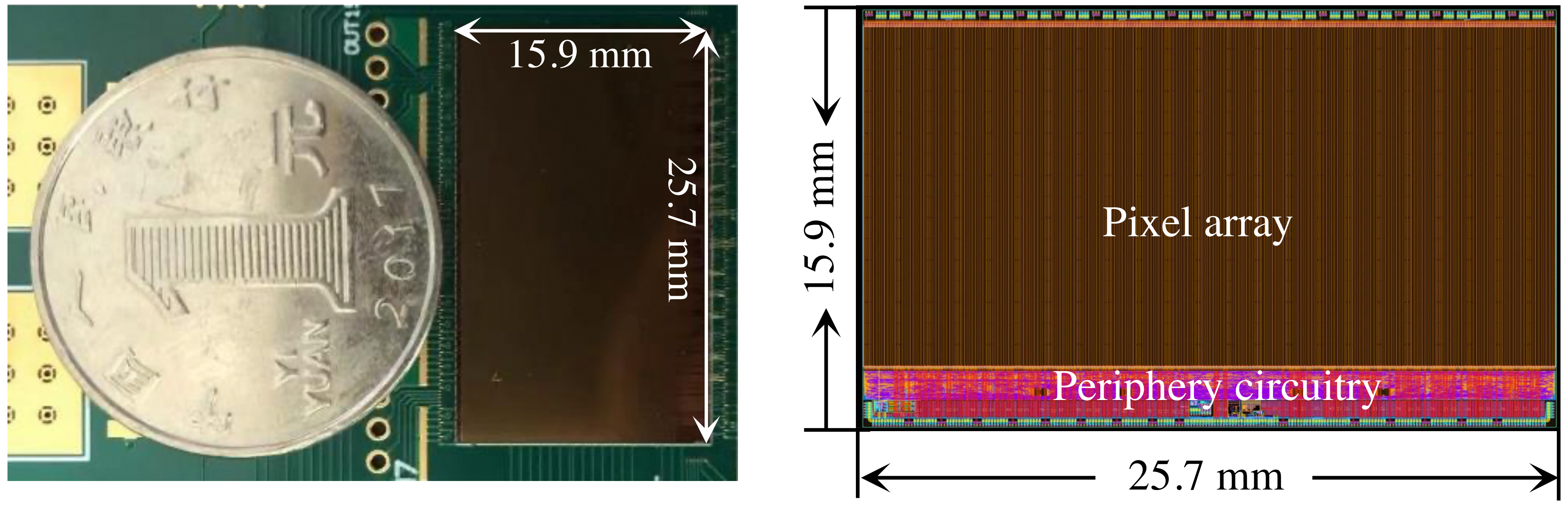
- Two multi-project chips: TaichuPix-1 and TaichuPix-2 (Chip size: 5 mm x 5 mm)
- The first engineering run chip: TaichuPix-3 applied for CEPC vertex detector prototype
  - Full scale: 25.7 mm x 15.9 mm
  - Pixel matrix: 1024 columns x 512 rows
  - Double-column data driven readout architecture



TaiChuPix-1



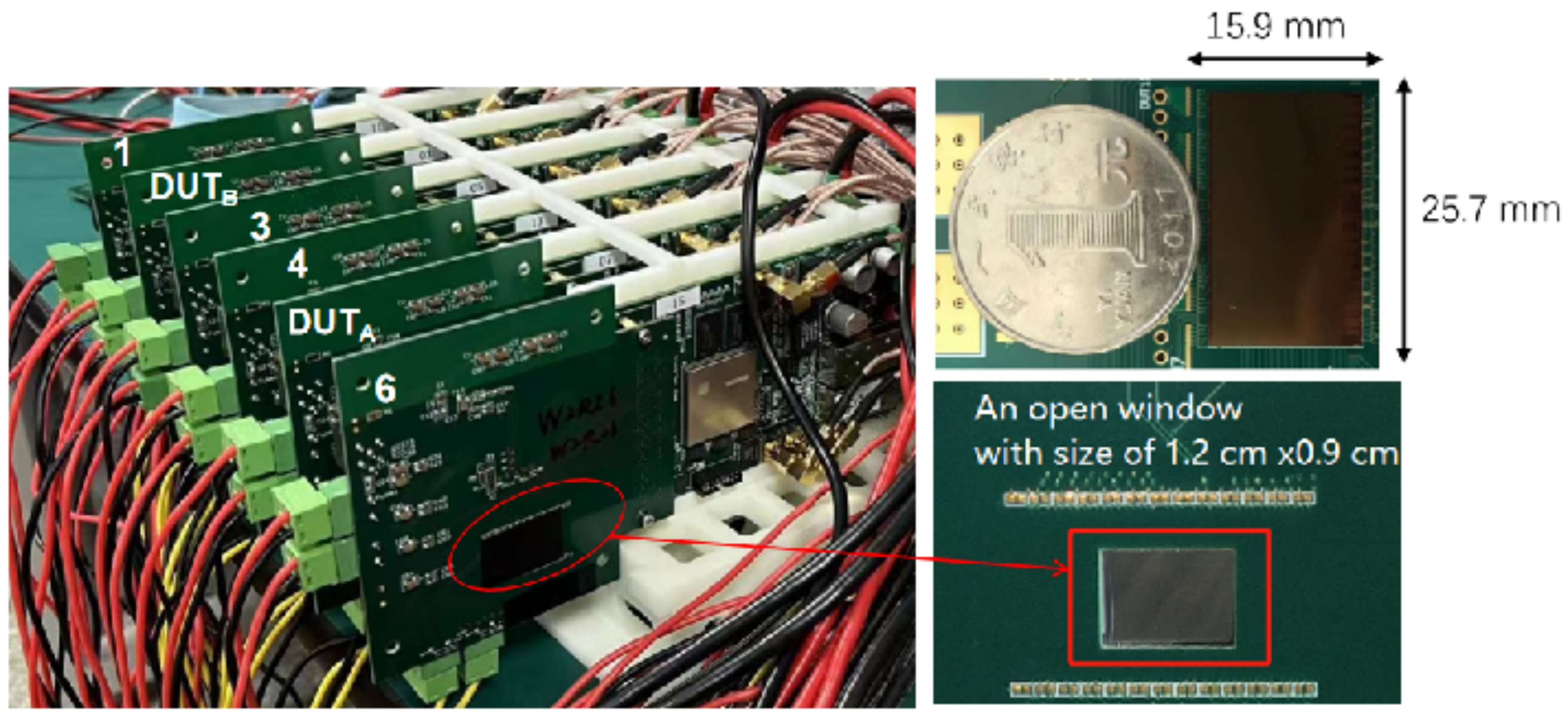
TaiChuPix-2

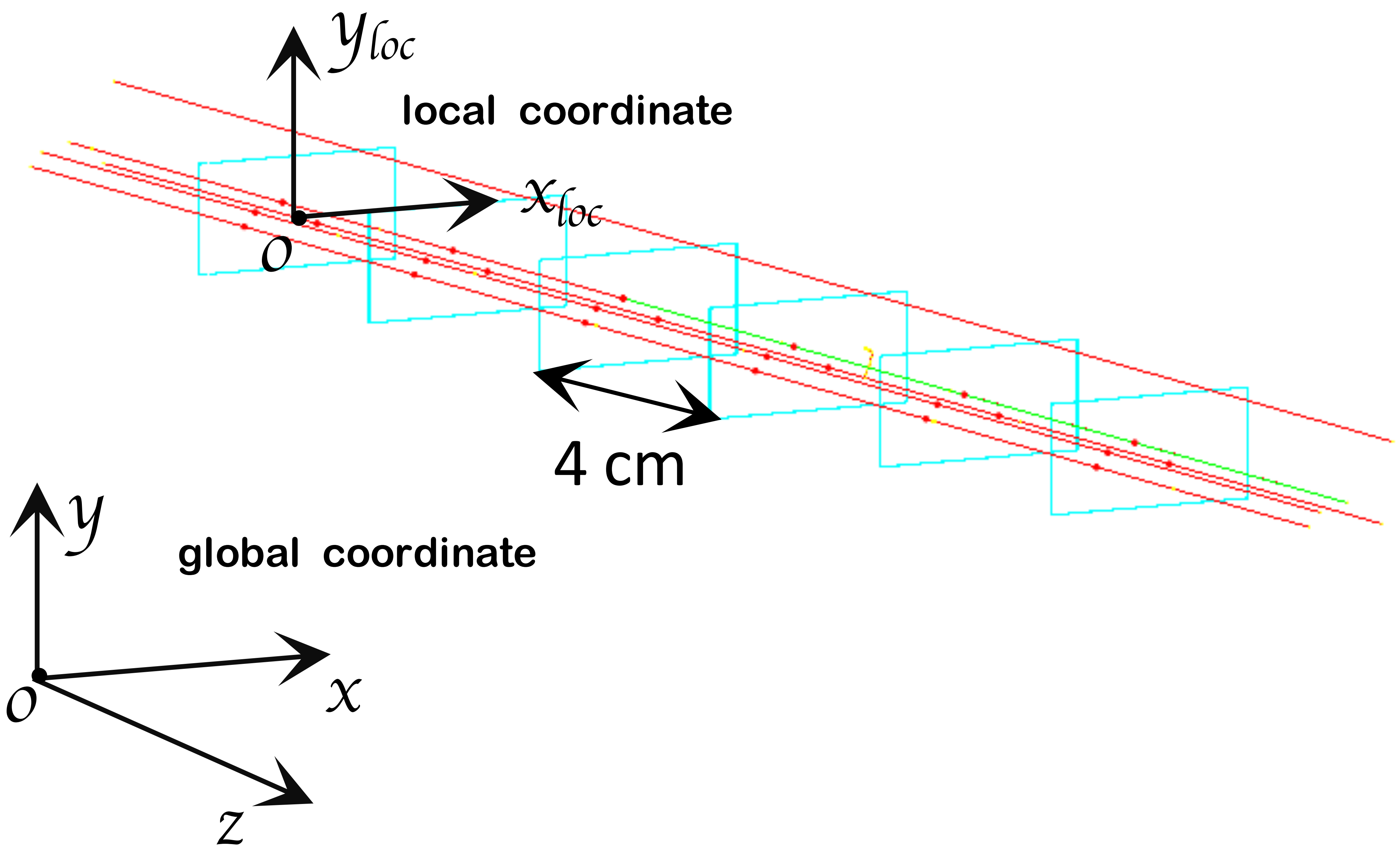


TaiChuPix-3

➡ Characterisation of the TaichuPix-3

- Beam telescope with TaichuPix-3 tested @ DESY II (2022.12)





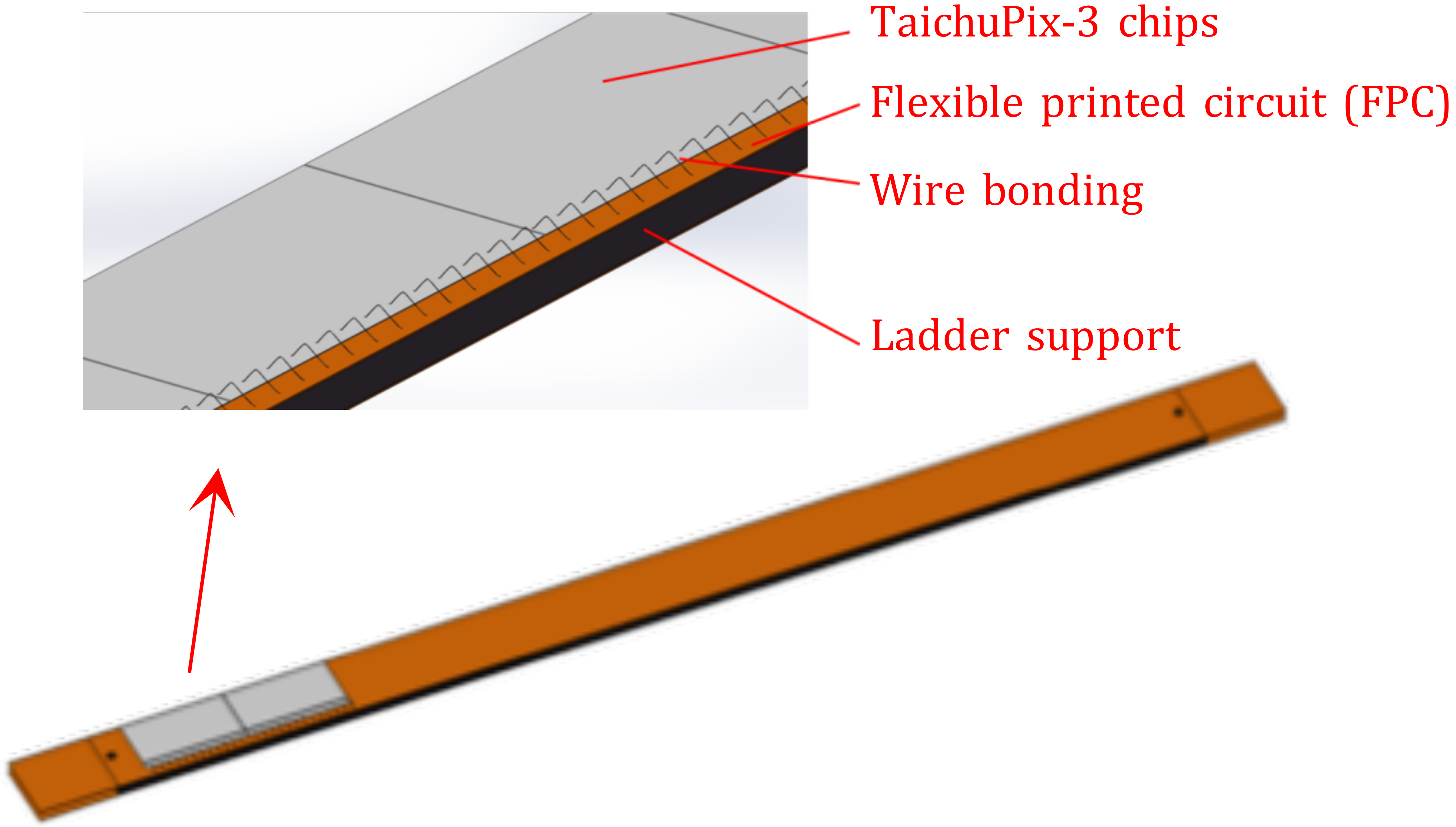
- Process[1]
  - DUT$_B$: Standard process
  - DUT$_A$: Modified process with an extra low dose n-type layer compared to DUTB (larger depletion region, faster charge collection)
- Characterisation[2]
  - Spatial resolution: 4.5 μm for DUT$_B$, 4.8 μm for DUT$_A$
  - Efficiency: both > 99 % for DUT$_B$ and DUT$_A$

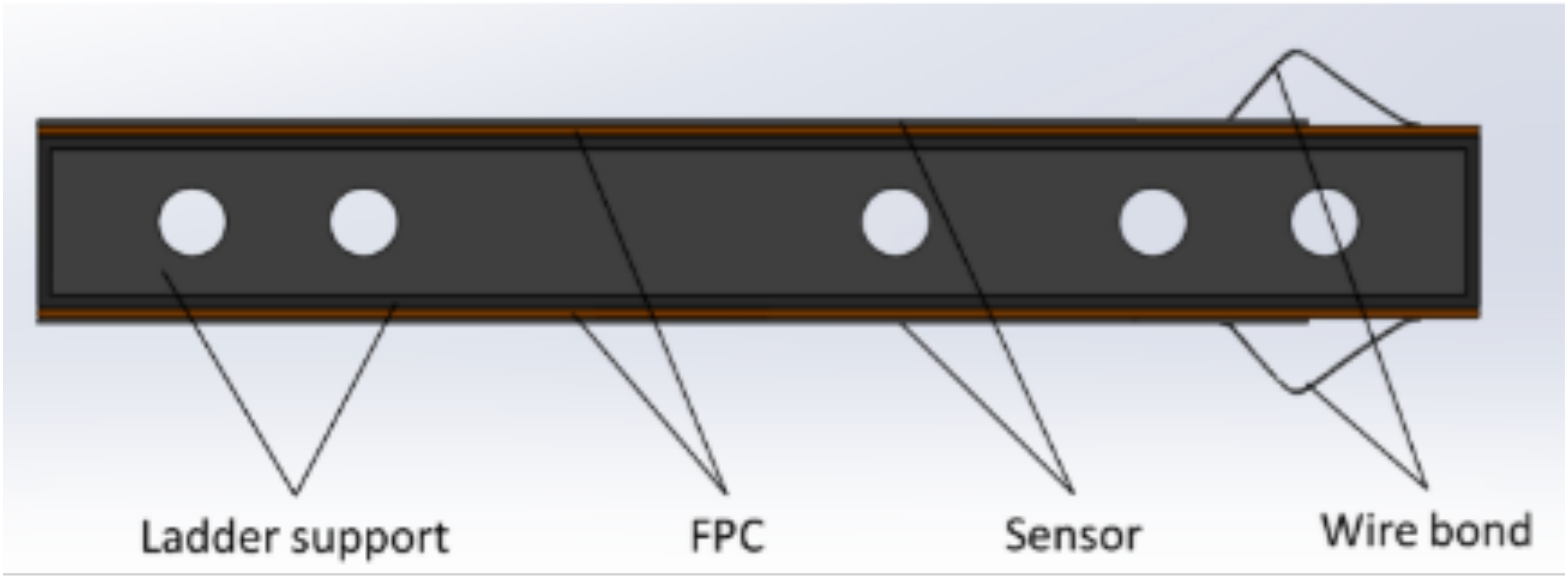
[1] W. Snoeys et al., “A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance,” Nucl. Instrum. Meth. A, vol. 871, pp. 90–96, 2017.
[2] T. Wu, S. Li, W. Wang et al., “Beam test of a 180 nm cmos pixel sensor for the CEPC vertex detector,” Nucl. Instrum. Methods A, vol. 1059, p. 319 168945, 2024.

Vertex detector module prototyping

➡ Detection module — Ladder

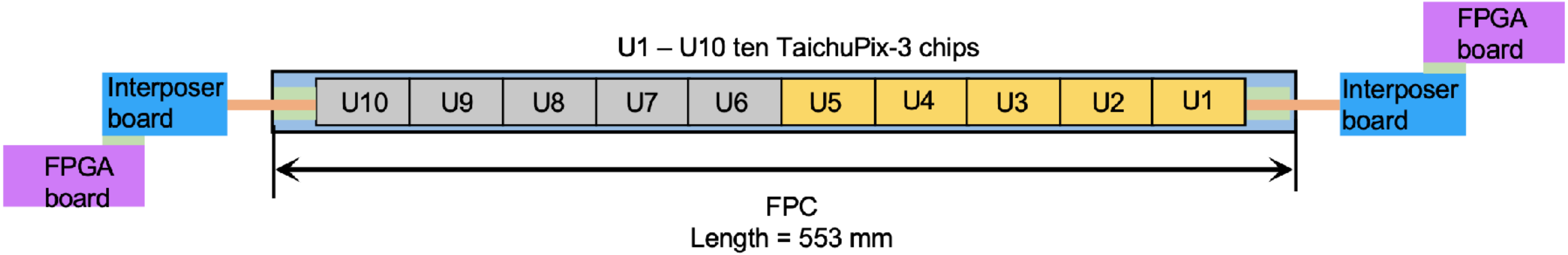
- TaichuPix-3 chips (maximum 10, both side) + FPC (both side) + carbon fiber support structure
- Two FPCs are glued to the both sides of the ladder support
- Sensors are glued and wire-bonded to the FPC

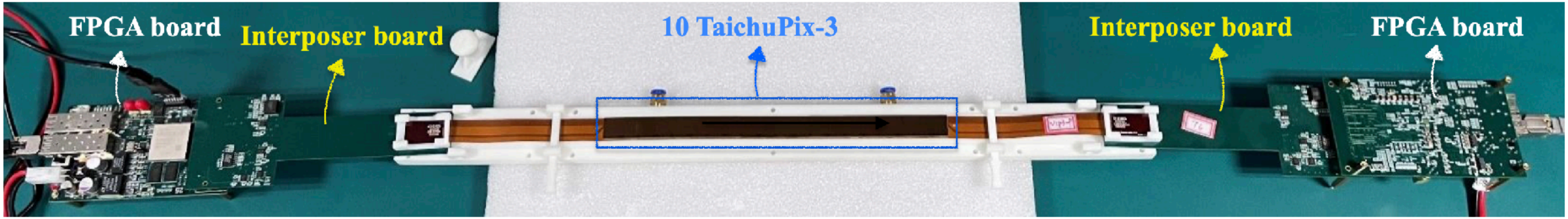




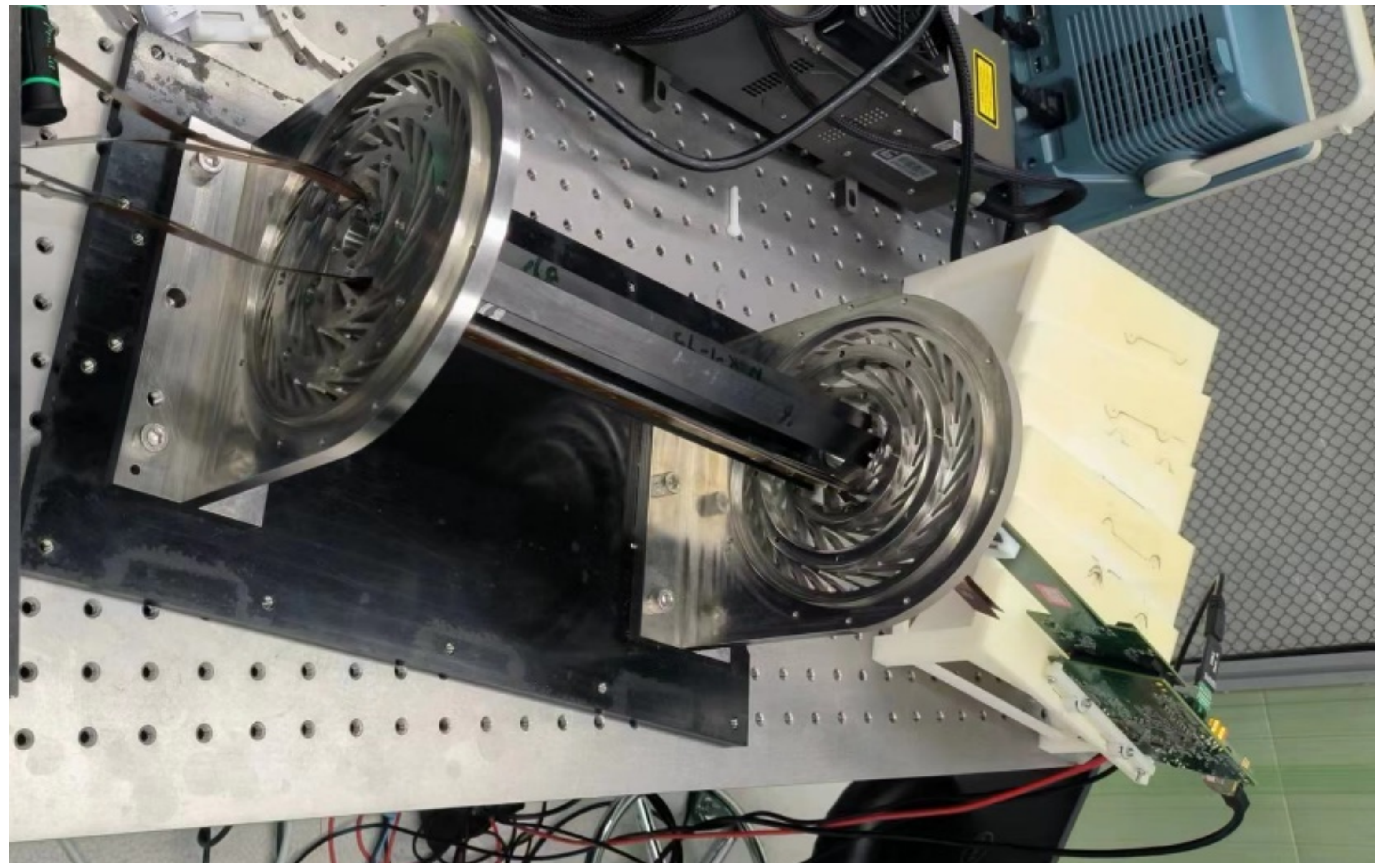
➡ Readout board for ladder

- Read out from both ends
  - FPC: power and ground routing for chips, control bus, receive data and clock
  - Interposer board: linear regulator, DAC, data link
  - FPGA board: chip configuration, package data, FIFOs

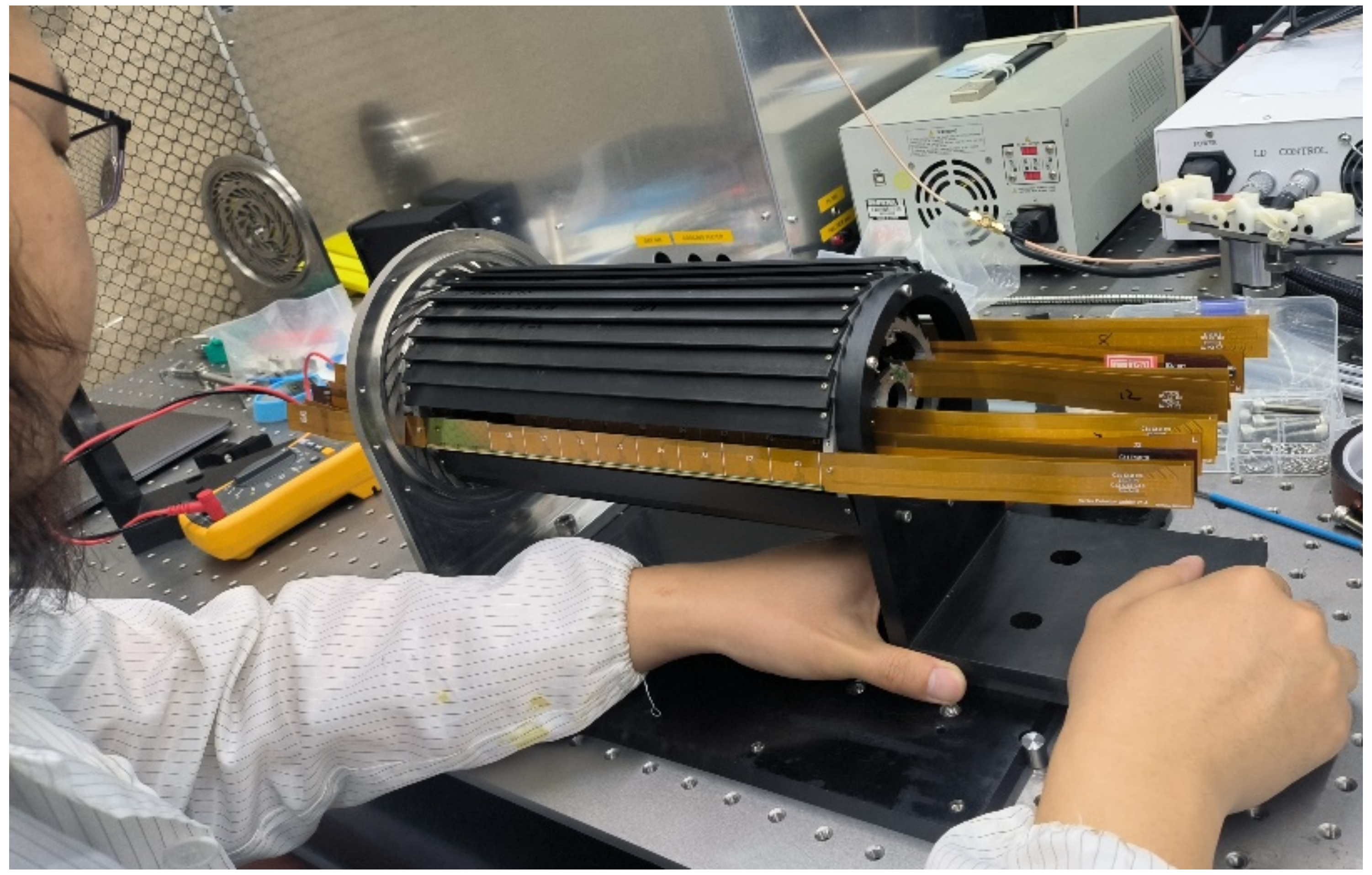




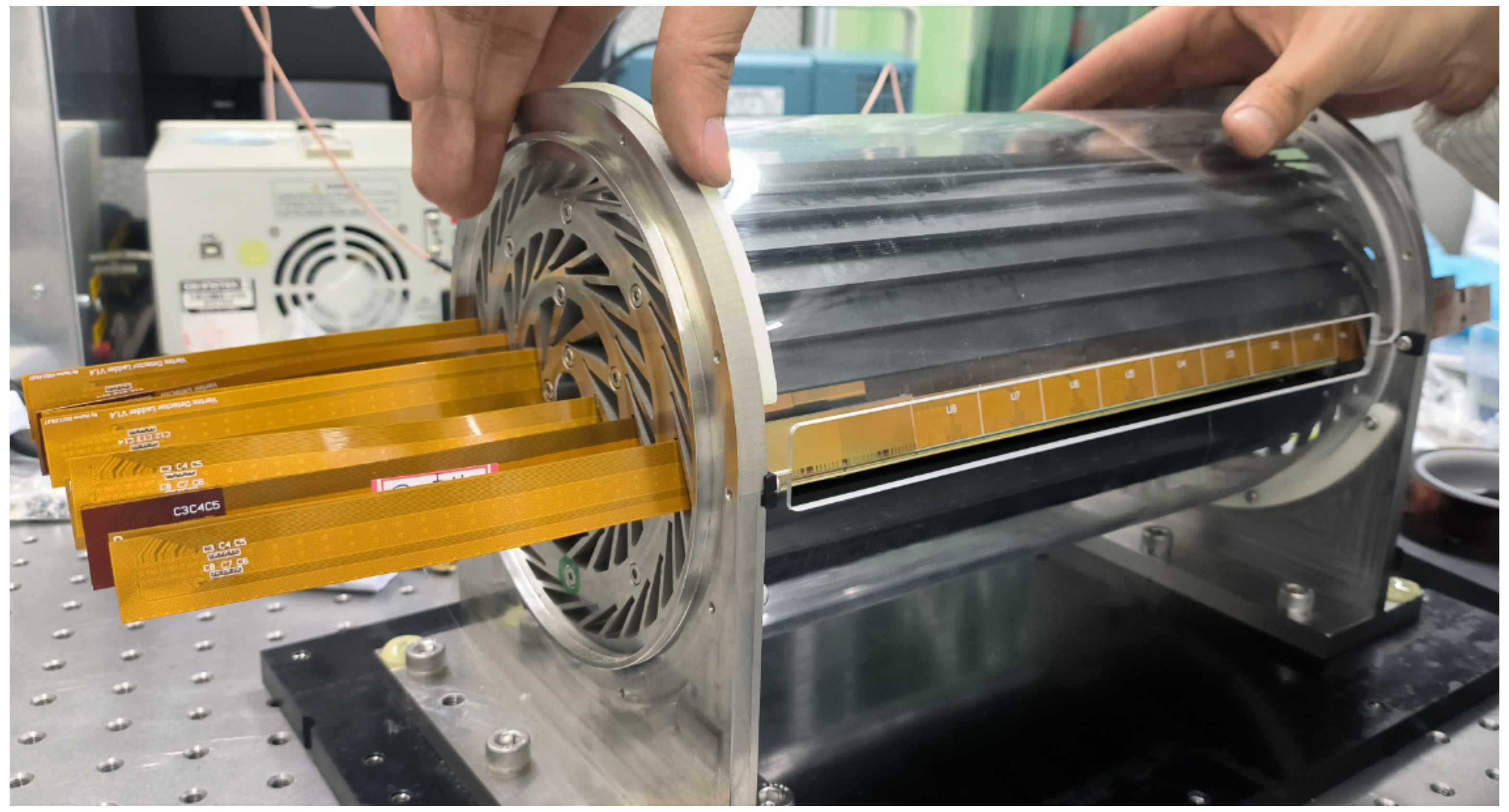
Vertex detector prototype assembly



1. Six ladders were installed along the radiational direction



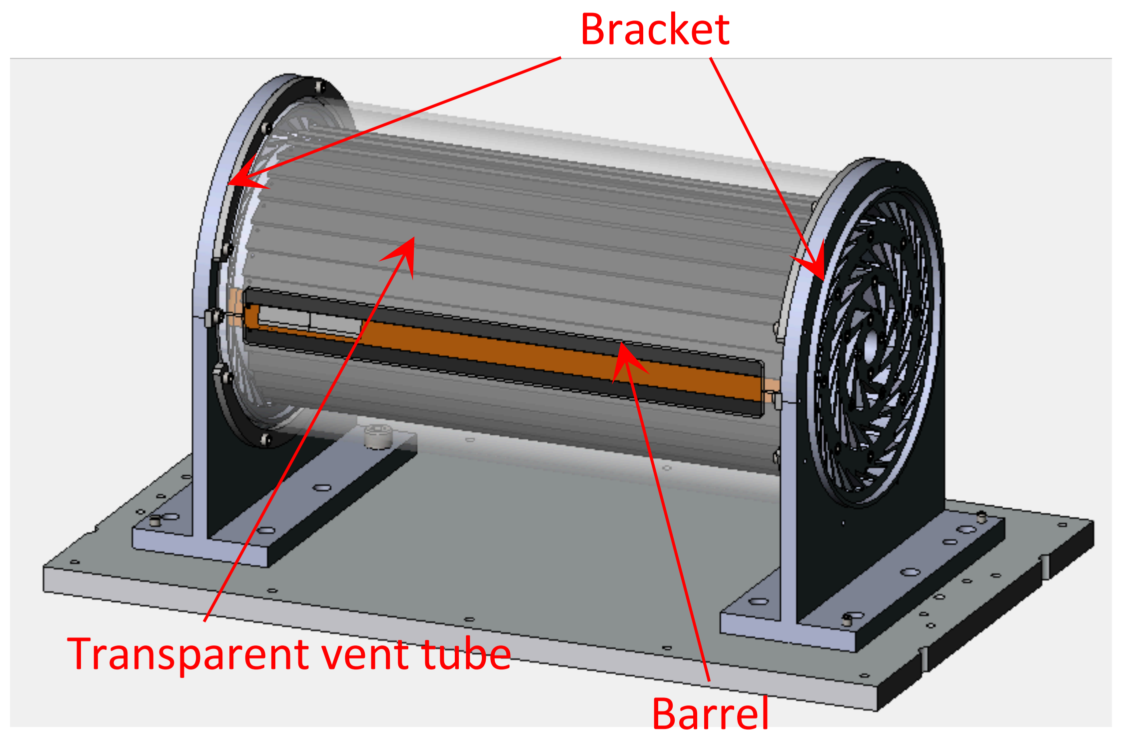
2. The endcap was under installation



3. The transparent cover is used to protect the prototype

4. The full prototype setup was tested at IHEP before beam test

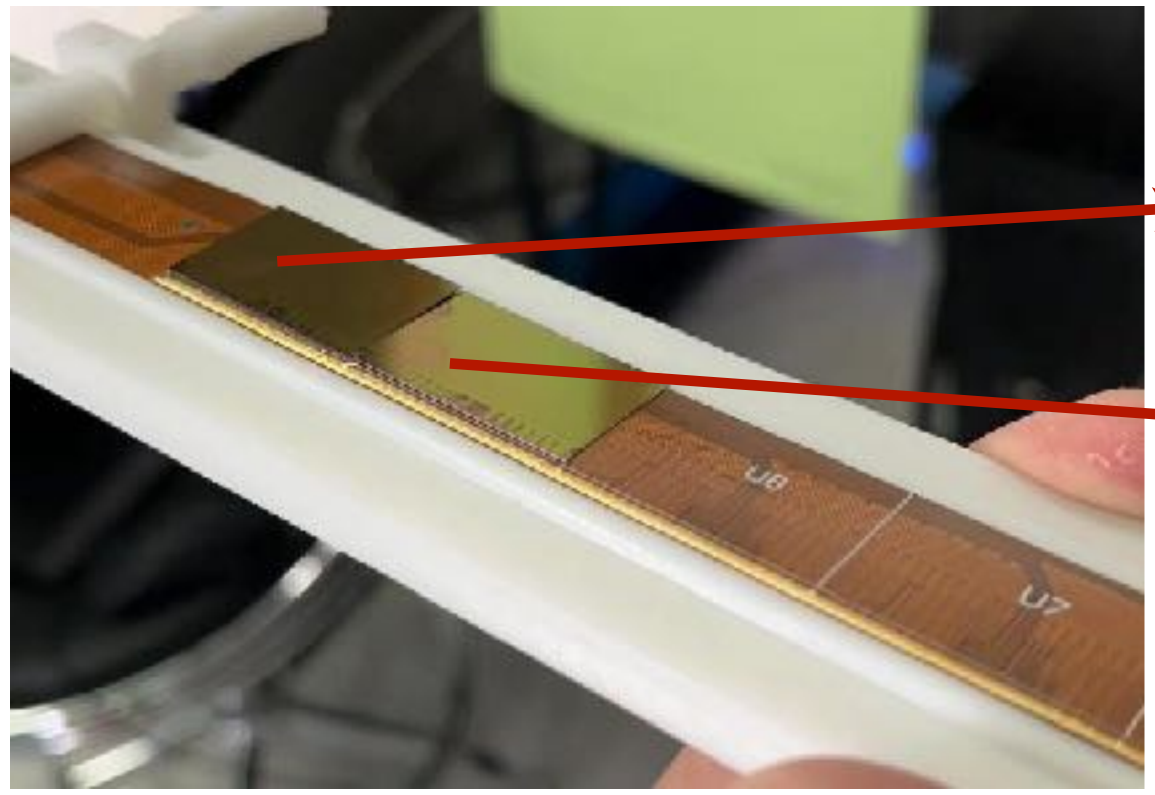
- The mechanical structure size of prototype is same with the CDR design
- More details about the mechanical structure can be found in this paper.



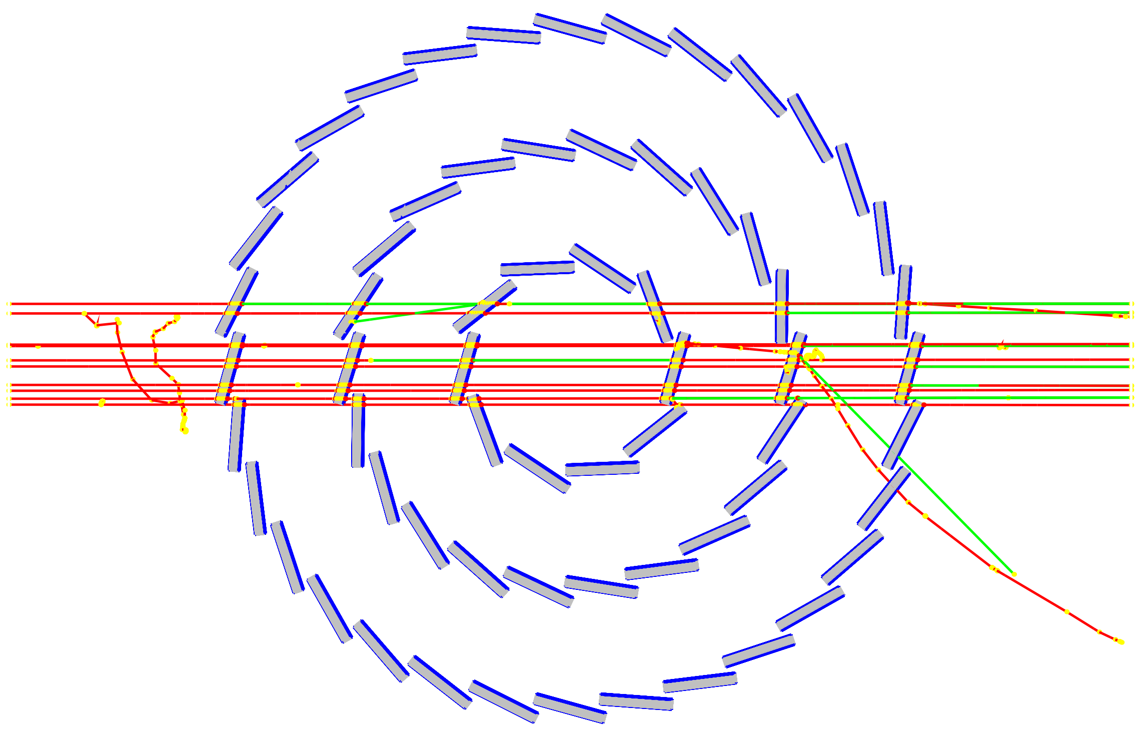
Beam test on prototype @ DESY II

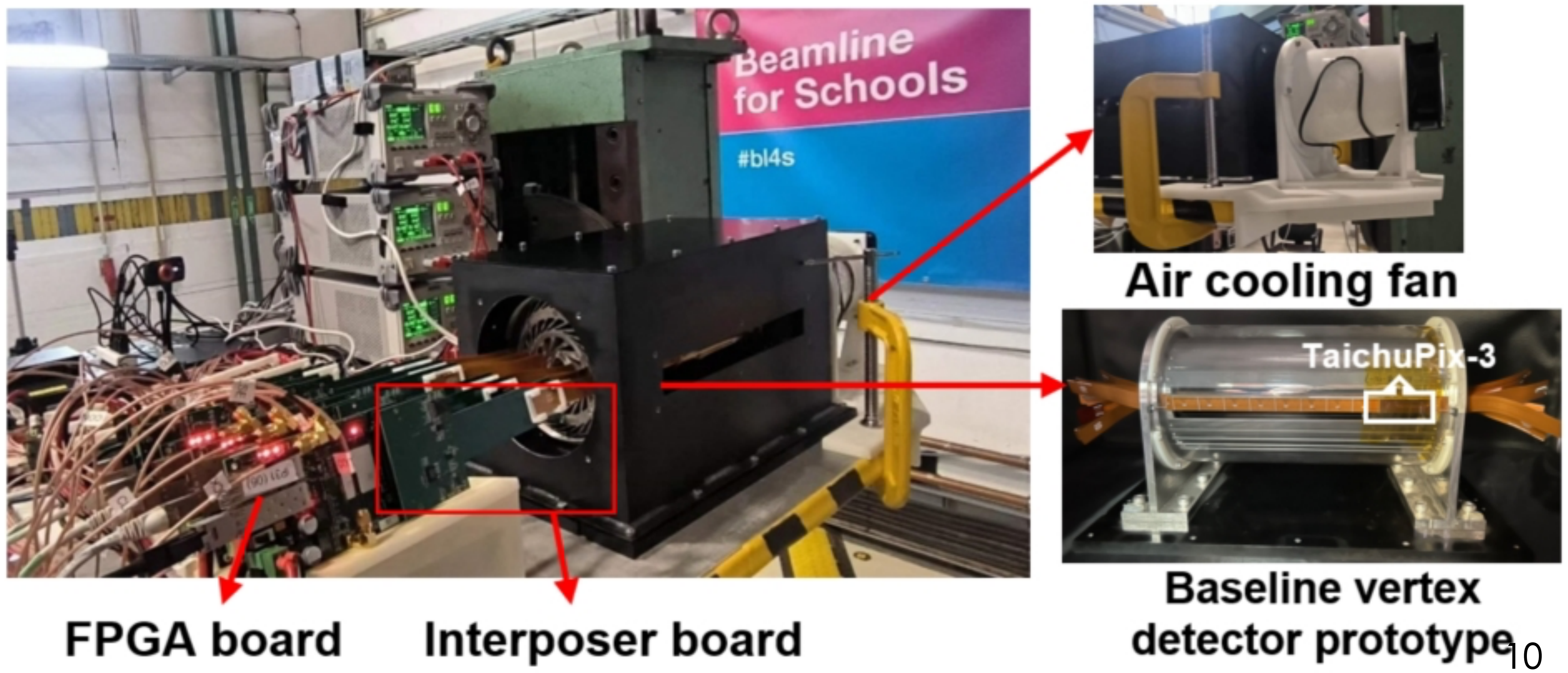
➡ Setup

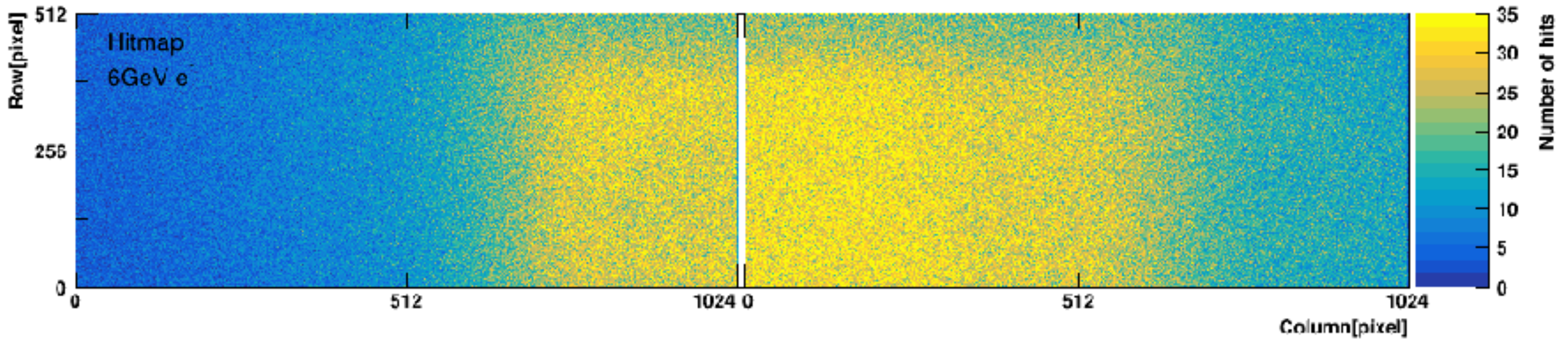
- Six ladders with 2 TaichuPix-3 chips on each side (total 24 chips installed)
- The biggest collimator available (2.5 cm x 2.5 cm) was used to focus on the two chips on the prototype
- 4-6 GeV electron beam @ DESY II TB21
- Air cooling fan and dry ice used to cool down the prototype (40°C -> 28°C)



Two TaichuPix-3 chips on both sides of the ladder

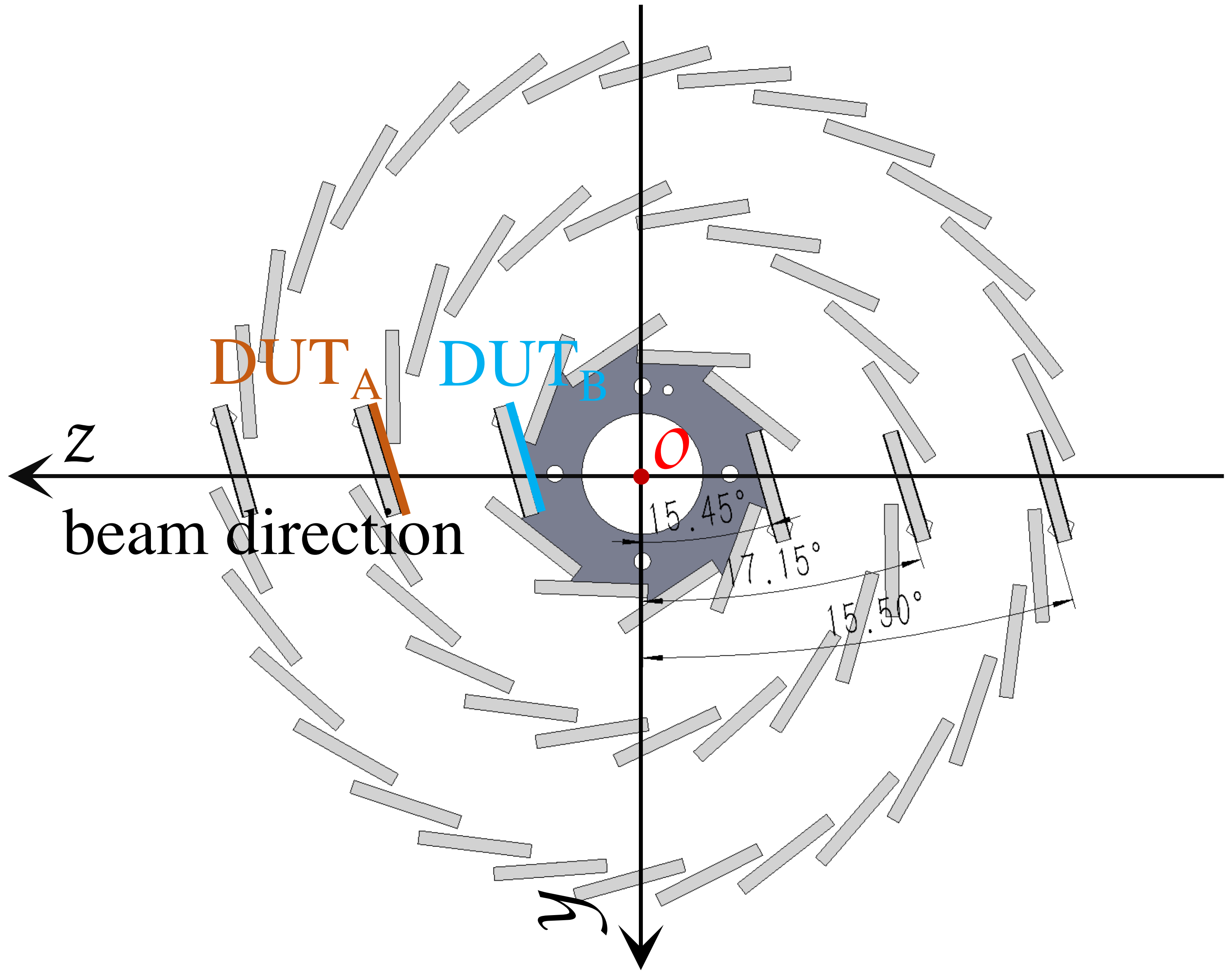






➡ Data analysis

- Analysis flow
  - Tracks reconstructed from the hit information on TaichuPix-3
  - Two DUTs with different process
  - ladder tilt angle (15.5°, 17.15°, 15.45°)
  - ladder diameter (~ 59.9 mm, 36.6 mm, 18.1 mm)

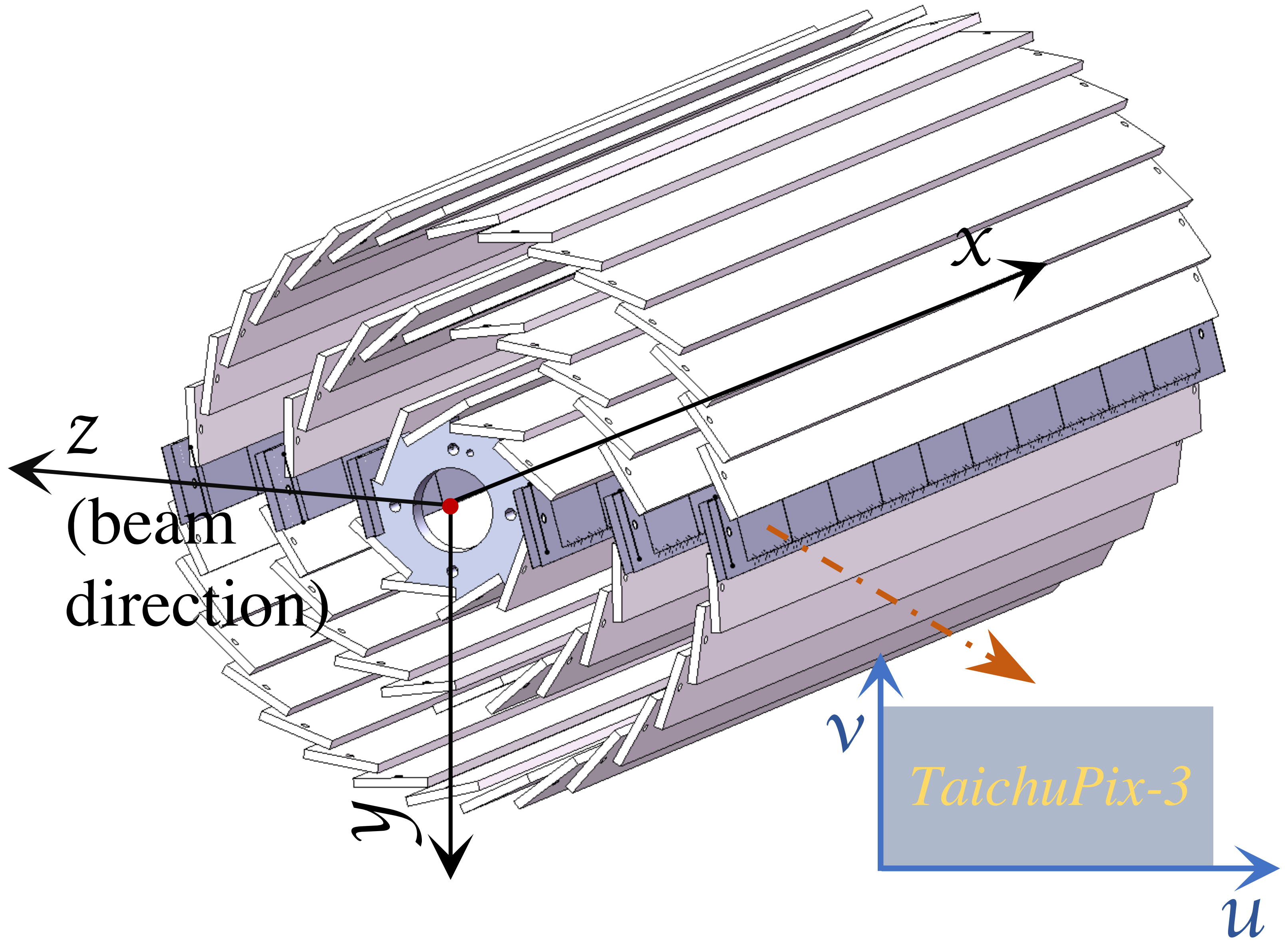


Raw Data → Decoding → Event building → Clustering → Track finding → Alignment → Track fitting

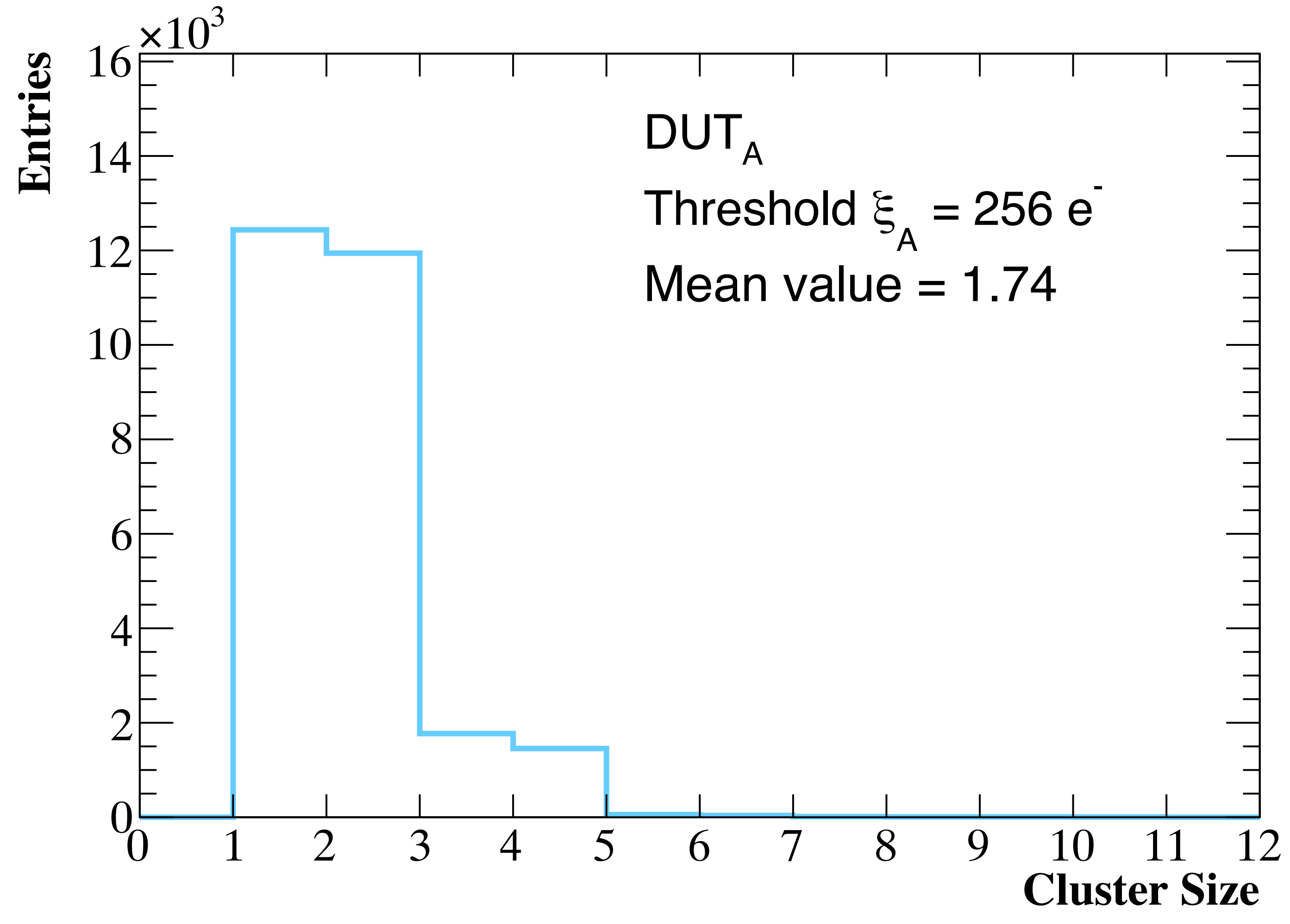
timeStamp_FPGA coincidence (→ Event building)

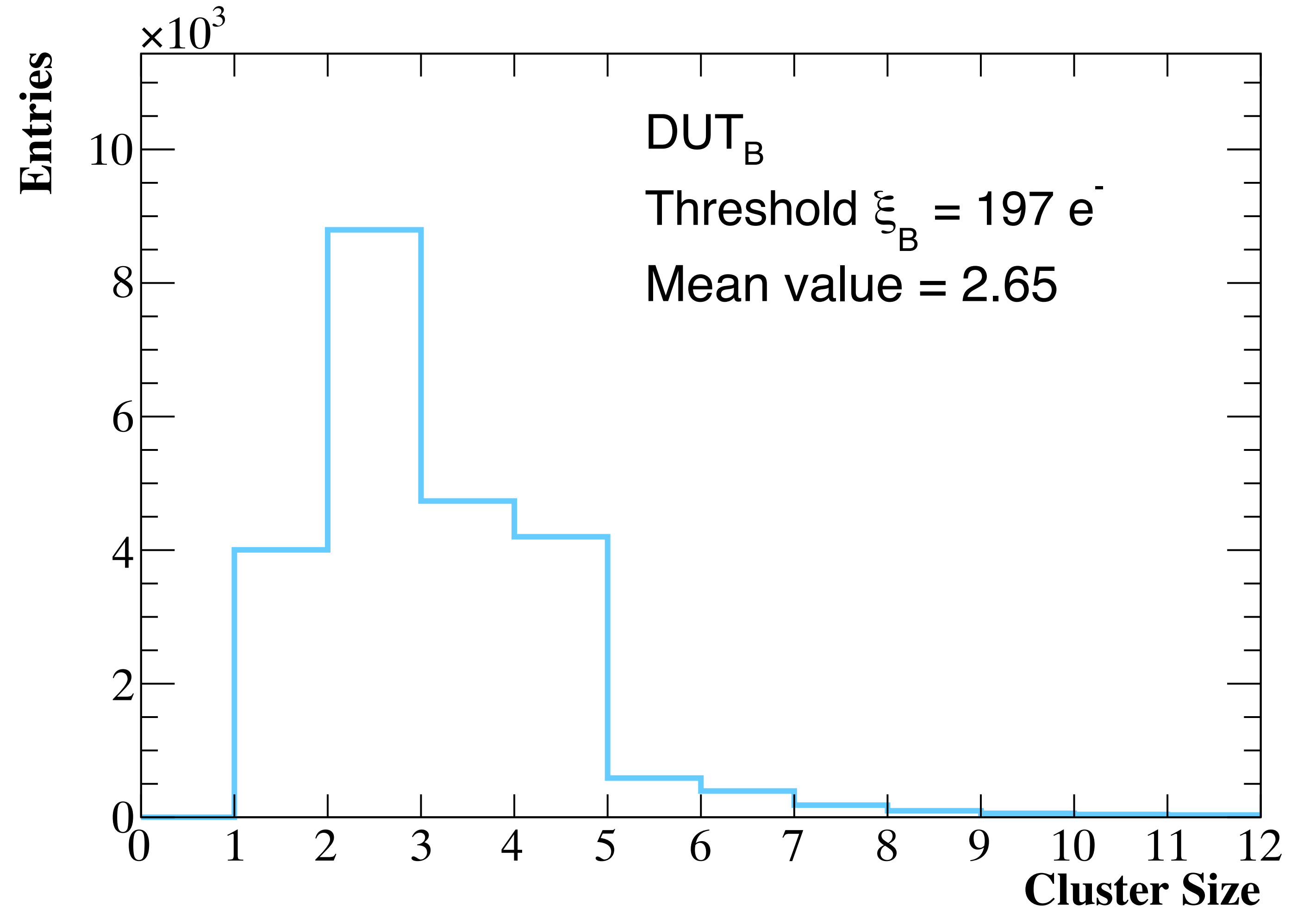
MILLEPEDE (→ Alignment)

Track fitting: Straight line fit; General broken line fit

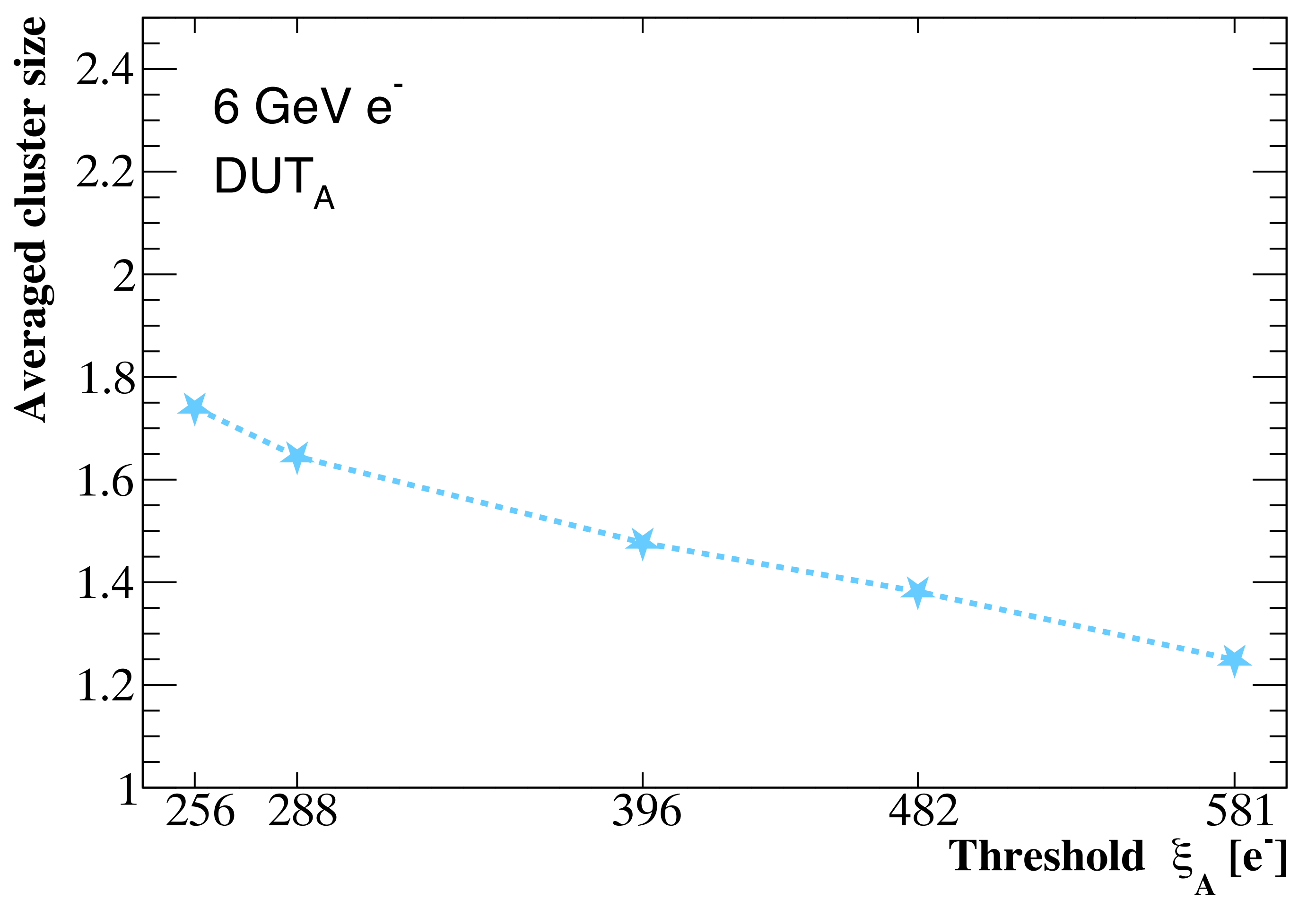


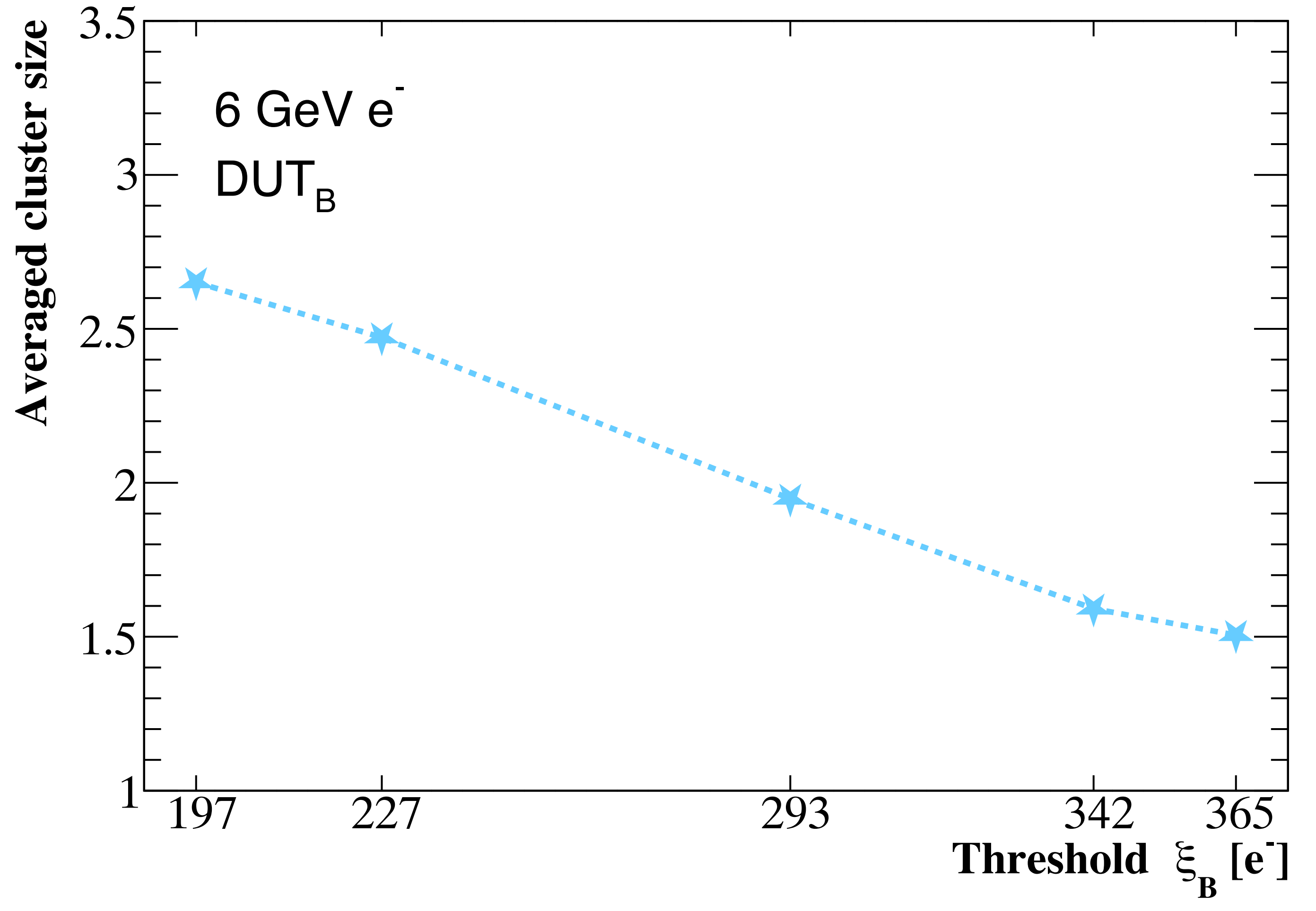
- Cluster Size





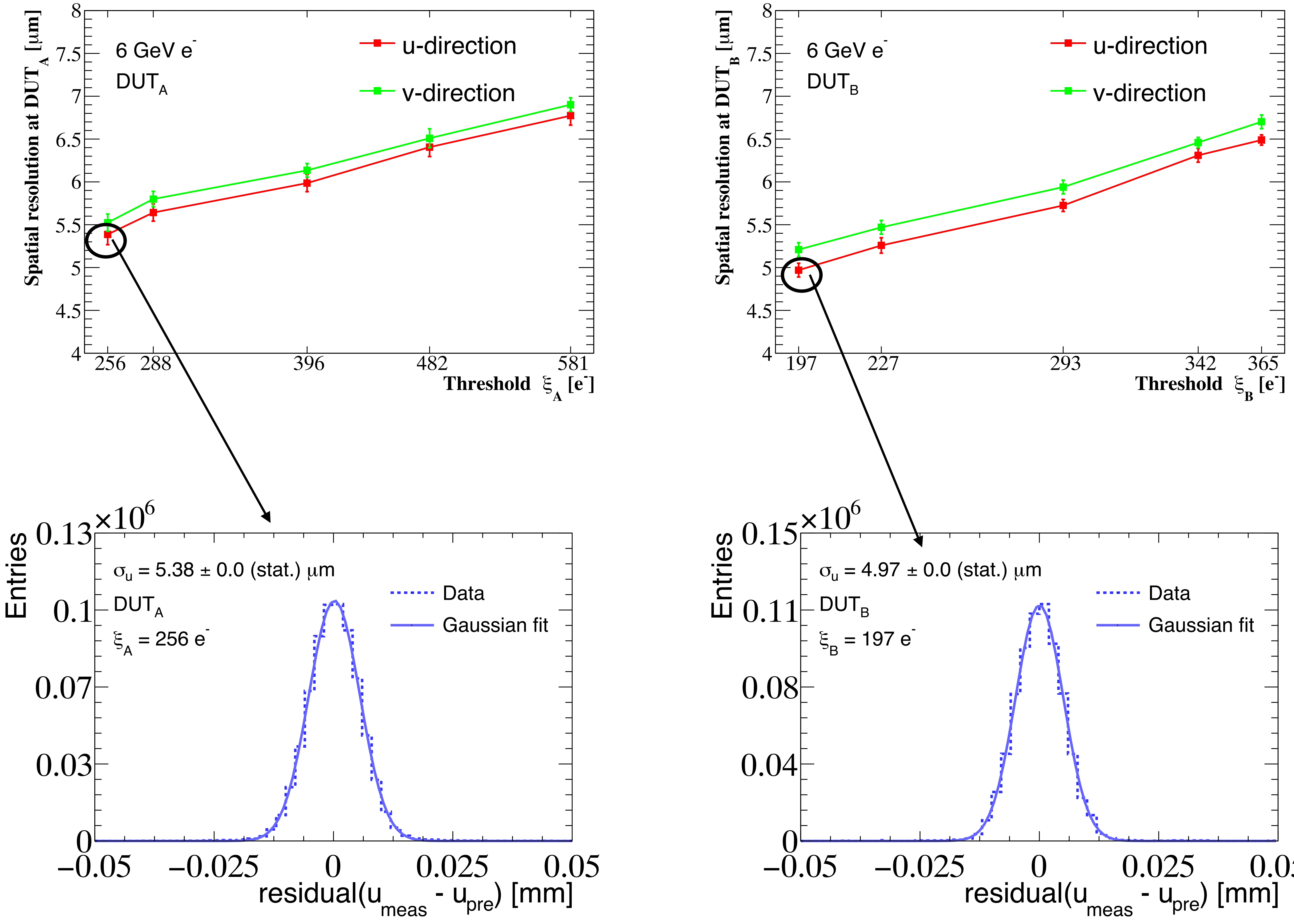
- The centre of the cluster is the geometric centre (binary readout)
- The maximum averaged cluster size is 1.74 pixels for DUTA, 2.56 pixels for DUTB





- Averaged cluster size decreases with threshold increases

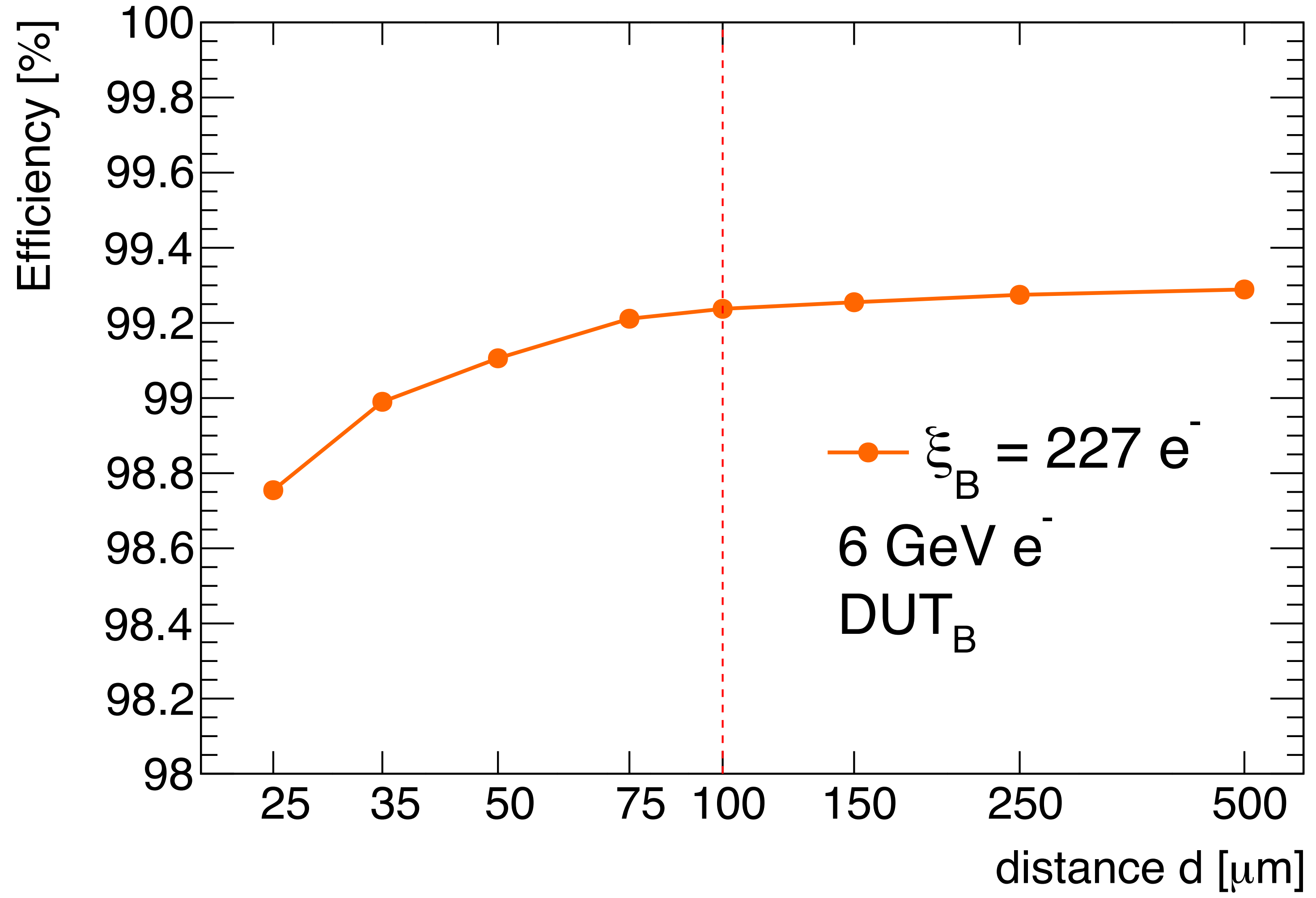
- Spatial resolution



- The width of unbiased residual distribution fitted with Gaussian function
- Spatial resolution deteriorates as threshold increases
- Systematic uncertainties source:
  - 11 % scattering angle predicted by Highland formula;
  - 5% beam energy dispersion

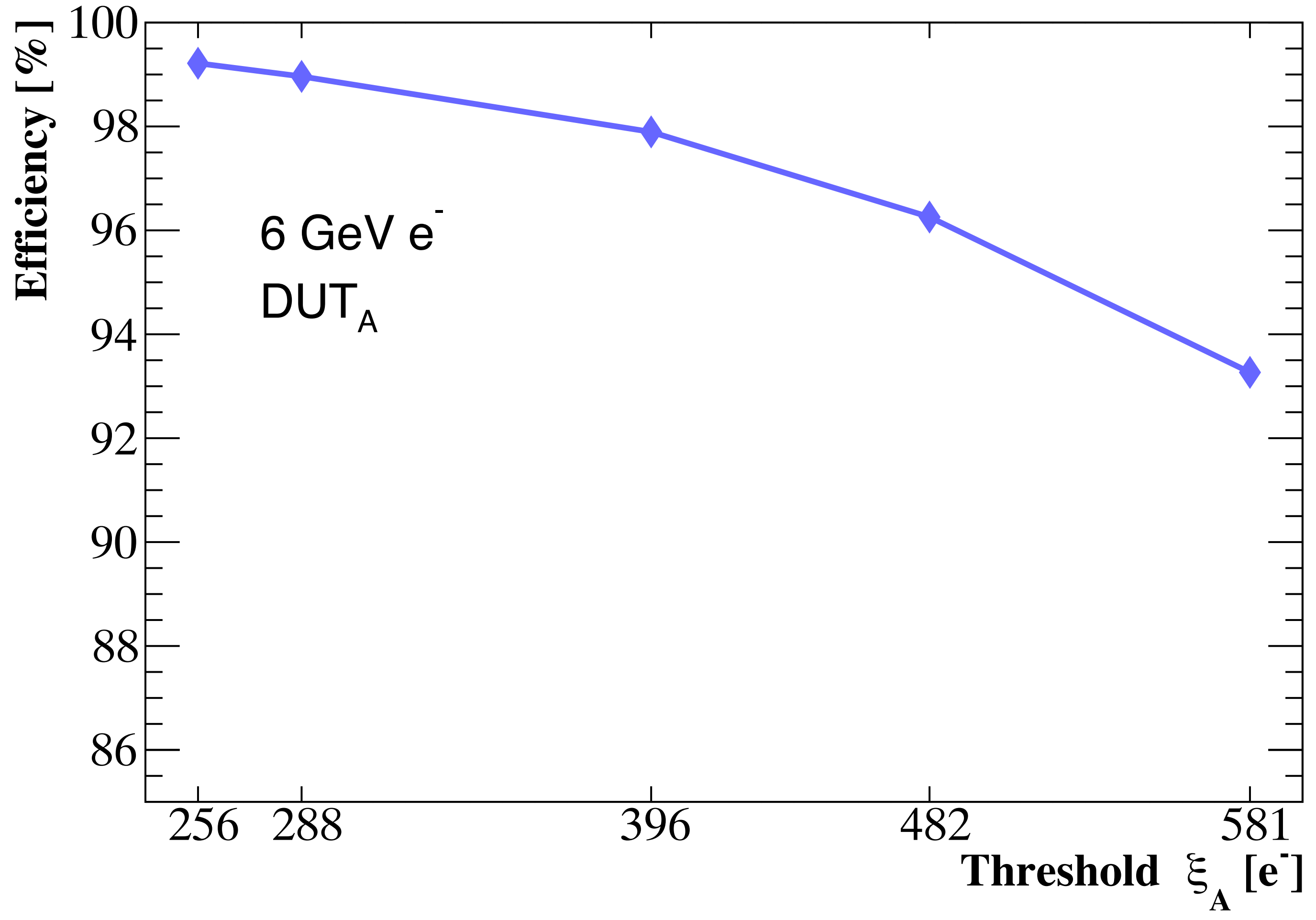
- Detection efficiency
  - Efficiency definition

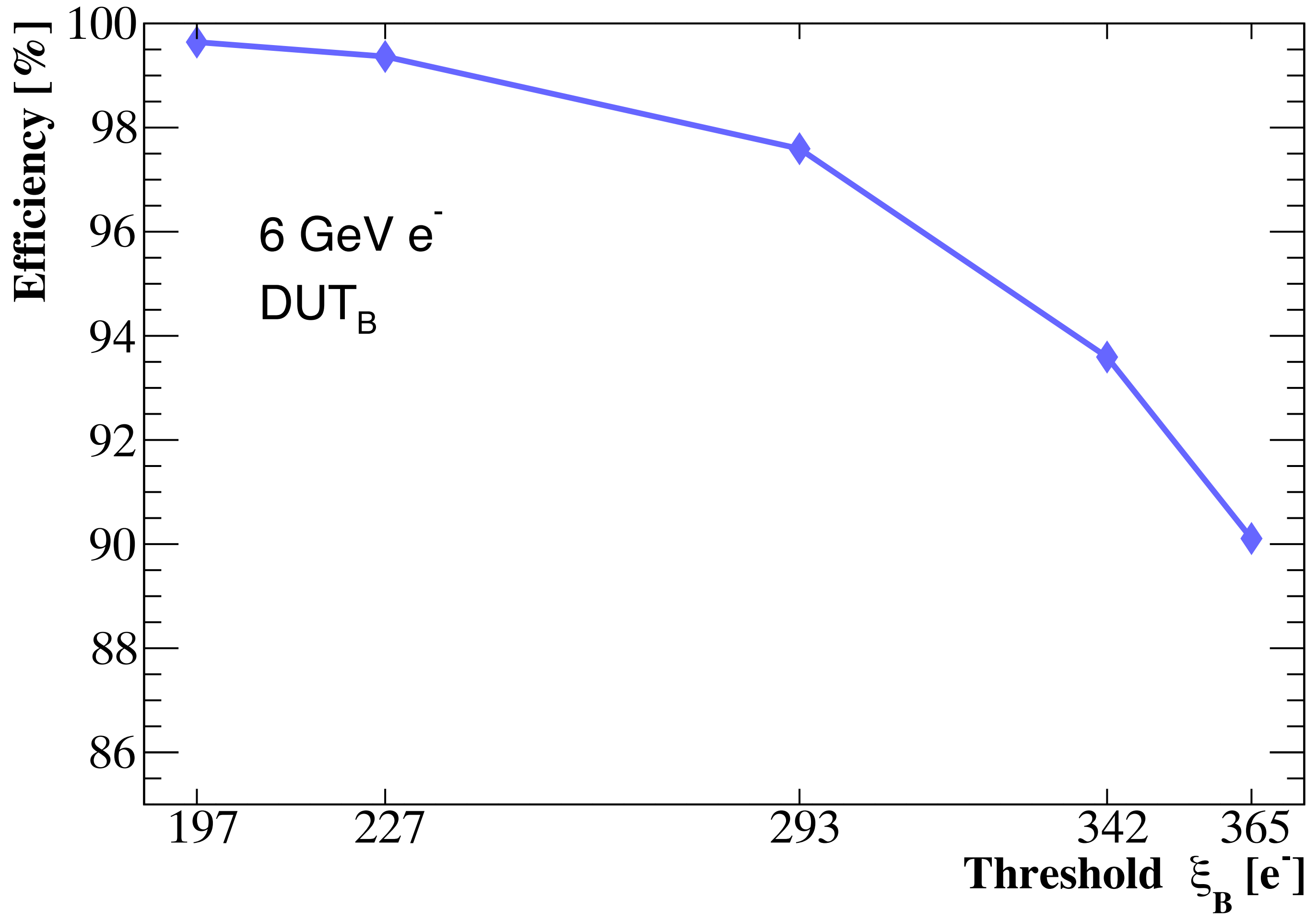
$$Eff. = \frac{N^{matched\ tracks}_{|x_{meas},y_{meas}-x_{pre},y_{pre}|<d}}{N^{tracks}_{all}}$$



- When d = 100 μm, the efficiency saturates

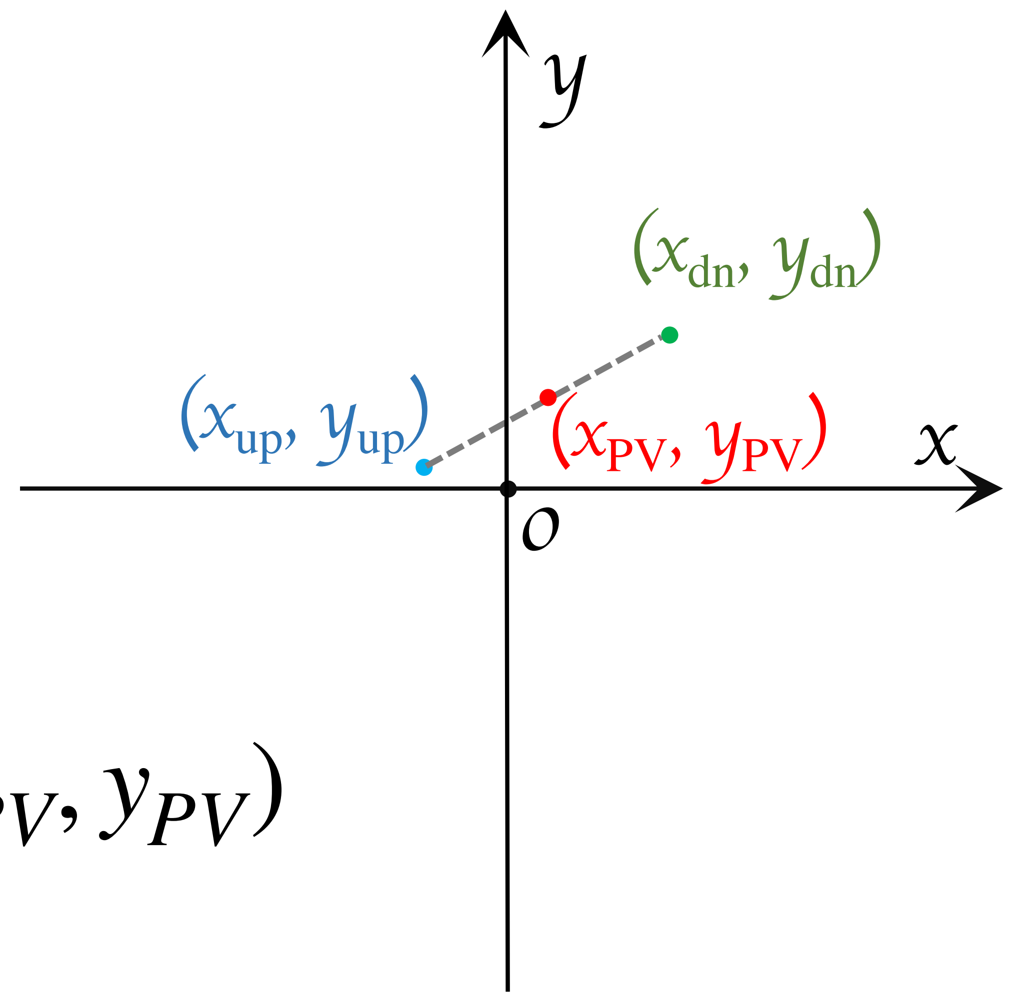
  - d is chosen to be 100 um to reject badly reconstructed tracks
  - The efficiency can be larger than 99 % for both processes

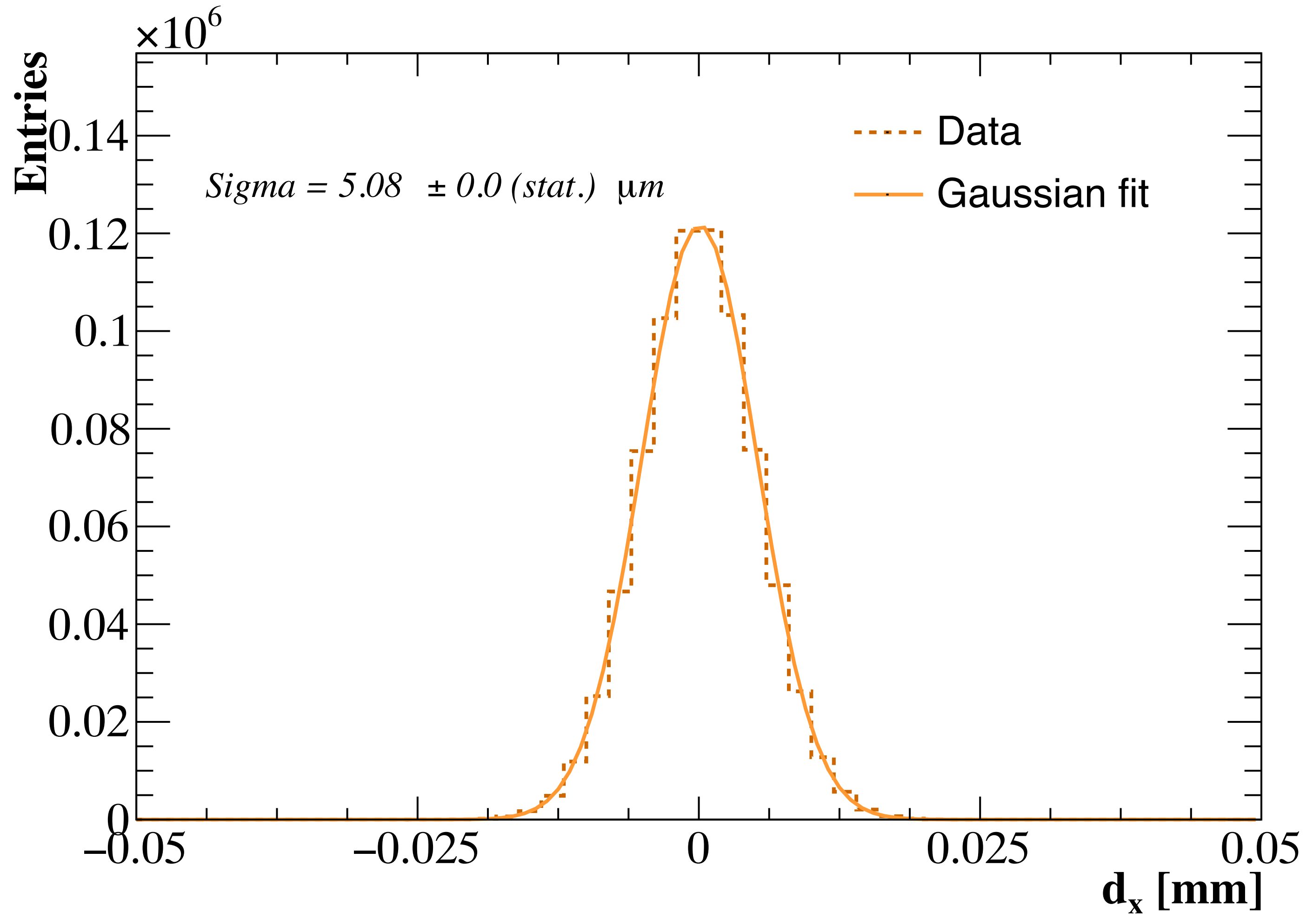


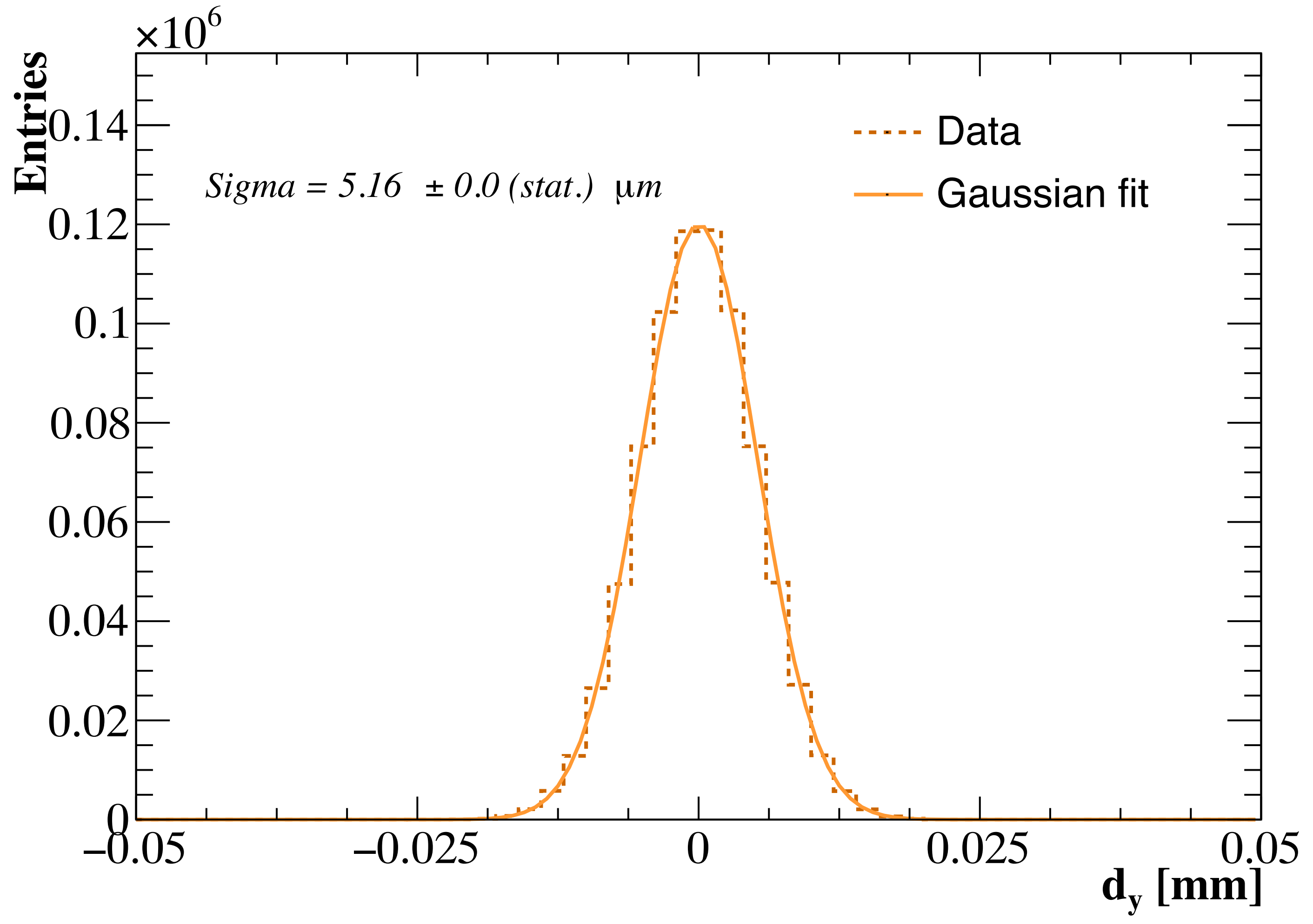


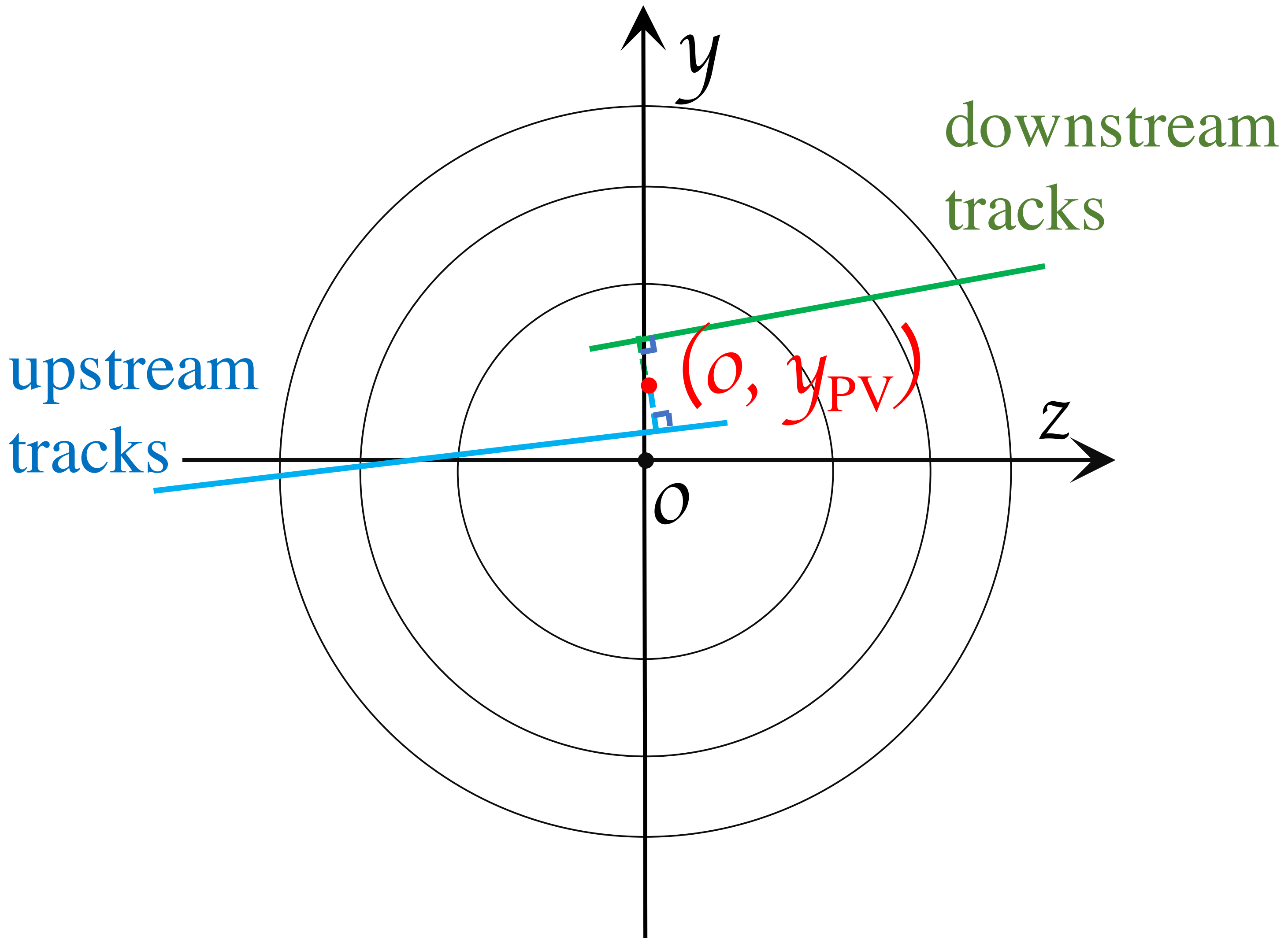
- Impact parameter

  - Definition: perpendicular distance between the track and the primary vertex (PV)
  - Split the tracks into upstream tracks and downstream tracks
  - Assumed PV (x_{PV}, y_{PV}) : the middle point of (x_{up}, y_{up}) and (x_{dn}, y_{dn})
  - (x_{up}, y_{up}) and (x_{dn}, y_{dn}) are the tracks intersection point with $z = 0$ plane
  - Impact parameter $d_{x,y}$ are the distance between up/downstream tracks and (x_{PV}, y_{PV})
    - The widths of $d_{x,y}$ are the impact parameter resolution, ~5.1 μm









➡ Conclusion

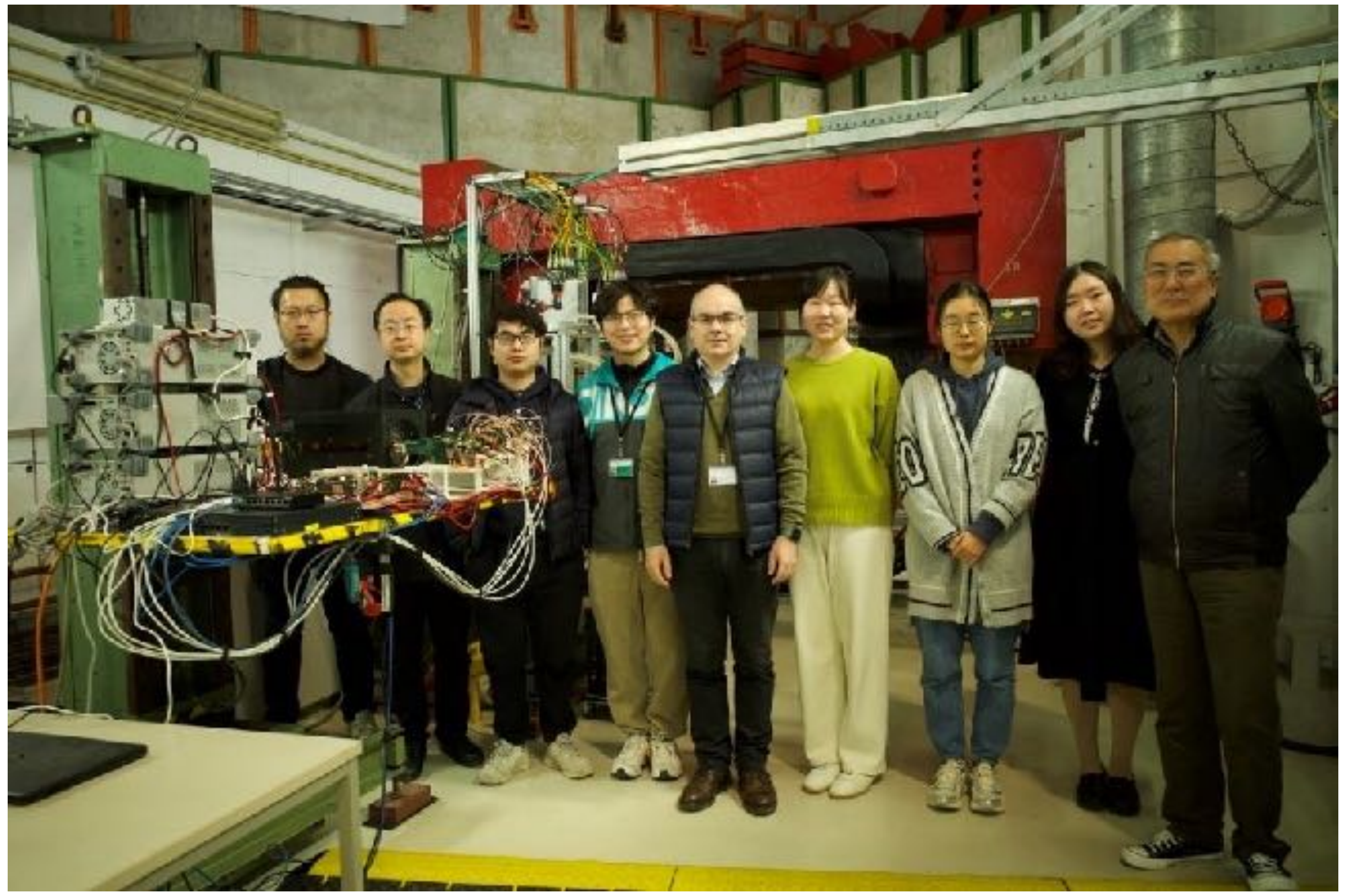
- CEPC vertex team developed the first vertex prototype for CEPC
- The prototype was characterised by a 6 GeV electron beam provided by DESY
  - Spatial resolution: ~ 5 μm
  - Detection efficiency: > 99 %
  - Impact resolution: ~ 5.1 μm
- Upcoming CEPC TDR will propose new optimized vertex detector design based on the accelerator part of TDR (mechanical structure, silicon pixel sensors, reconstruction and analysis software...)

CEPC Vertex detector team

- IHEP, CAS, China: João Guimarães da Costa, Wei Wei, Zhijun Liang, Ying Zhang, Tianya Wu, Shuqi Li, Wei Wang, Jia Zhou, Ziyue Yan, Xinhui Huang, Hao Zeng, Xuewei Jia, Jun Hu, Jinyu Fu, Hongyu Zhang, Gang Li, Linghui Wu, Mingyi Dong, Xiaoting Li, Weiguo Lu, etc.
- Nanjing University: Ming Qi, Lei Zhang, Xiaoxu Zhang, Yiming Hu , etc.
- Northwestern Polytechnical University: Xiaomin Wei, Jia Wang, Ran Zheng, etc.
- Shandong University: Liang Zhang, Jianing Dong , etc.
- IFAE, Barcelona, Spain: Sebastian Grinstein, Raimon Casanova , etc.

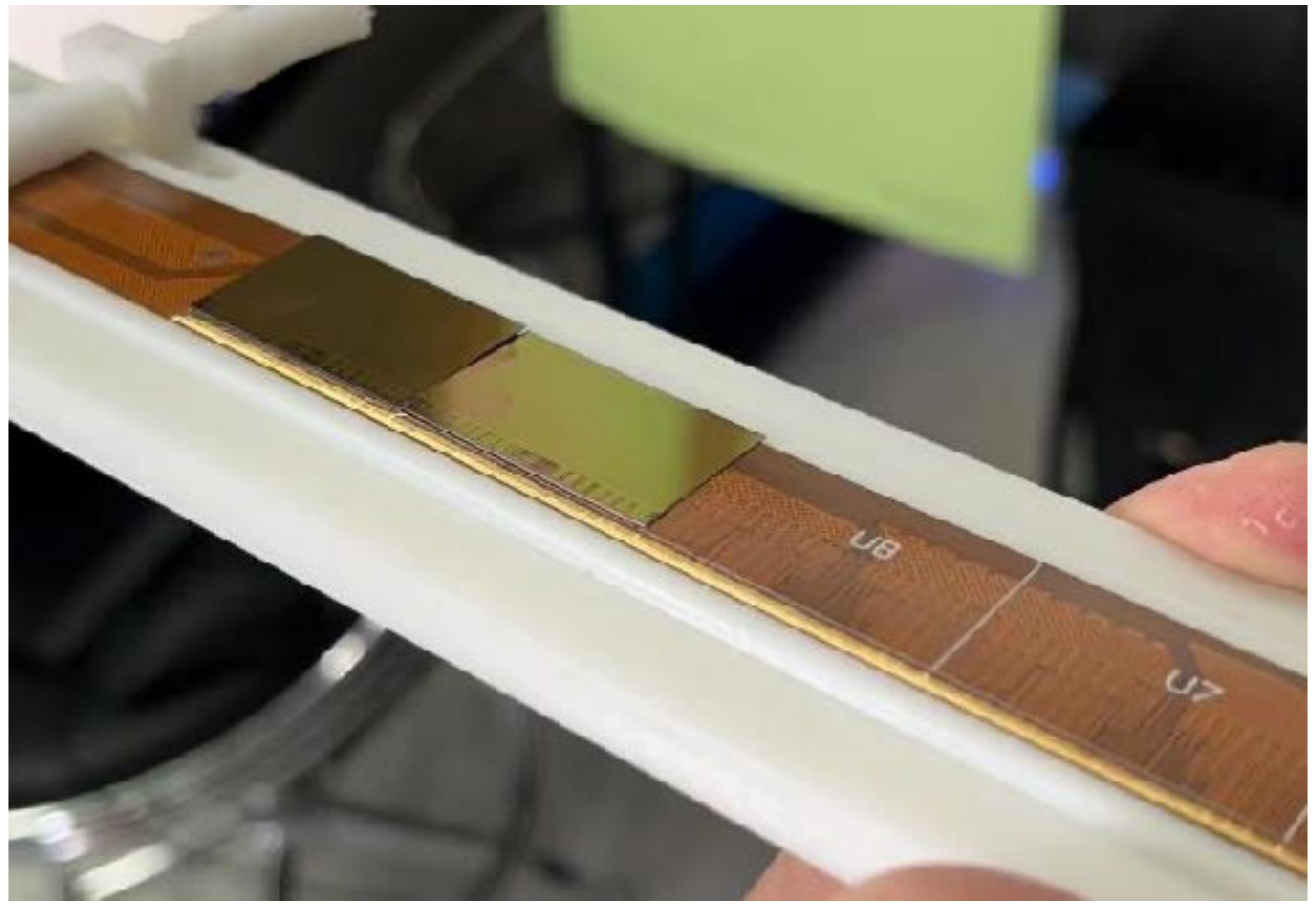
2022.12 @ DESY II TB21 for TaichuPix-3 telescope level tests

2023.04 @ DESY II TB21 for prototype level tests



Thanks for DESY providing for the excellent beam !

Backup



Two TaichuPix-3 chips are glued onto one end of the ladder due to the size of the collimator (2.5 cm x 2.5 cm) at DESY beam line

➡ Readout electronics and DAQ

- Interposer board:
  - transmit data from fired pixels and control signals between the ladder and the FPGA boards
  - supply DC voltage to the ladders
- FPGA board:
  - clock controller port
  - global configuration port
  - timestamp synchronisation port
- DAQ:
  - real-time sampling output to monitor the status
  - data rate: 18 Mb/s during beam test