

MAPS in a 65 nm CMOS imaging technology

• **MAPS** integrates the sensor and the readout electronics in the same wafer. Compared to hybrid detectors:

- Reduces complexity and production cost
- Smaller pixel sizes are achievable
- Reduces material budget

MAPS with a small collection electrode results in small sensor capacitance and a large S/N.

✓ Good tracking resolution (~ 3μ m) ✓ Small power consumption (~ 50 mW/cm^2)

H2M (Hybrid-to-Monolithic)

- Ports a hybrid pixel detector architecture into a monolithic chip.
- **Digital-on-top** design workflow.
- Manufactured in a TPSCo 65 nm CMOS imaging process.



Good candidates for lepton, electron-ion colliders, and test beam telescopes

- Simulation-based process modifications and layout optimization enhance charge collection.
- From 180 nm to 65 nm CMOS Imaging Technology
 - ✓ Higher density of in-pixel logic
 - ✓ Smaller pixels or more complex in-pixel logic

Charge collection in thin ~ 10 µm) depleted p-epi layer Low-ohmic p-substrate A. Simancas

- 35 μ m pixel pitch in 64x16 pixel matrix (total sensitive area: 2.24 × 0.56 mm²).
- Non-simultaneous **acquisition modes**, per pixel: 8 bit <u>ToT</u> resolution, 8 bit <u>ToA</u> resolution (100 MHz clock - 10 ns timing), photon counting, and triggered.
- **Readout**: 40 MHz clock, frame-based without zero-suppression.



Testbeam measurements

Sketch of the readout scheme at SPS

Sketch of the test beam setup at DESY II AIDA TLU

Laser measurements

Backside incidence with an infrared pulsed laser.



- Observed expected efficiency and fake-hit rate dependence on threshold (THL), but :
- Significant **noise** contribution below \sim 320 electrons, combination of noise level and long acquisition time.
- **In-pixel efficiency indicates charge loss**, not predicted by simulations using generic doping profiles.

V_{bias} = - 1.2 V, THL ≈ 520 e⁻

V_{bias} = - 3.6 V, THL ≈ 520 e⁻

 \star Collection electrode V_{bias} = - 3.6 V, THL ≈ 400 e⁻

___10

0.9

Efficier

0.6

0.5

- Confirmation of in-pixel efficiency pattern observed in test beam measurements.
- **Pixel-to-pixel differences** attributed to differences in the circuit's Krummenacher current and feedback capacitance.





- Pattern qualitatively reproduced in simulations using proprietary doping profiles, related to the size and location of the n-wells of the analog circuitry.
- Mitigated at larger V_{bias} and lower thresholds.





- Summary
- Fully functional advanced digital-on-top sensor in a 65 nm CIS.
- Successfully integrated into the **Caribou DAQ**.
- Non-uniform in-pixel efficiency observed in testbeam.
 - Qualitatively confirmed by simulations and laser measurements.
- Combined effect of fast front-end, low V_{bias}, large pixel size, and threshold.
- Investigating reducing the noise and lowest threshold achievable using the triggered acquisition mode.
- Studying **new chip operational parameters** for a more stable operation of the CSA with Krummenacher feedback and smaller pixel-to-pixel differences.
- Threshold and ToT calibration per pixel to physical units for direct comparison to simulations.

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