Experience and First Results of the HGCAL Beam Tests in 2023

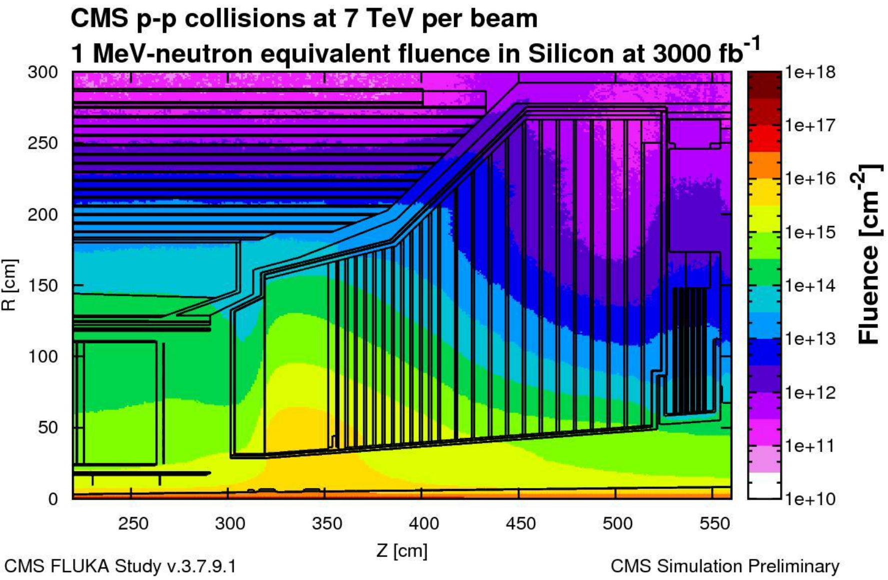
Geliang Liu on behalf of the CMS Collaboration

Apr. 17th 2024, 12th Beam Telescopes and Test Beams Workshop

Outlines

- The silicon module and electronics at the HGCAL
- The beam test setup in 2023
  - The full electronics chain is tested with beams for the first time !!!
- First results from the beam test data

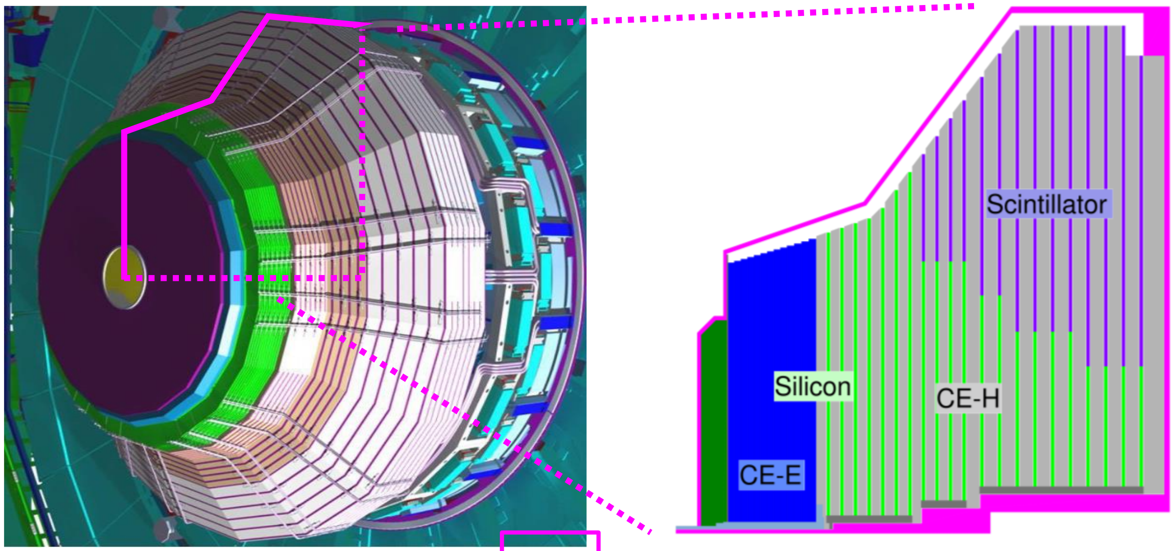
The HGCAL and the silicon module



Challenges during the **High Luminosity Large Hadron Collider (HL-LHC)**

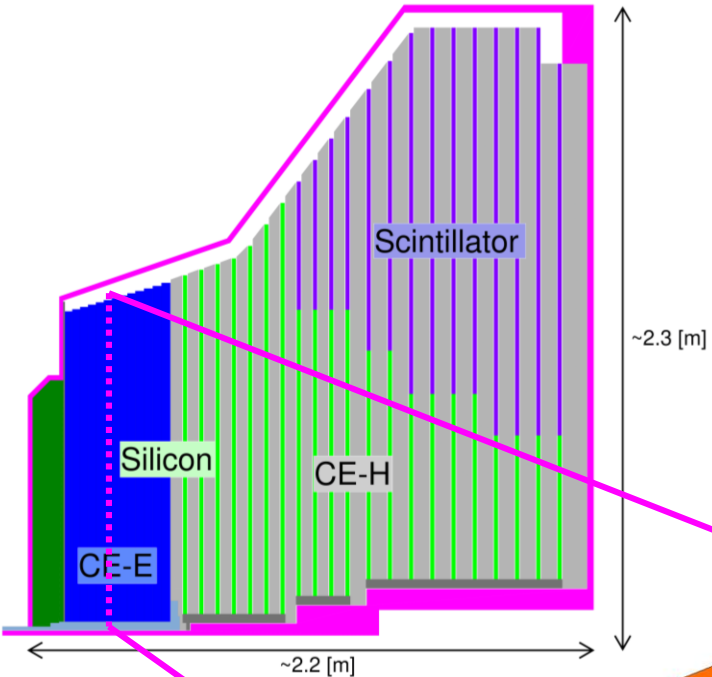
- High irradiation
- High pileup

As part of the phase-II upgrade of the CMS detector, **the High Granularity Calorimeter (HGCAL)** will replace the existing endcap calorimeters



×2

The HGCAL and the silicon module

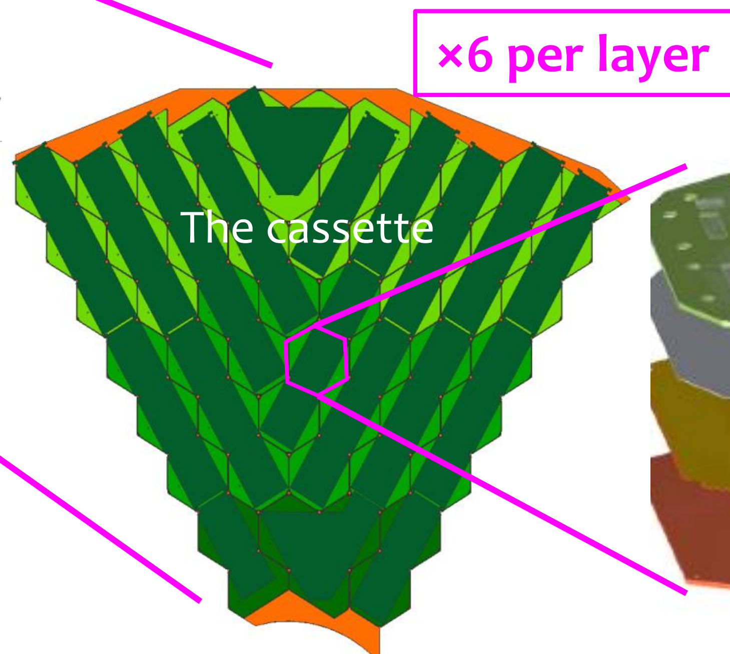


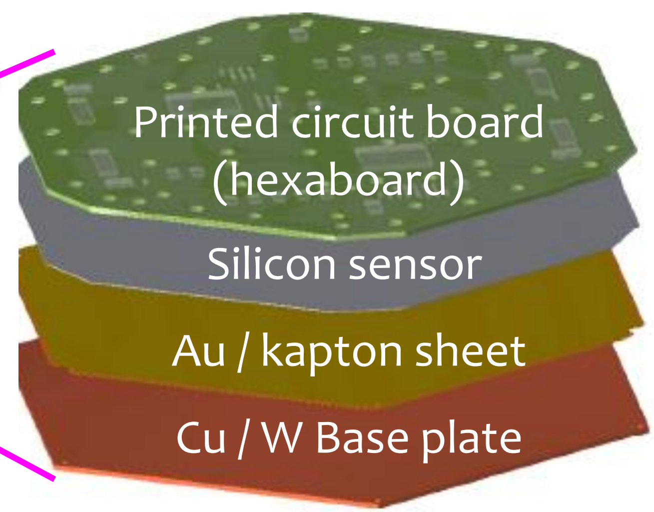
Structures of the HGCAL:

- Silicon modules in the electromagnetic section (**CE-E**).
- Mixture of silicon modules and scintillator tile-modules in the hadronic section (**CE-H**).

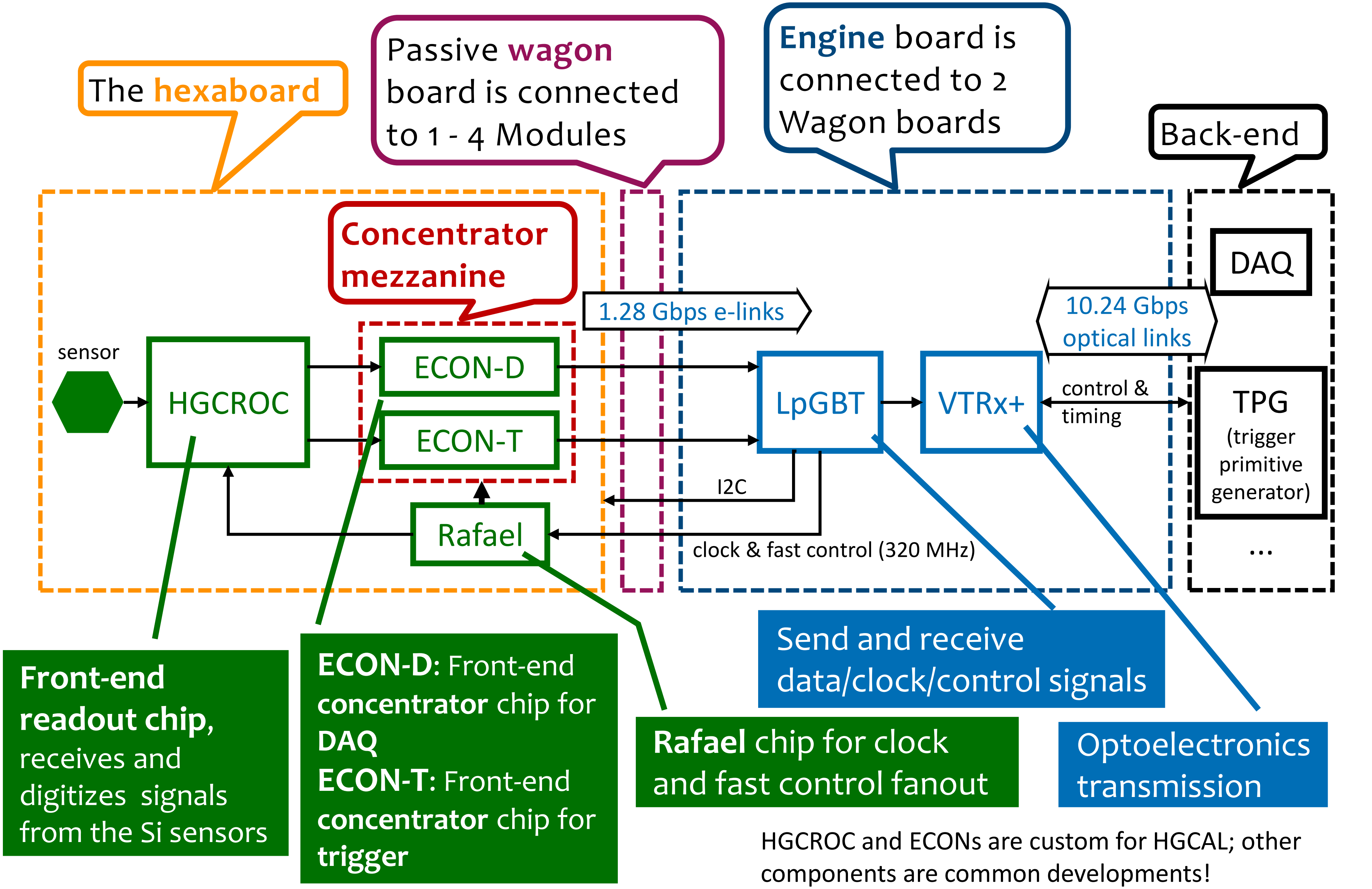
Features of the HGCAL:

- **Large coverage**: 1.5 < |η| < 3.0
- **5D information**: space-time-energy
- **High granularity**: 6M channels in silicon region, 270K channels in scintillator region

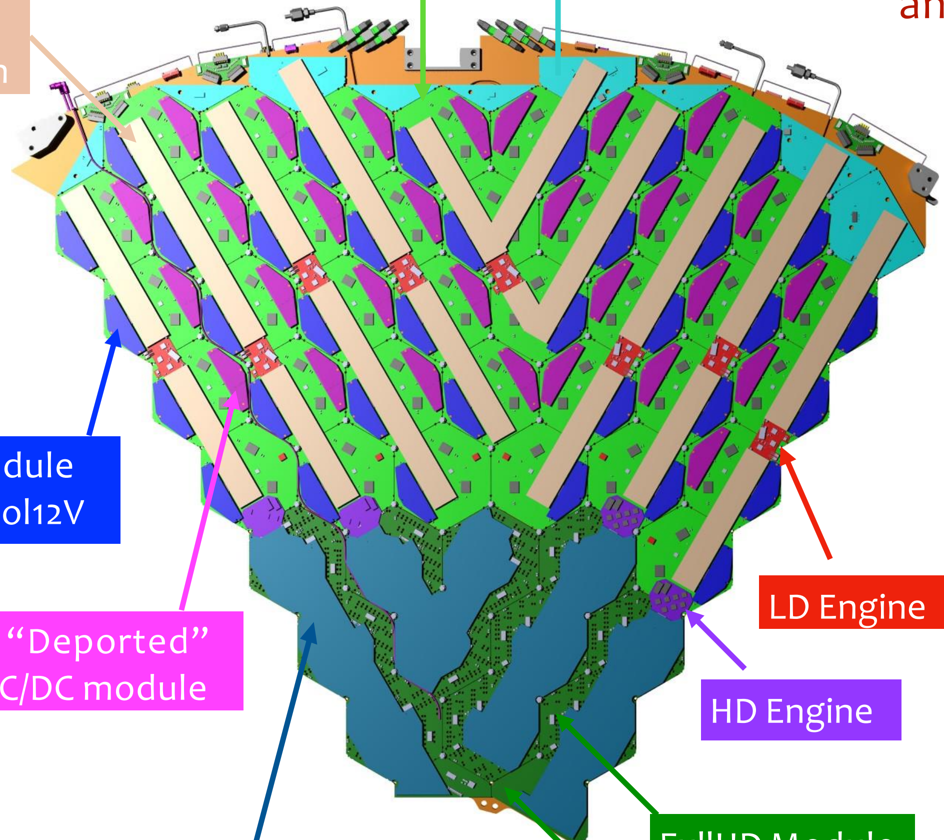




The electronics architecture of the silicon section



The modular implementation [presentation by N. Strobbe]



Note: each layer is different! Occupancies vary greatly within and between layers

Low density (LD) region
- Si sensor 200 or 300 µm thickness
- 192 channels (3 HGCROCs) per full 8" hexagonal module

High density (HD) region
- Si sensor 120 µm active thickness
- 432 channels (6 HGCROCs) per full 8" hexagonal module

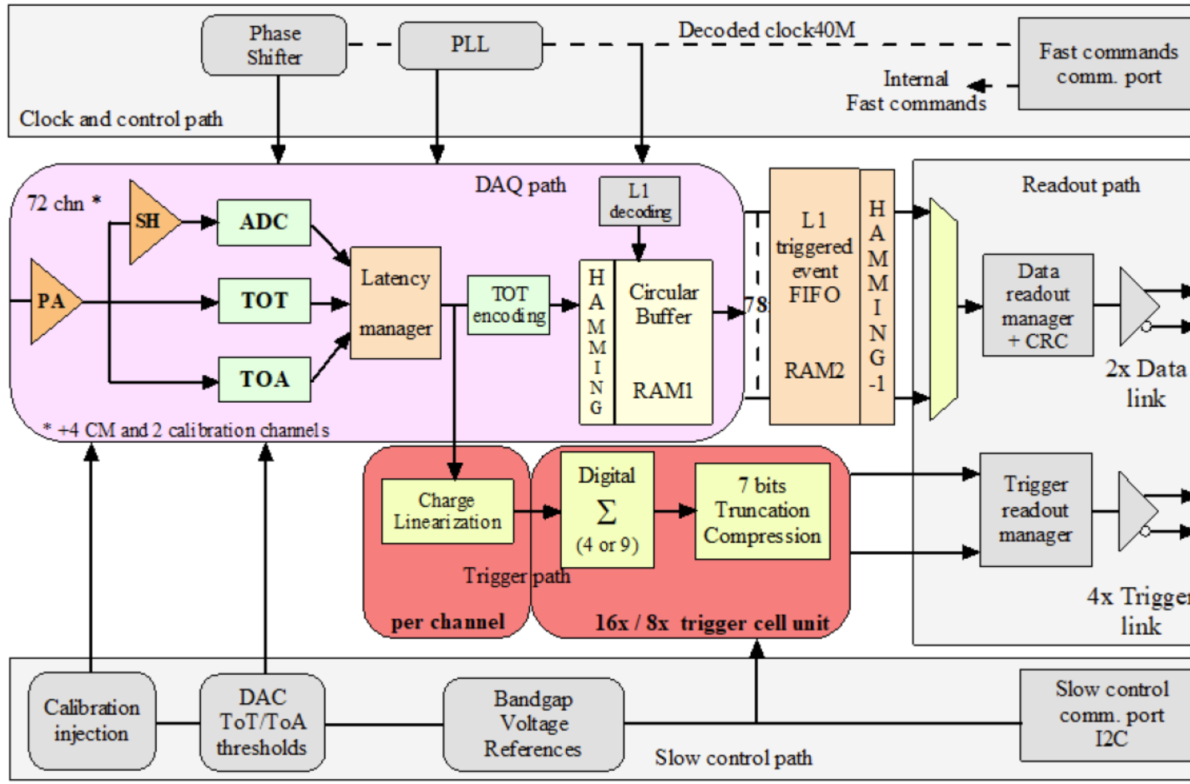
The HGCROC at the HGCAL

HGCROC(v3) as the front-end readout ASIC on the hexaboards

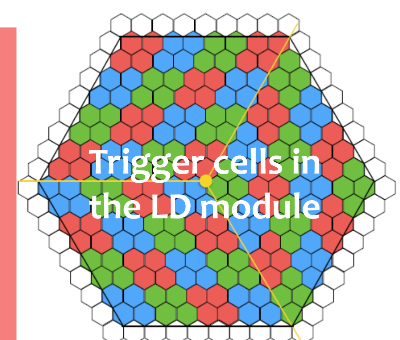
- 40 MHz clock in phase with the 25ns bunching crossing (BX) at the HL-LHC

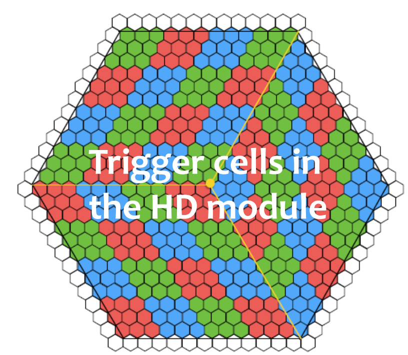
Two data paths: DAQ & trigger

- Charge measurement:
  - **ADC** (analog-digital-converter) count at low charge
  - **TOT** (time-over-threshold) at high charge
- Time measurement:
  - **TOA** (time-of-arrival)
- Two DAQ 1.28 Gbps CLPS output links



- Compressed data of the charge @ 40 MHz for **L1 trigger**.
  - **Charge linearisation** over ADC / TOT range
  - **Reduced granularity**: 48 trigger cells per module
  - **Charge encoded** in 7 bits for bandwidth (4b exponent + 3b mantissa)
- Four trigger 1.28 Gbps output links



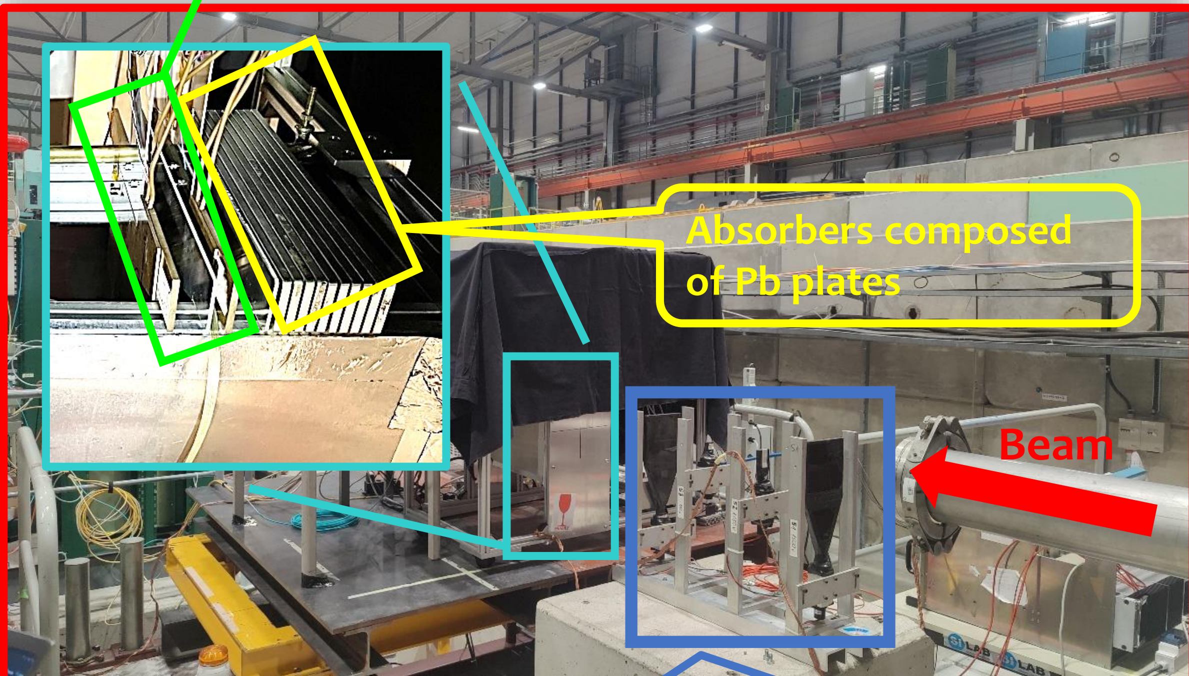


The HGCAL beam test 2023 at CERN

- At CERN Super Proton Synchrotron (SPS) H4 beamline.
- One week in August (2nd to 9th), two weeks in September (13th to 28th)

Setup

HGCAL prototype
- Modules on copper plates, working at bias voltage -270V



External trigger system based on multiple scintillators + PMTs: precision < 1 ns

Back-end DAQ, control

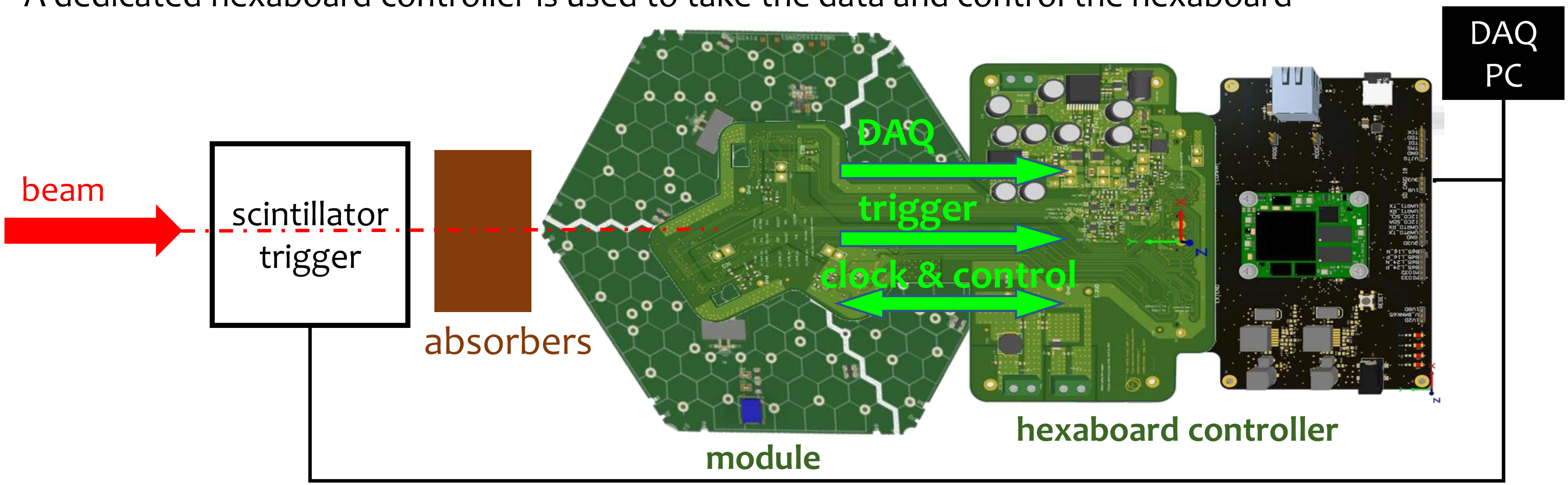
Two systems were tested:

- Single module tester (used in the 2021 and 2022 beam test)
- **The full electronics chain to be used in real life (FOR THE FIRST TIME !!!)**

Tested with electron, muon and pion beams

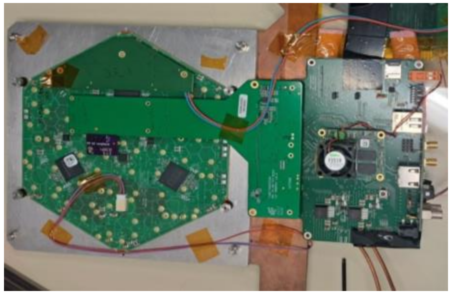
Single module test: setup

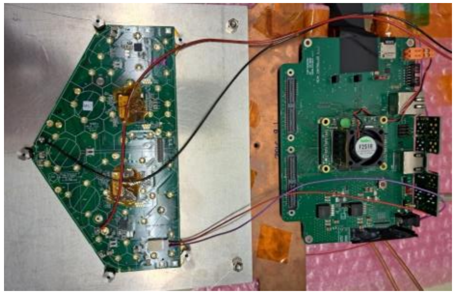
- 13th to 17th September
- HGCAL prototype composed of one single module
- A dedicated hexaboard controller is used to take the data and control the hexaboard



- Four modules of different types were tested

LD, full, 200 µm (sensor) | **HD, full, 120 µm** | **LD, semi-left, 300 µm** | **LD, semi-right, 300 µm**

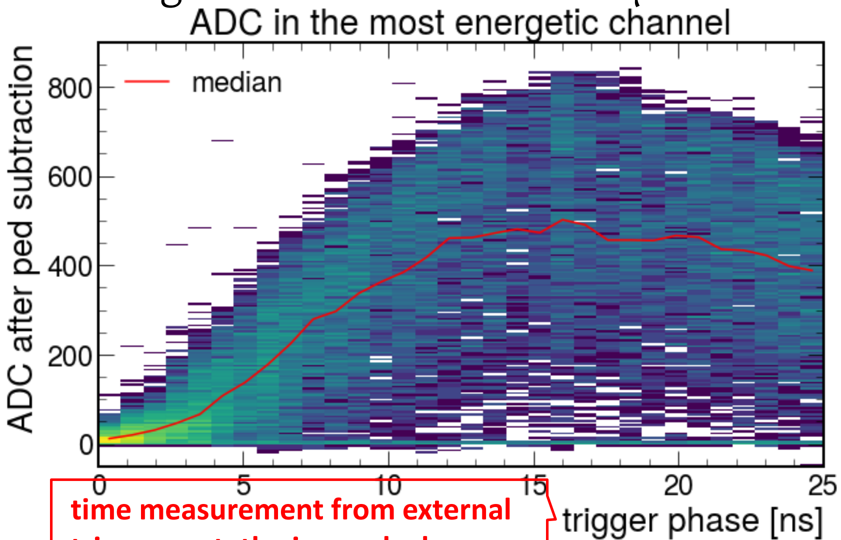


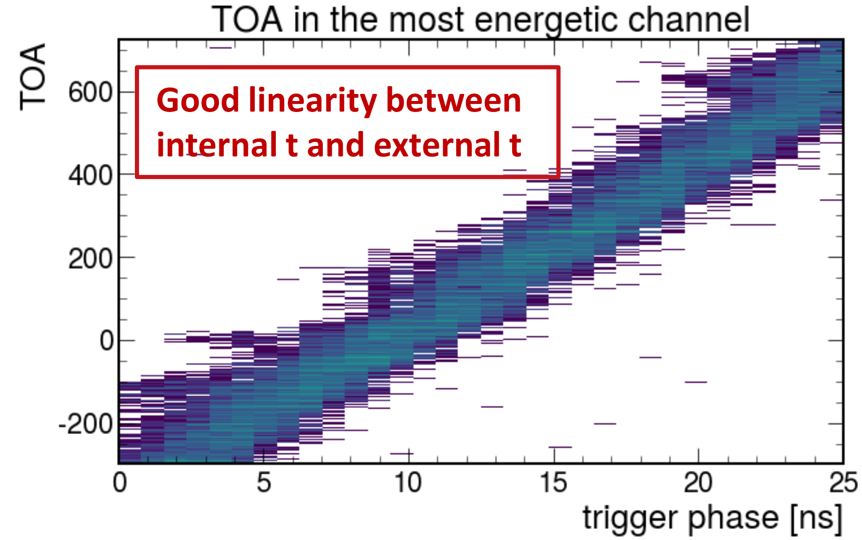


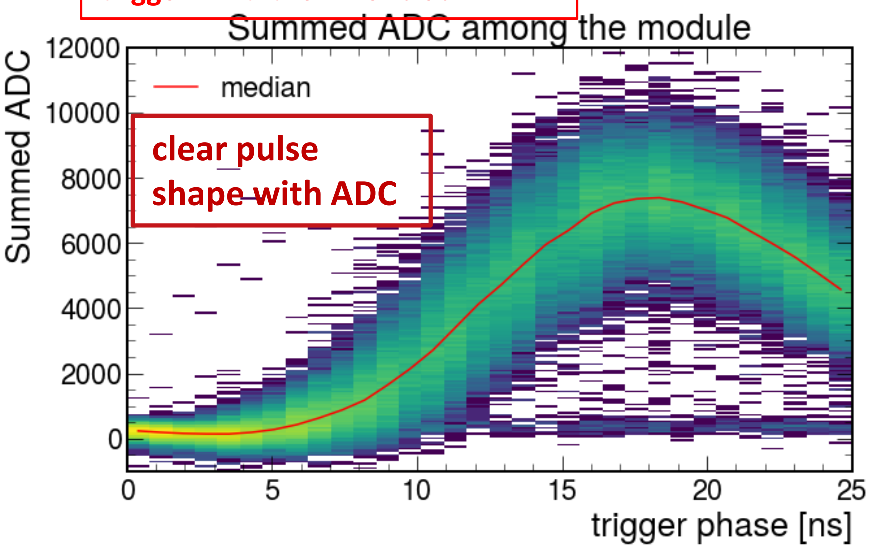
- System monitored by Grafana

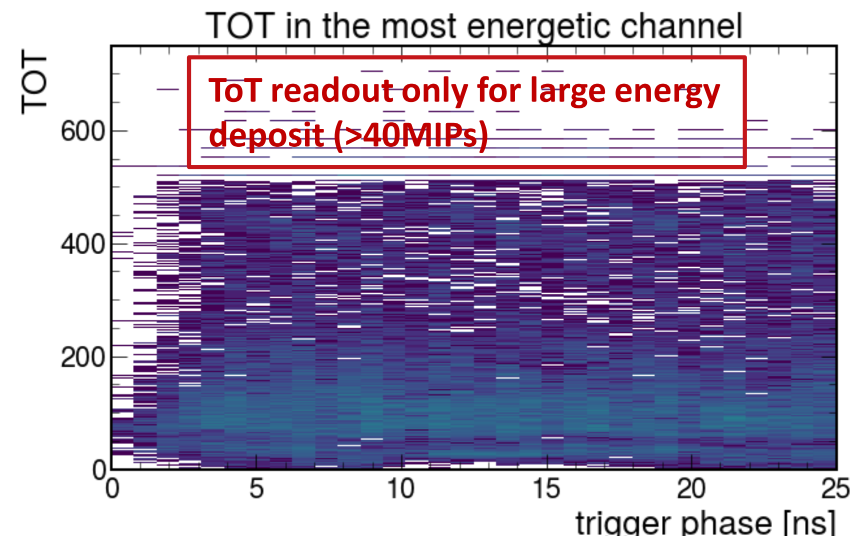
Single module test: first results

- Readout signals from the LD full 200 μm module





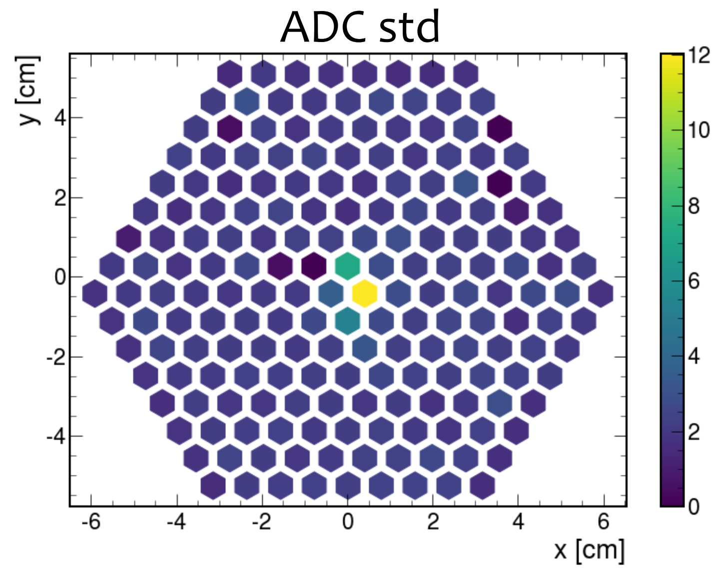




Calibration ongoing for all of these readout

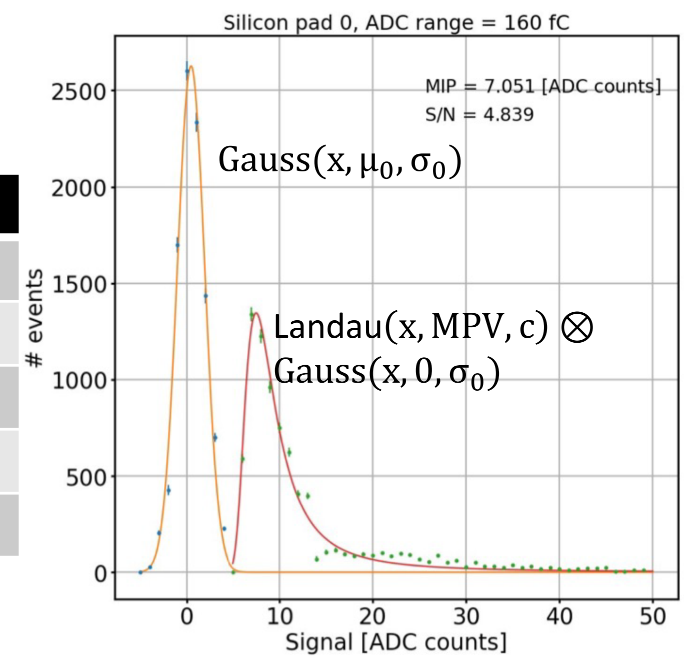
Single module test: first results

- Reconstruction of minimum ionizing particle (**MIP**): an important signature of the detection resolution.
- Use **electron beams with absorbers** to reconstruct MIPs:
  - Narrow beam spot (right plot), moved the table to scan in more channels
  - High rates
- Pion / muon beams: too low rates



- Workflow:
  - Subtract pedestals
  - Subtract noise correlated among channels
  - Select trigger phase to obtain events near the pulse maximum

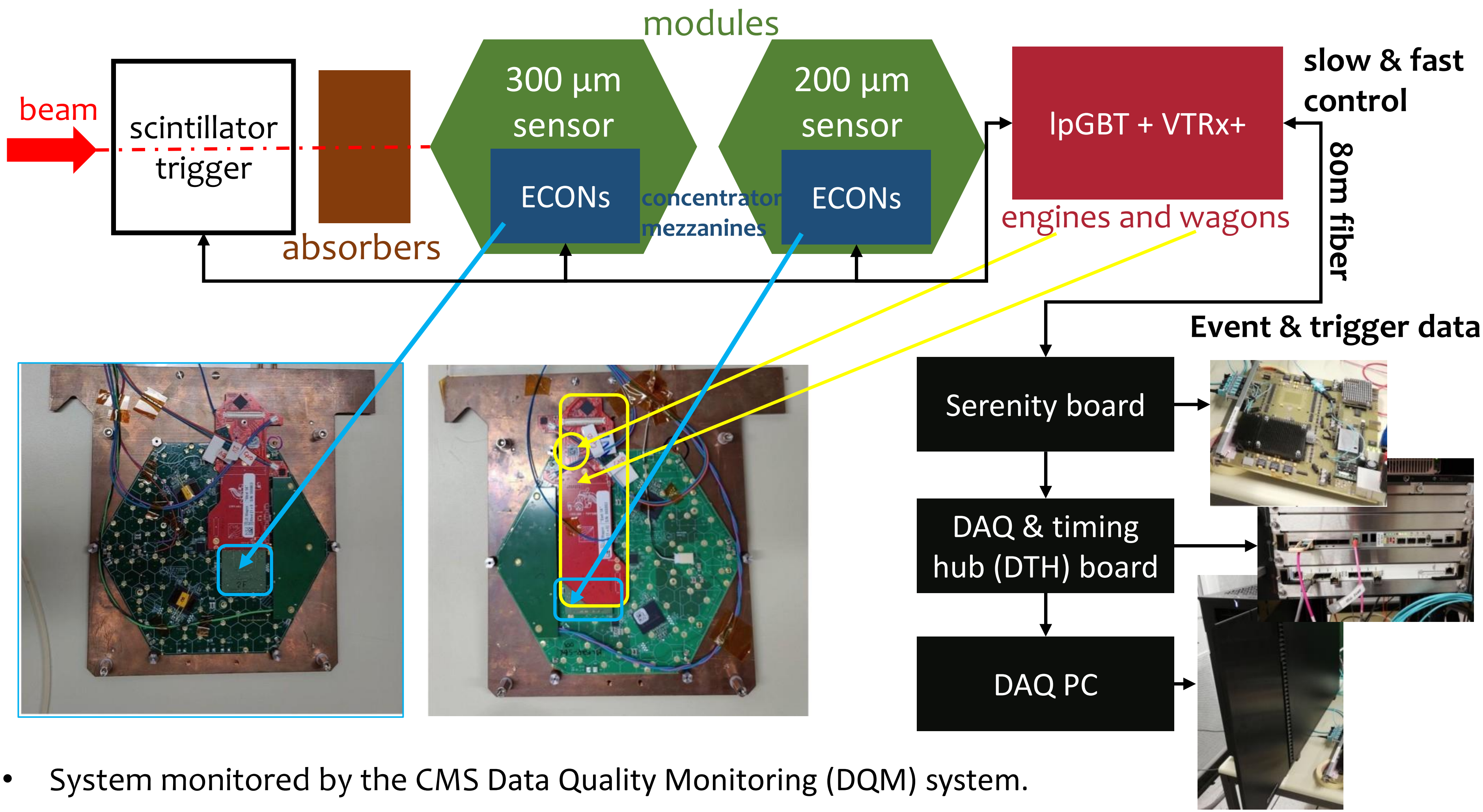
Module	Noise (e^-)	Measured S/N	Expected S/N
LD full, 300 µm	1900	12.8	12.1
LD full, 200 µm	1900	8.4	6.6
LD semi-right, 300 µm	2000	12	12.1
LD semi-left, 300 µm	1950	12.2	12.1
HD full, 120 µm	2000	4.8	5



We meet the expectation !!!

Test of the full electronics chain: setup

- The full electronics chain is assembled, from ECON-D / ECON-T to LpGBT to VTRx+, and to back-end.
- Two modules are tested: both full LD modules, one with 300 µm sensor, the other 200 µm.

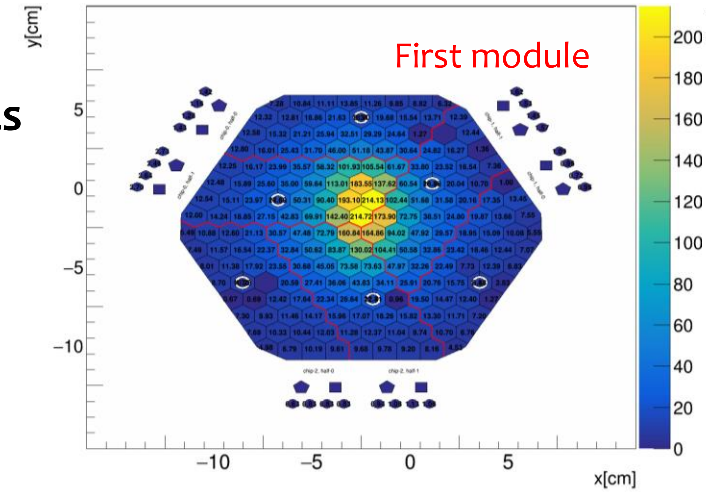


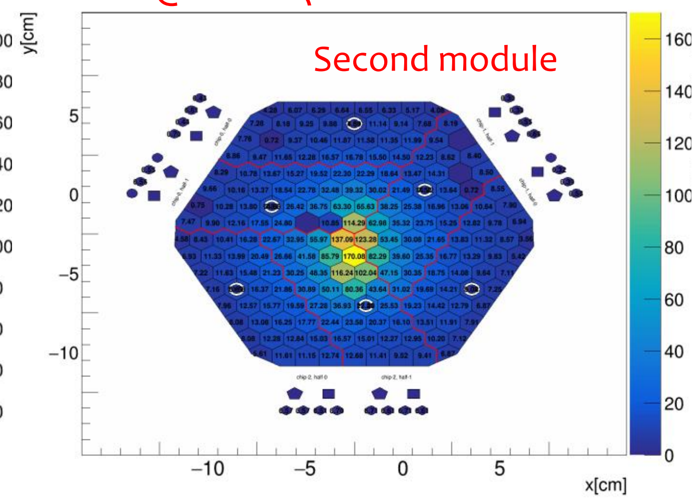
- System monitored by the CMS Data Quality Monitoring (DQM) system.

Test of the full electronics chain: first results

- **Successful readout from the full electronics chain !**
  - Beam spot from a electron run

ADC std from a electron run @CMSDQM

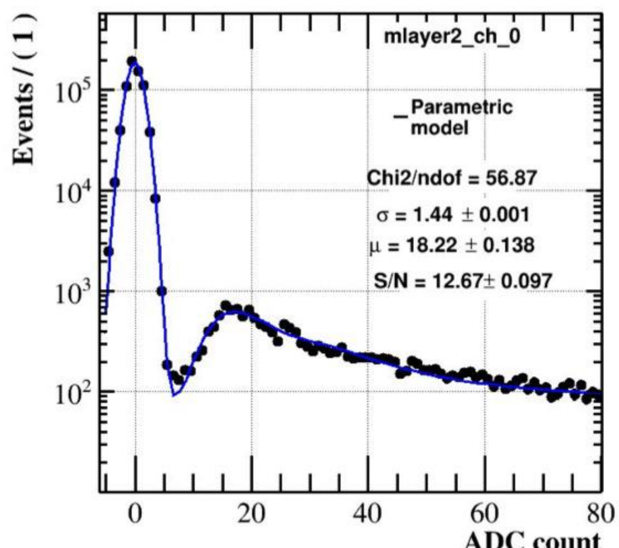


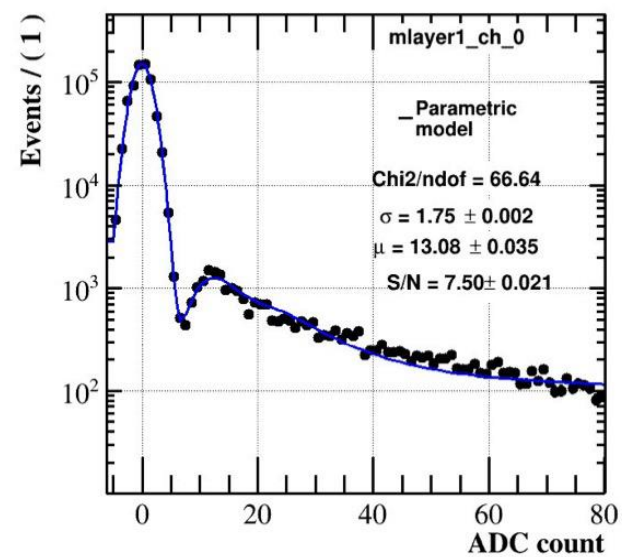


- Similar MIP studies are performed with the long overnight muon beam runs.

- Averaged S/N:
  - 12.5 for 300 µm sensor (single module test: 12.8; expectation: 12.1)
  - 8.1 for 200 µm sensor (single module test: 8.5; expectation: 6.6)

ADC count with MIPS from a muon run



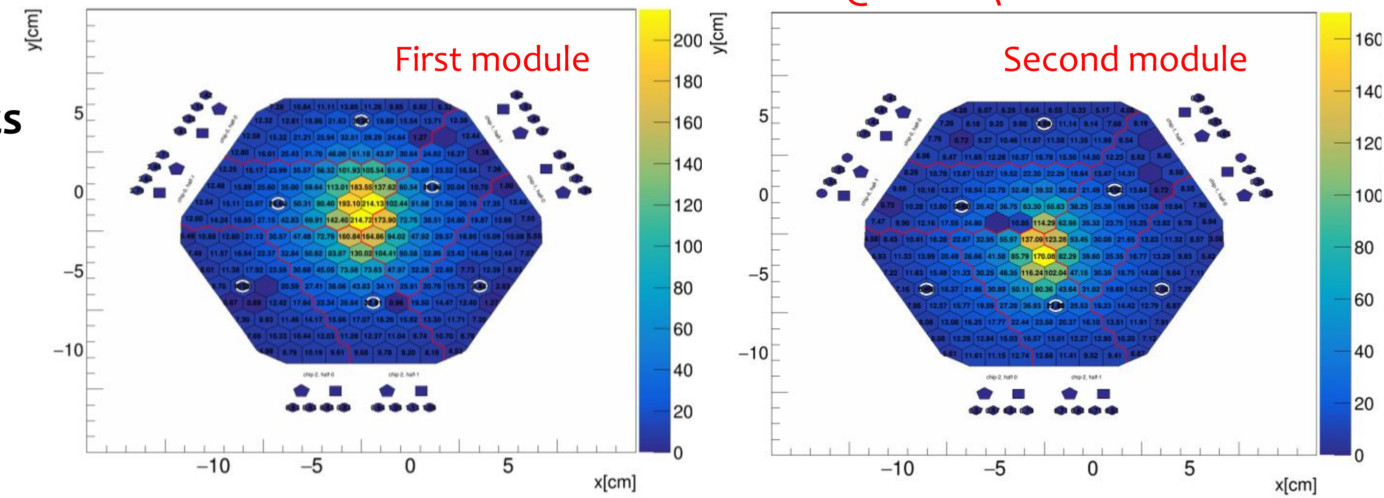


Good S/N and compatible with single module test!

Test of the full electronics chain: first results

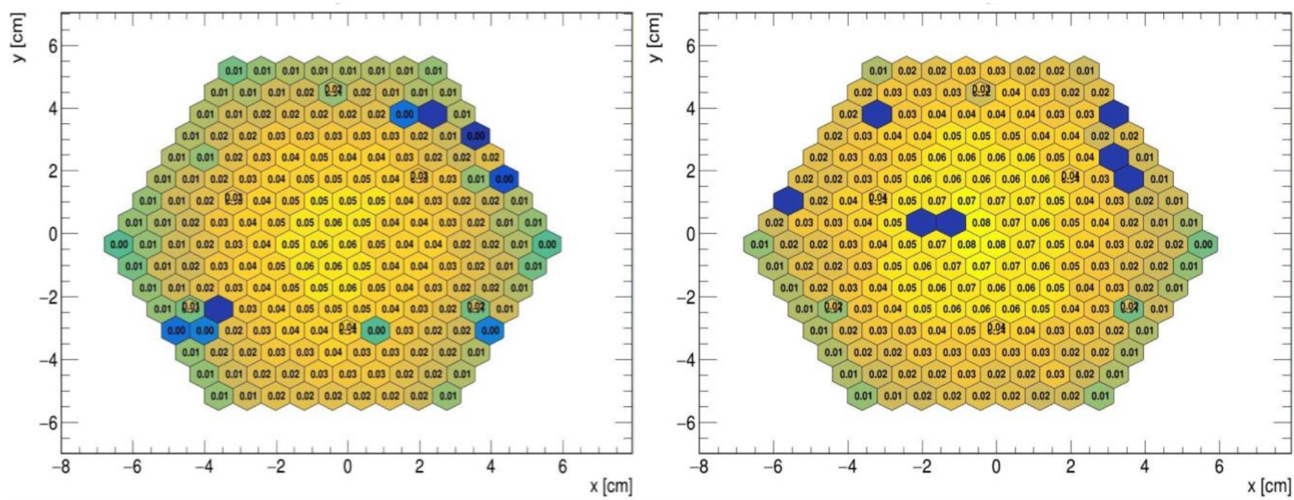
- **Successful readout from the full electronics chain !**
  - Beam spot from a electron run

ADC std from a electron run @CMSDQM



- Similar MIP studies are performed with the long overnight muon beam runs.

Fraction of MIP events in all channels



- Averaged S/N:
  - 12.5 for 300 µm sensor (single module test: 12.8; expectation: 12.1)
  - 8.1 for 200 µm sensor (single module test: 8.5; expectation: 6.6)

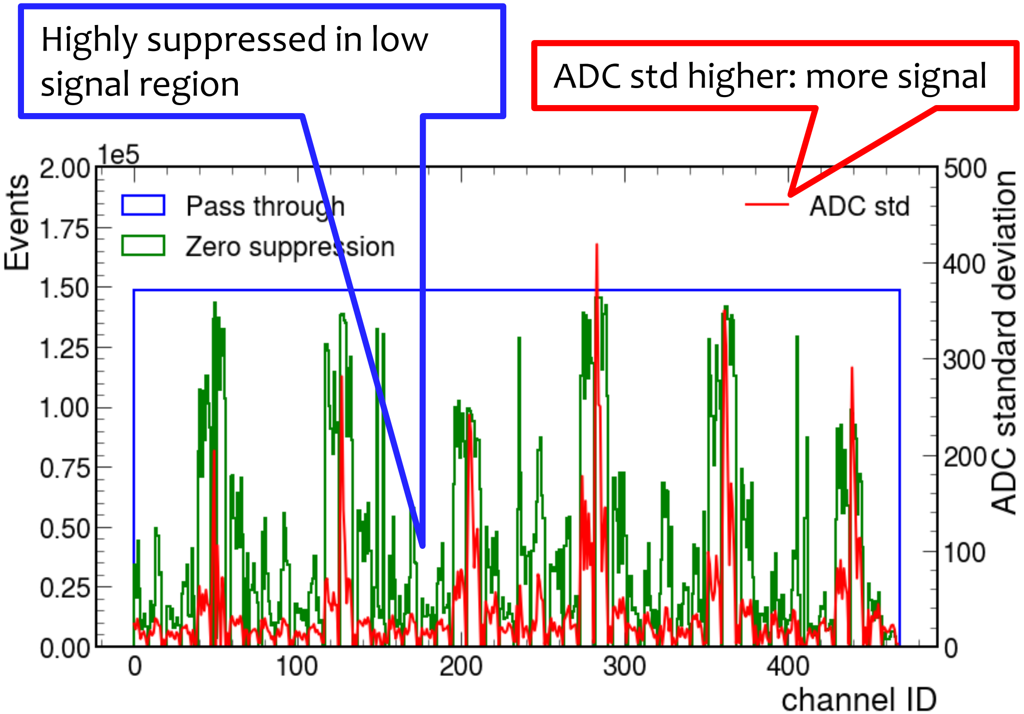
MIP signals seen in almost all channels !

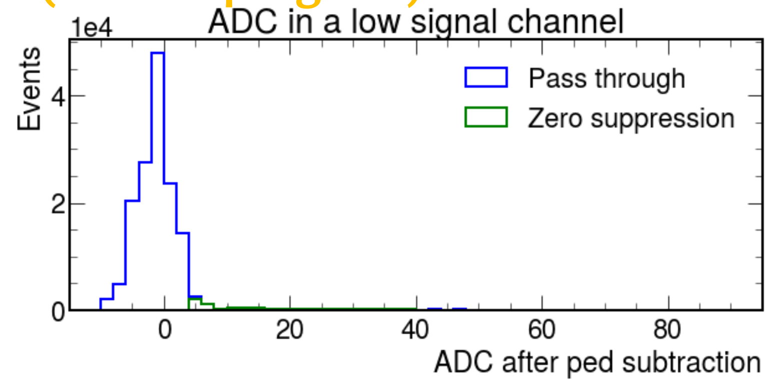
Test of the full electronics chain: first results

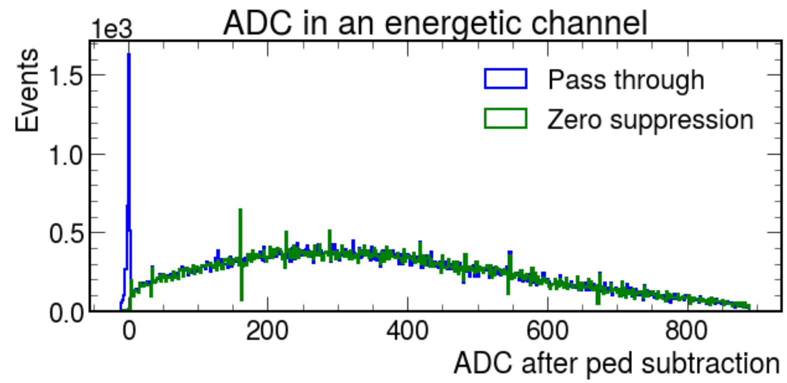
- **ECON-D zero suppression (ZS)**
  - The ECON-D can perform zero-suppression to only readout channels with sufficient energy (>3×Noise) and reduce the amount of readout data
  - Data are taken mostly with *passthrough* mode: no zero suppression is needed
  - Some runs are taken with *zero suppression* mode:

$$A > C + f(A_{CM}) + f(A_{last\ BX})$$

    - C = pedestal + 3 × noise from pedestal runs.
    - $f(A_{CM}) + f(A_{last\ BX})$ = 0: noise studies needed to determine them.
- **Effect of the zero-suppression in the electron run (work in progress)**



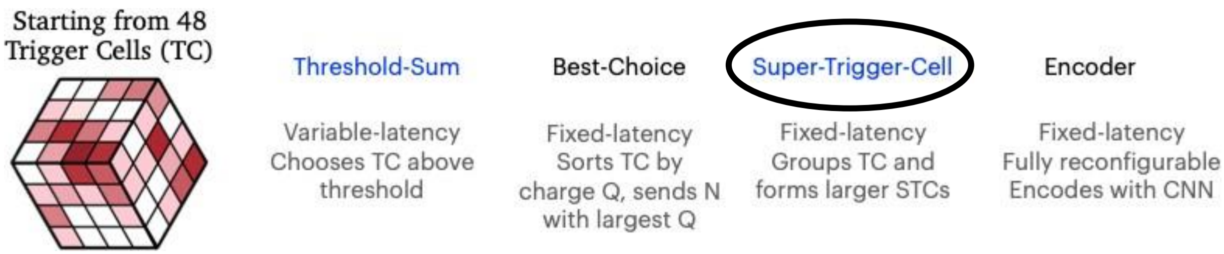




Test of the full electronics chain: first results

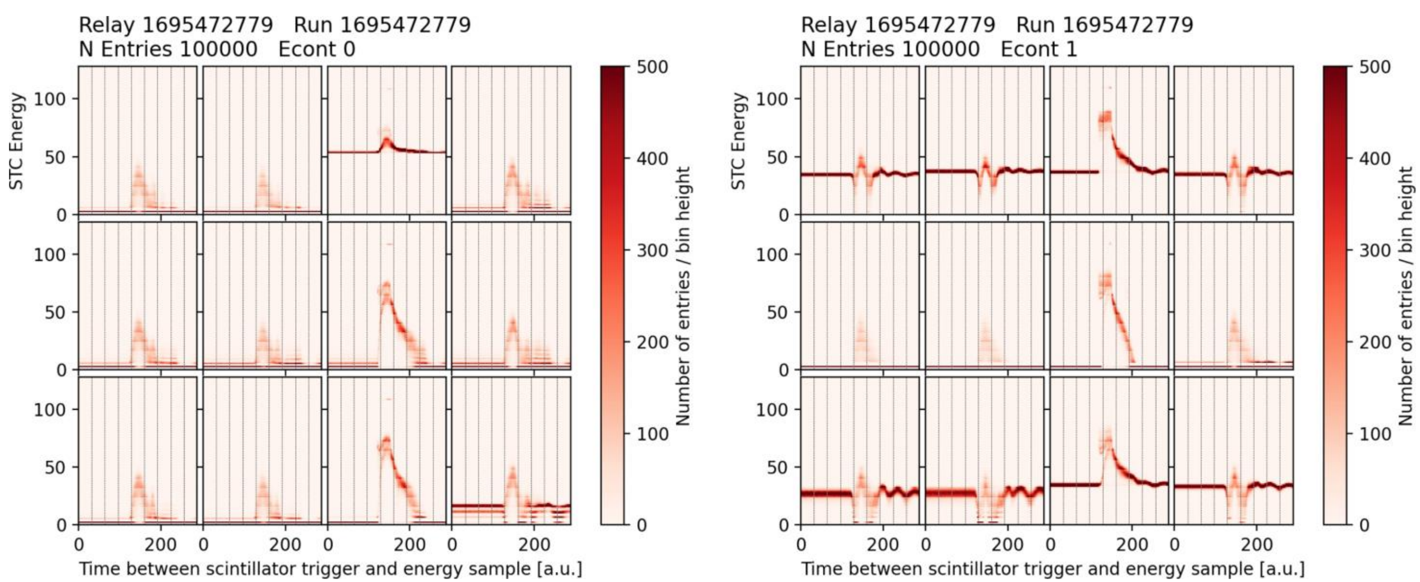
➢ **Data from ECON-T (Work in progress)**

- ECON-T takes data from the trigger path of HGCROC, generate charges for each trigger cell, and use certain algorithms to pass on information for trigger decision



- ECON-T configured mostly with Super Trigger Cell (STC) algorithm (for trigger decision): group every 2 by 2 trigger cells into one super trigger cell

STC readout as a function of the trigger phase in the two ECON-Ts

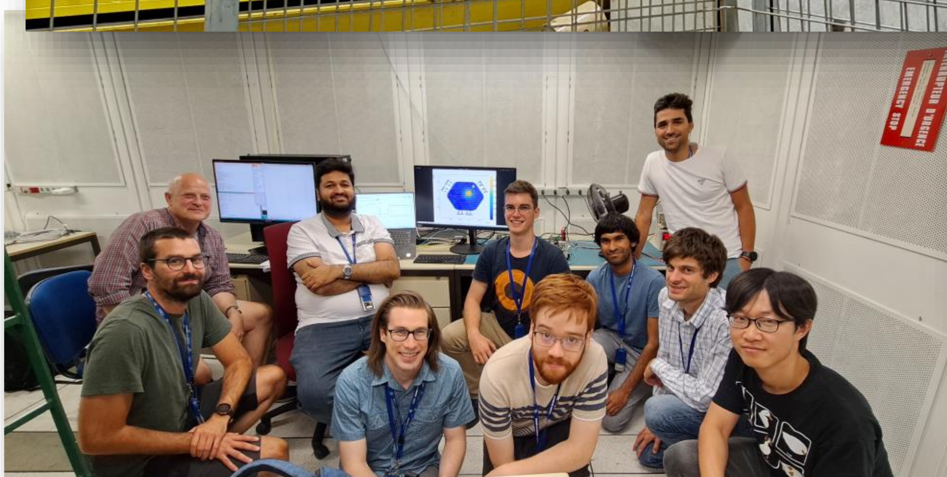


Conclusion

- **The progress and first results are presented, from the HGCAL beam tests in 2023, happened at CERN SPS H4 beamline.**
  - **Multiple silicon modules** have been available and tested, showing good performances.
  - Successful readout from the **full electronics chain** in the HGCAL prototype, in both DAQ and trigger paths.
  - **Analyses ongoing**, including noise studies, calibration of ADC, TOT and TOA, more studies of trigger readout.

- **HGCAL beam test in 2024!**
  - Expect 4 weeks in the summer, with one week only parasitic for preparation.
  - Larger prototypes: **more modules** in one layer, combination with **tile-scintillator modules**
  - Test performances with **magnetic field** (up to 3 Tesla).

Conclusion



Credits to everyone participating in the beam test !

Thanks for your attention !

Backup

The hexaboard controller of the single module test

Hexaboard interface (95 IO)

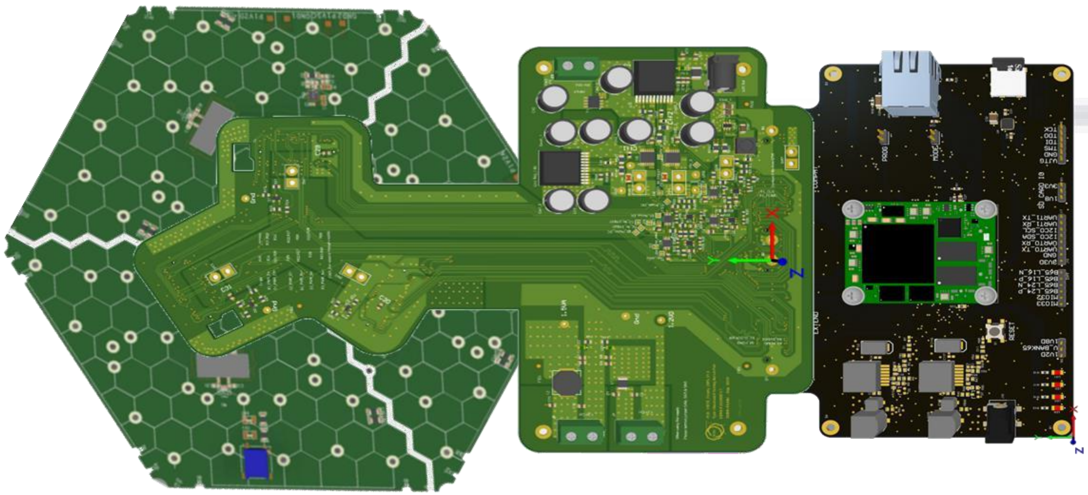
- 21 low speed control lines (used by the hexaboard)
- 5 I2C lines (clock, data)
- 4 low speed control lines (used for ADC Ready signals)
- 30 high speed differential lines (3x4 data + 3x4 trg + 3 clk320 +3 fcmd)

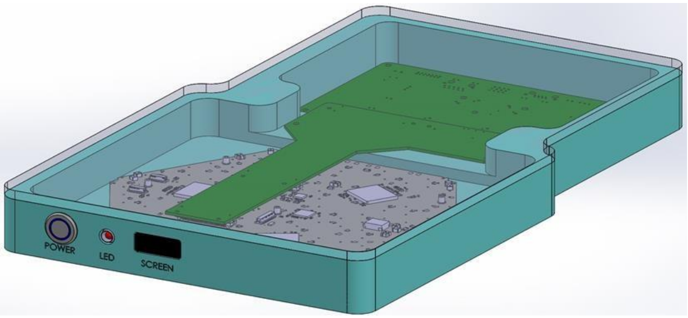
Trigger interface (8 IO)

- 4x Differential signal on RJ45 connector.

Processing system side

- 2 x userIO
- 1 x Serial
- 1 x I2C





The Grafana interface